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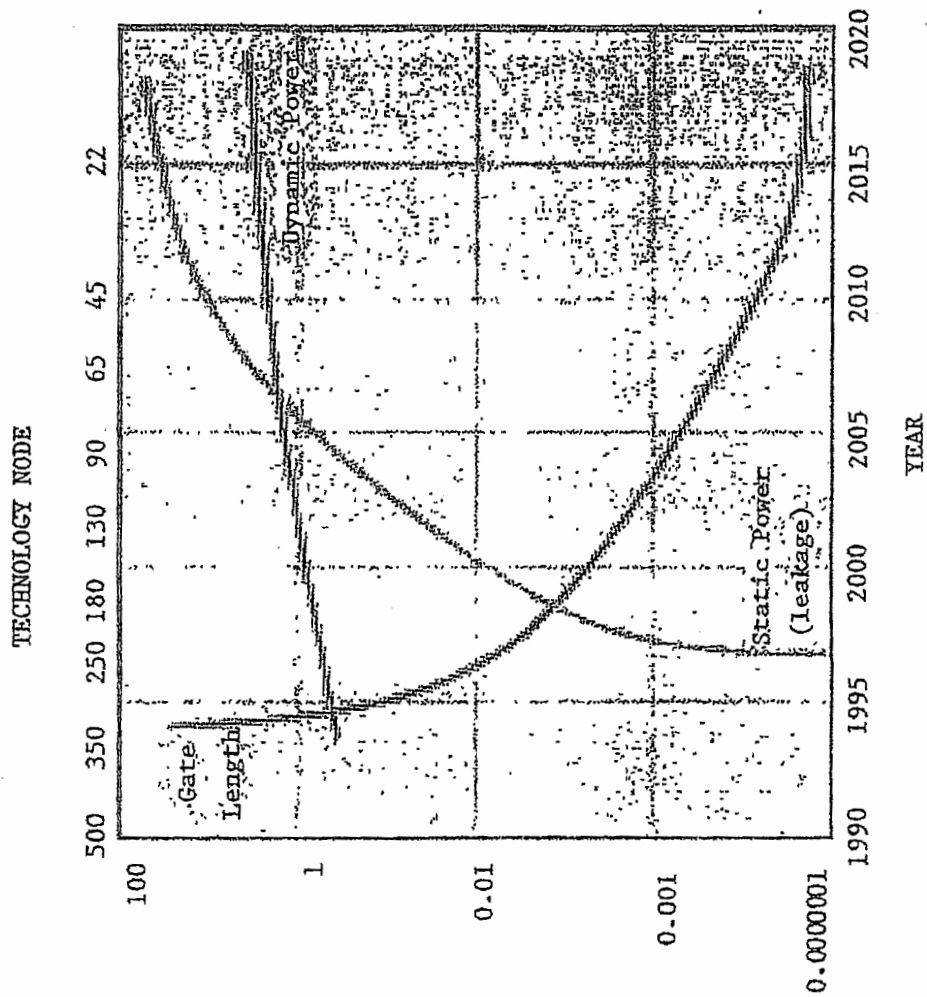


Figure 1: PRIOR ART

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Processors Today are Inefficient

Processor (90nm)	Energy/Operation (pJ) (32-bit Op)
ASIC	2
DSP	60
RISC	200
PC/Workstation	2,000

Figure 2: PRIOR ART

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Operation	Energy (0.13 μm)
32 Bit ALU Operation	5 pJ
32 Bit Register Read	10 pJ
Read 32 Bits from 8KB RAM	50 pJ
Transfer 32 Bits Across Chip (10 mm)	100 pJ
OCD Transfer 32 Bits Off Chip	1.9 pJ

Figure 3: PRIOR ART

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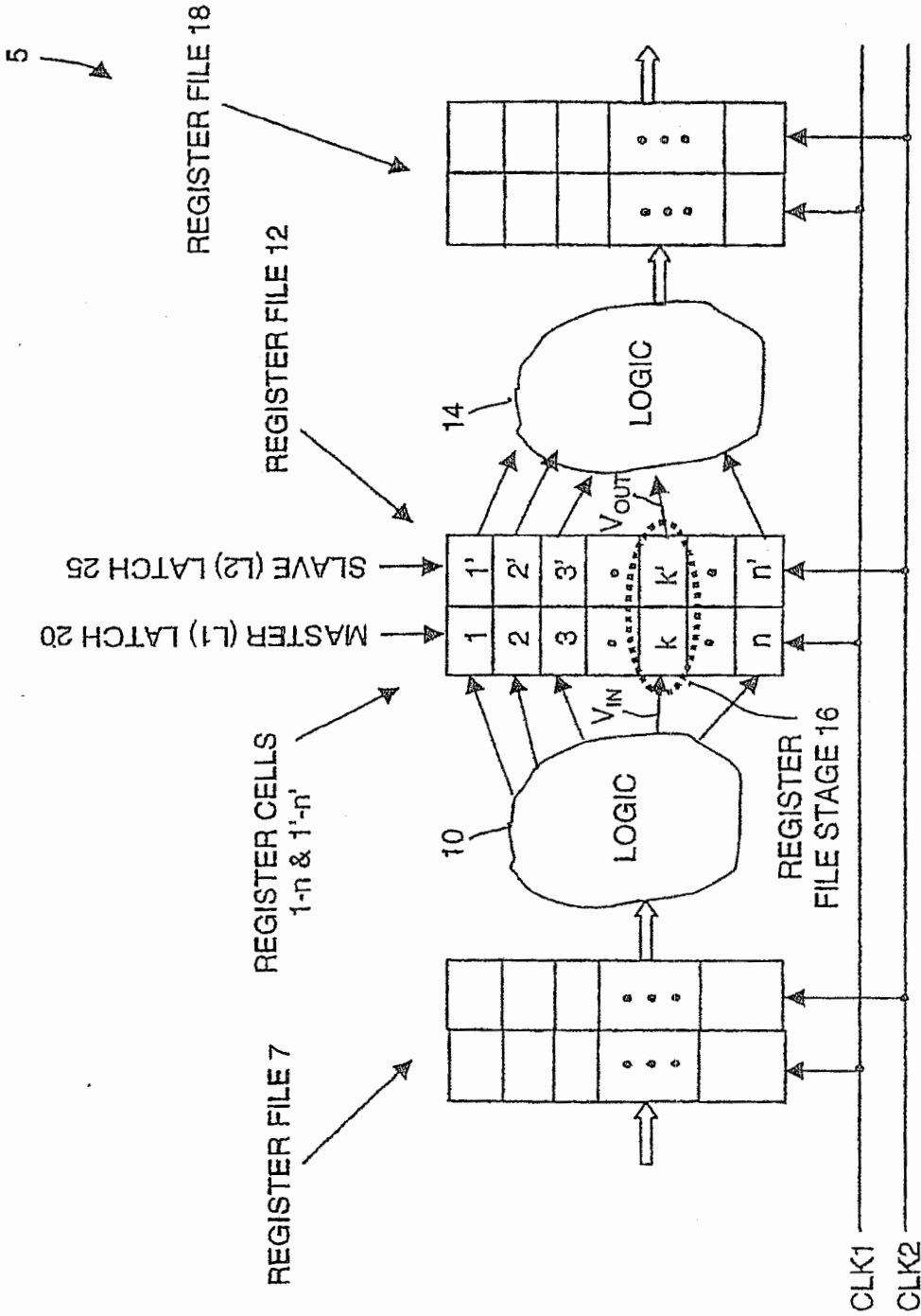


Figure 4A: PRIOR ART

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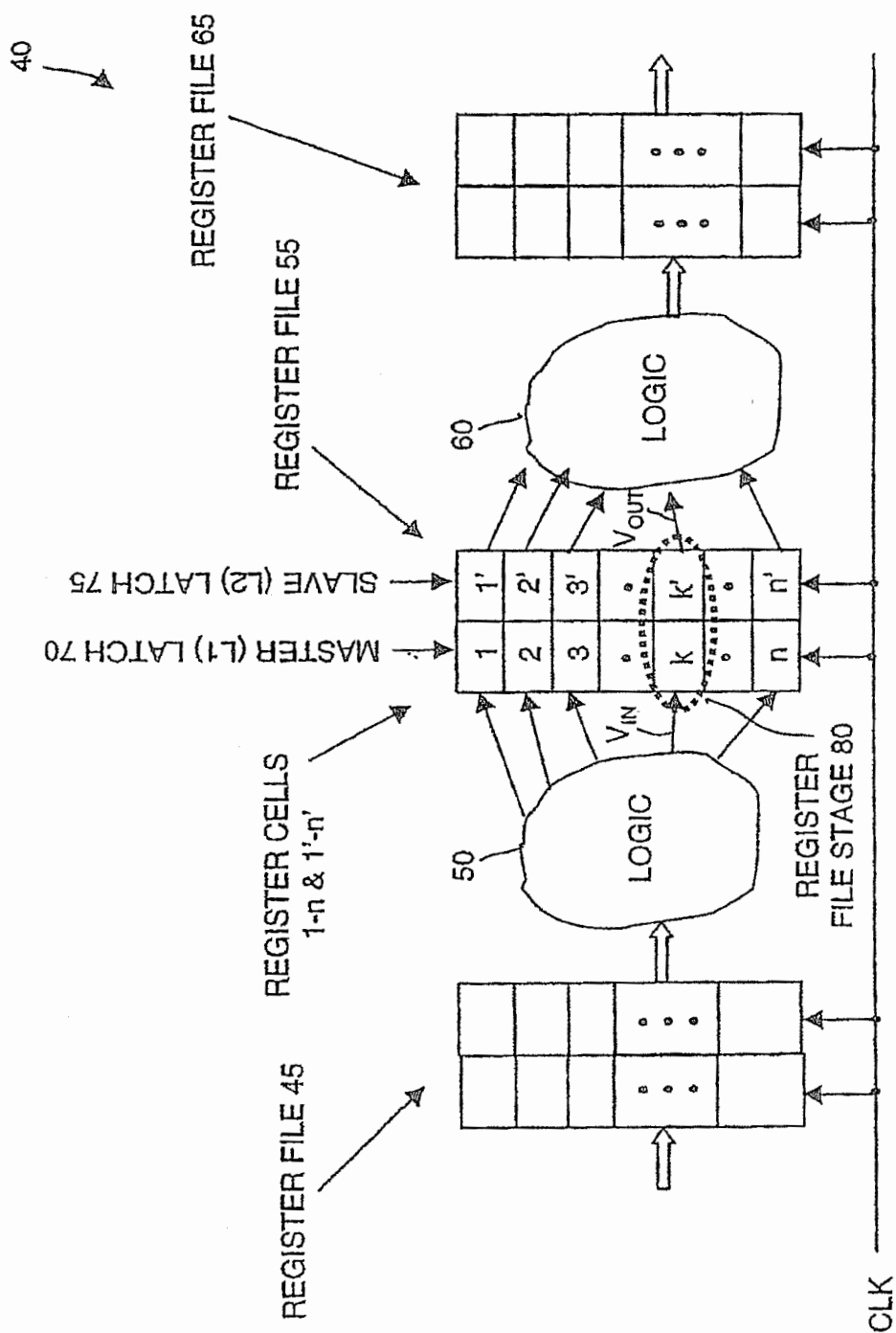


Figure 4B: PRIOR ART

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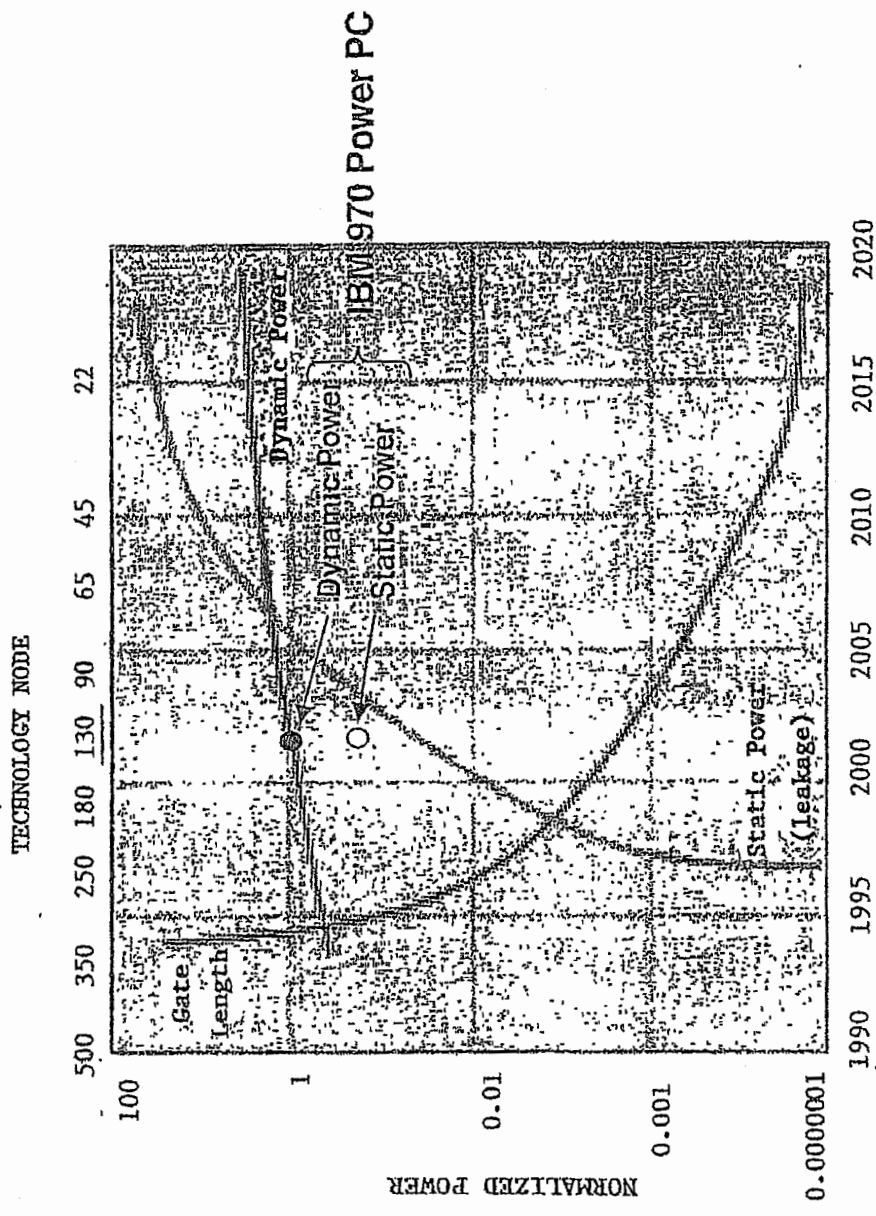


Figure 5: PRIOR ART

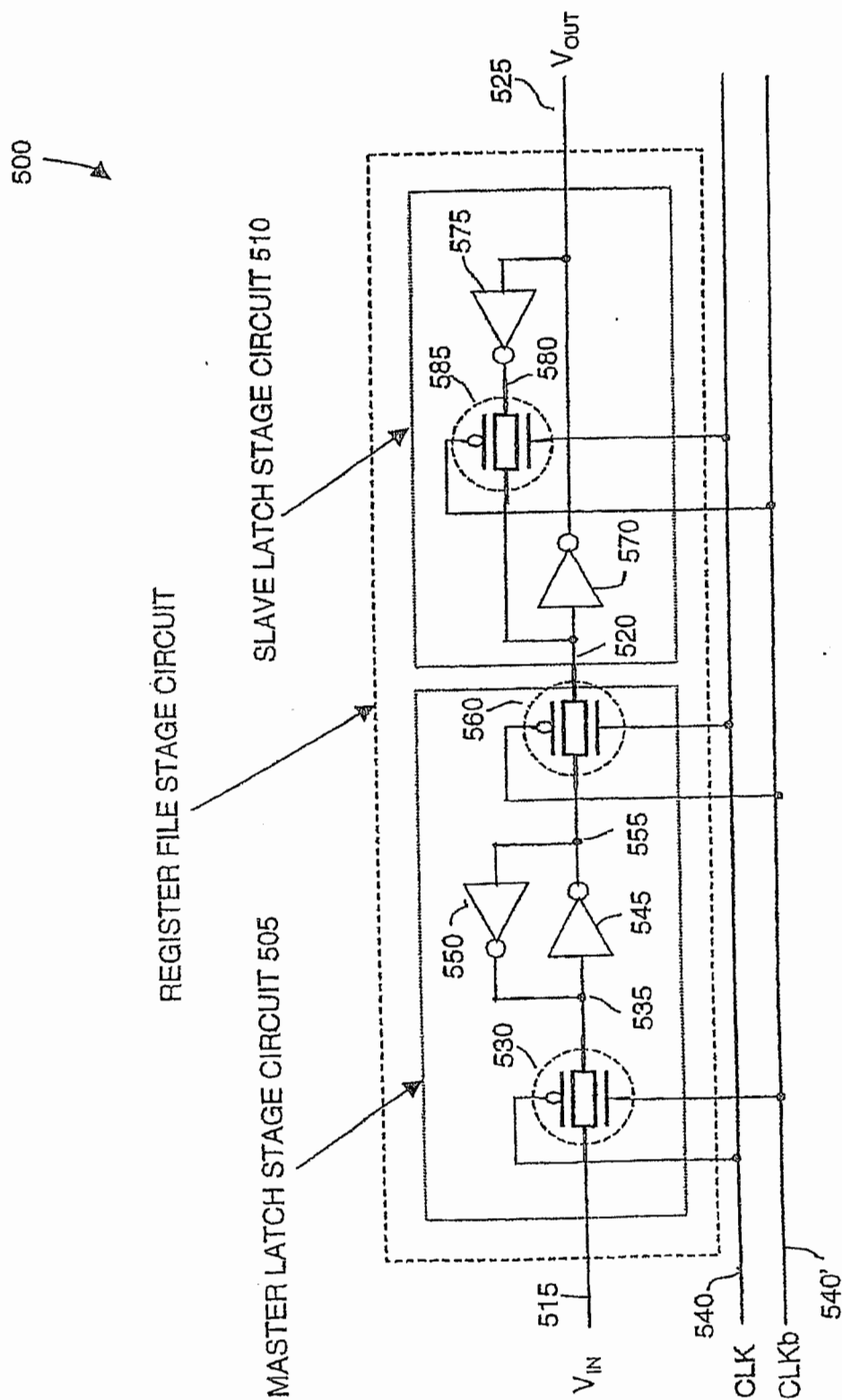


Figure 6: PRIOR ART

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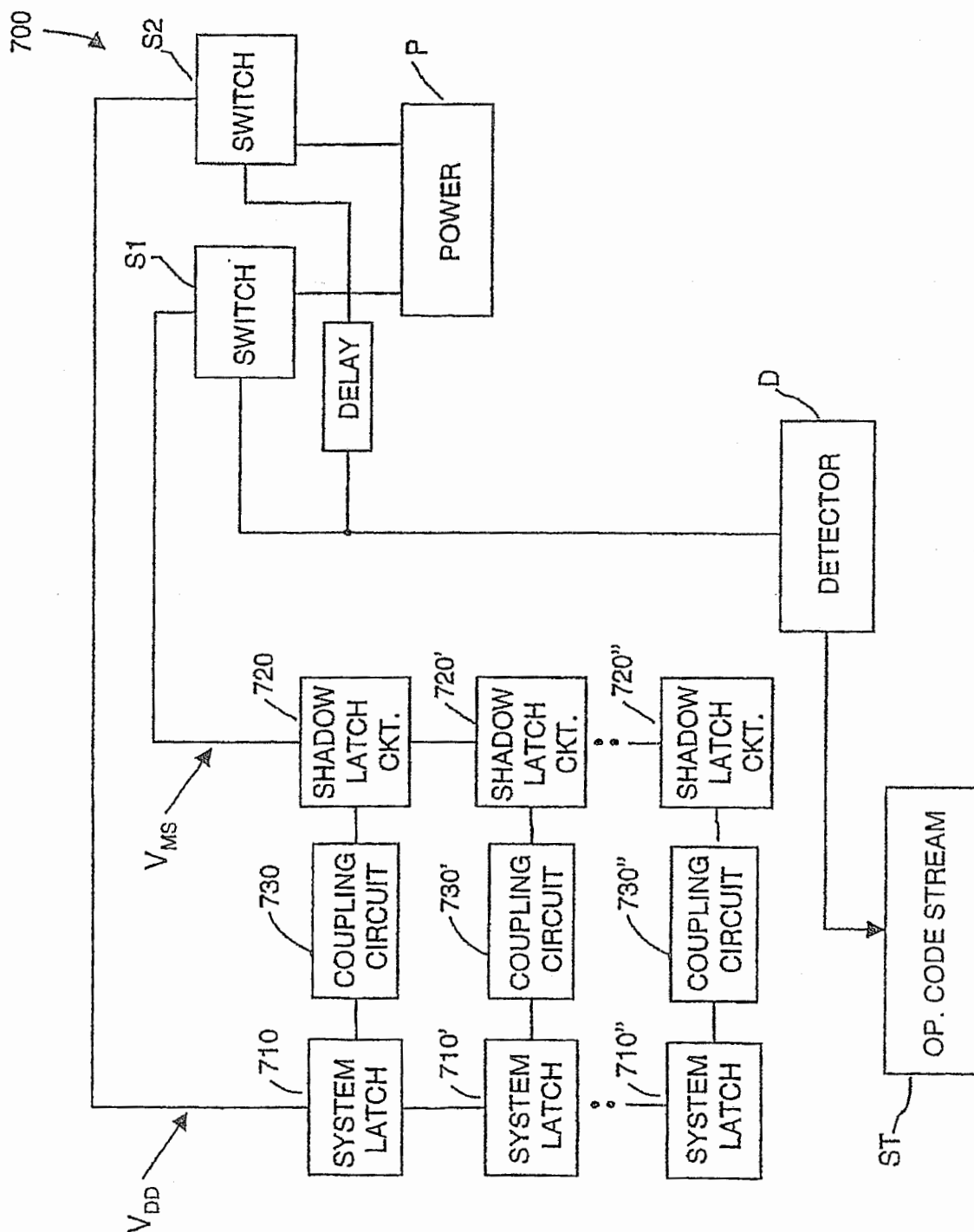


Figure 7: PRIOR ART

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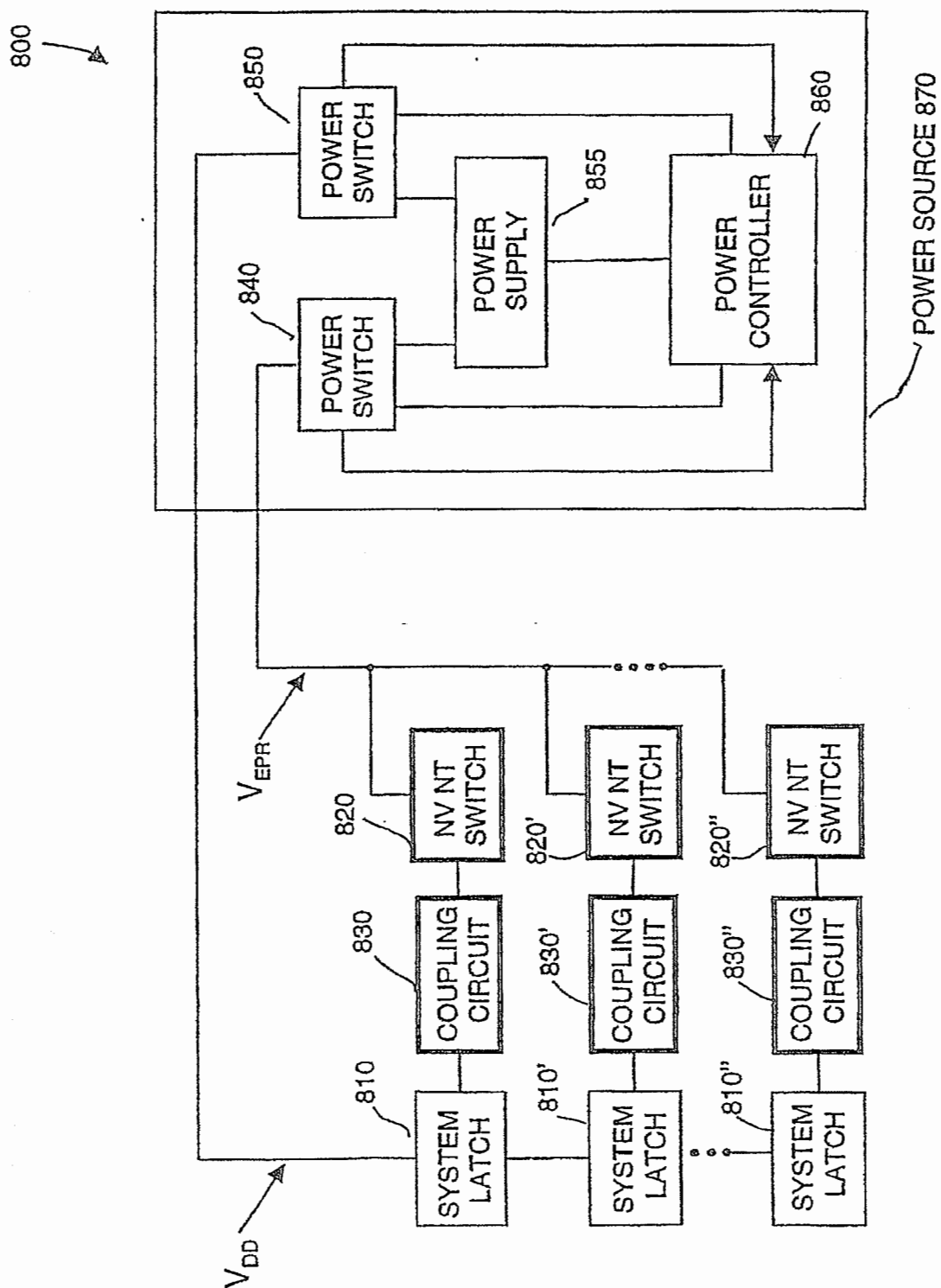


Figure 8A

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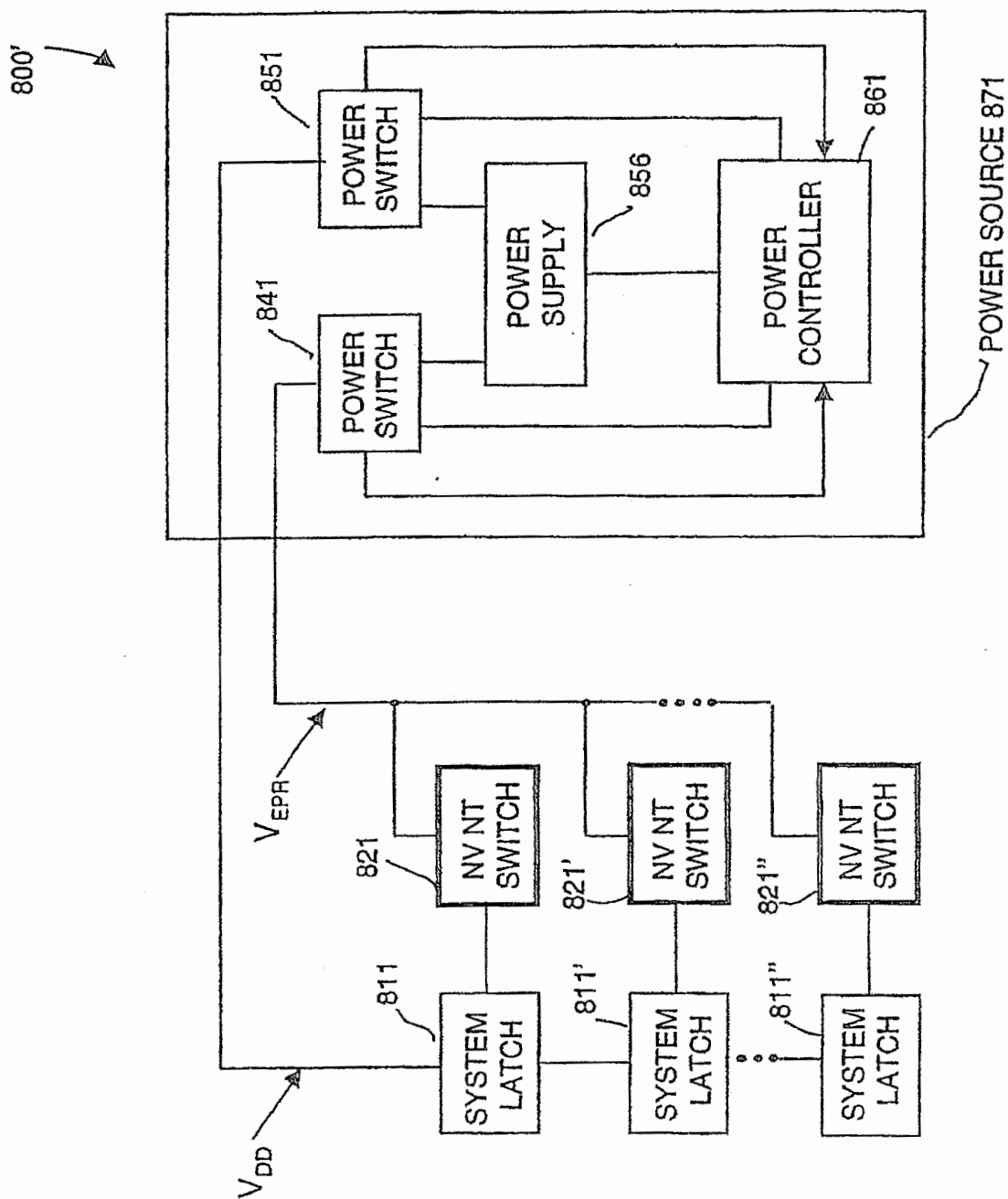


Figure 8B

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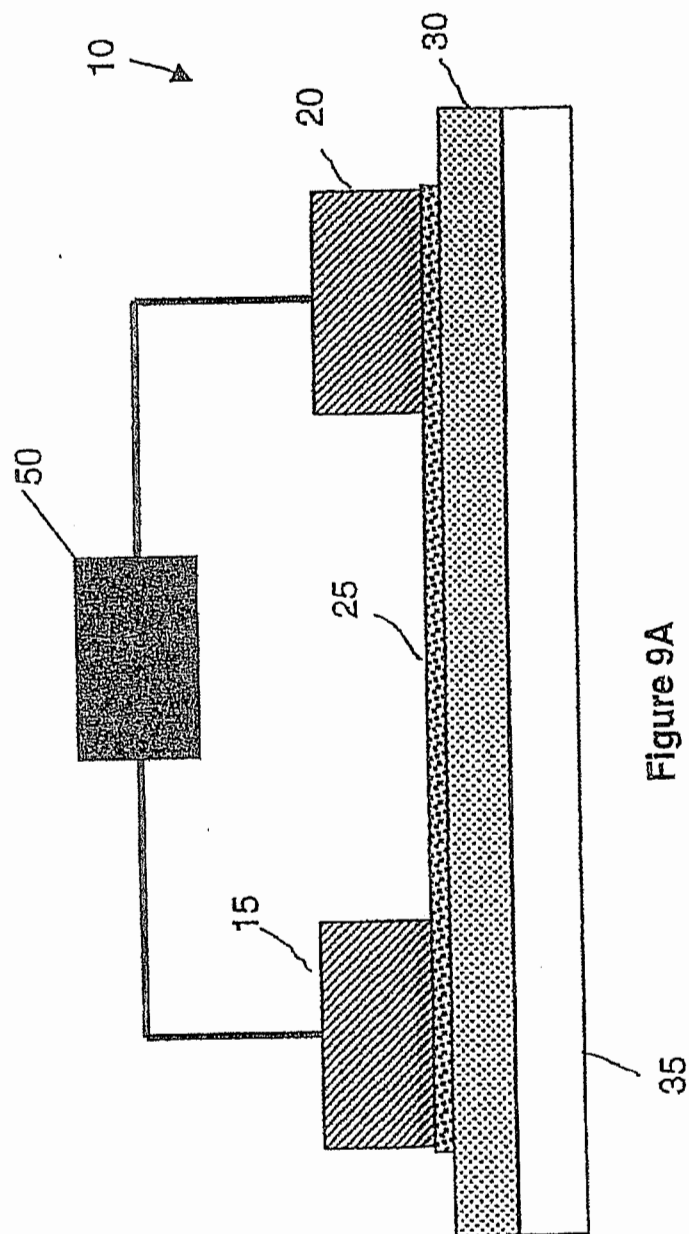


Figure 9A

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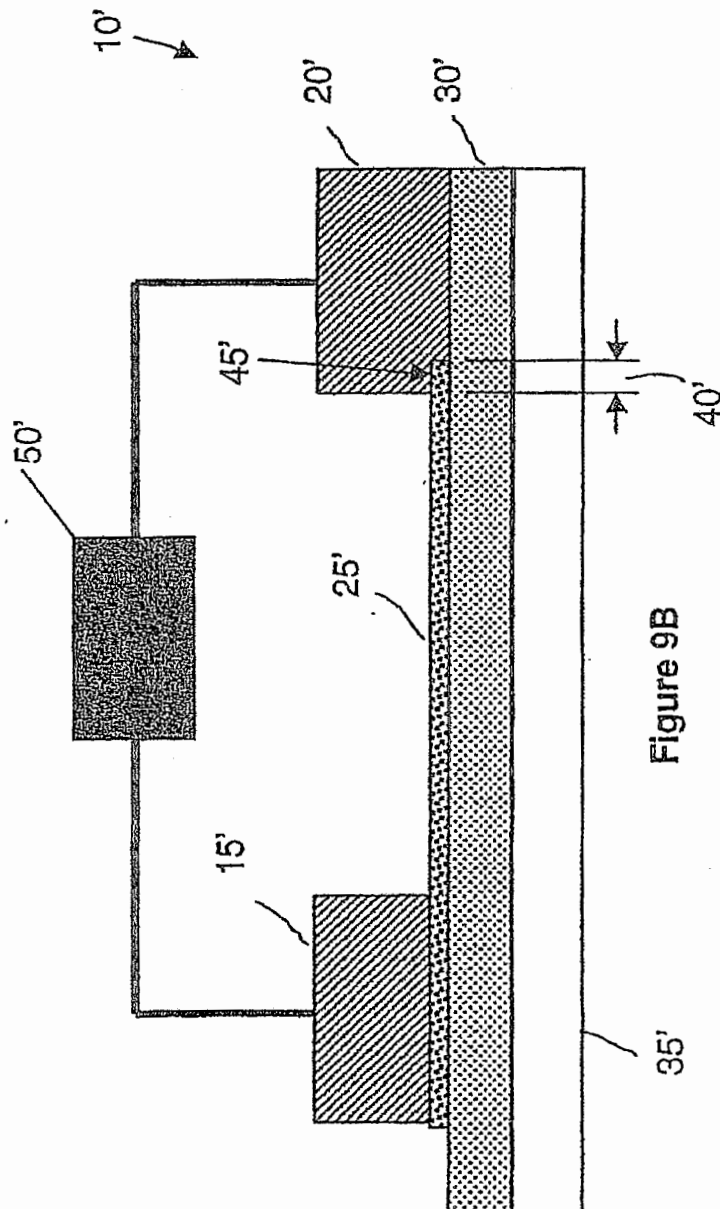


Figure 9B

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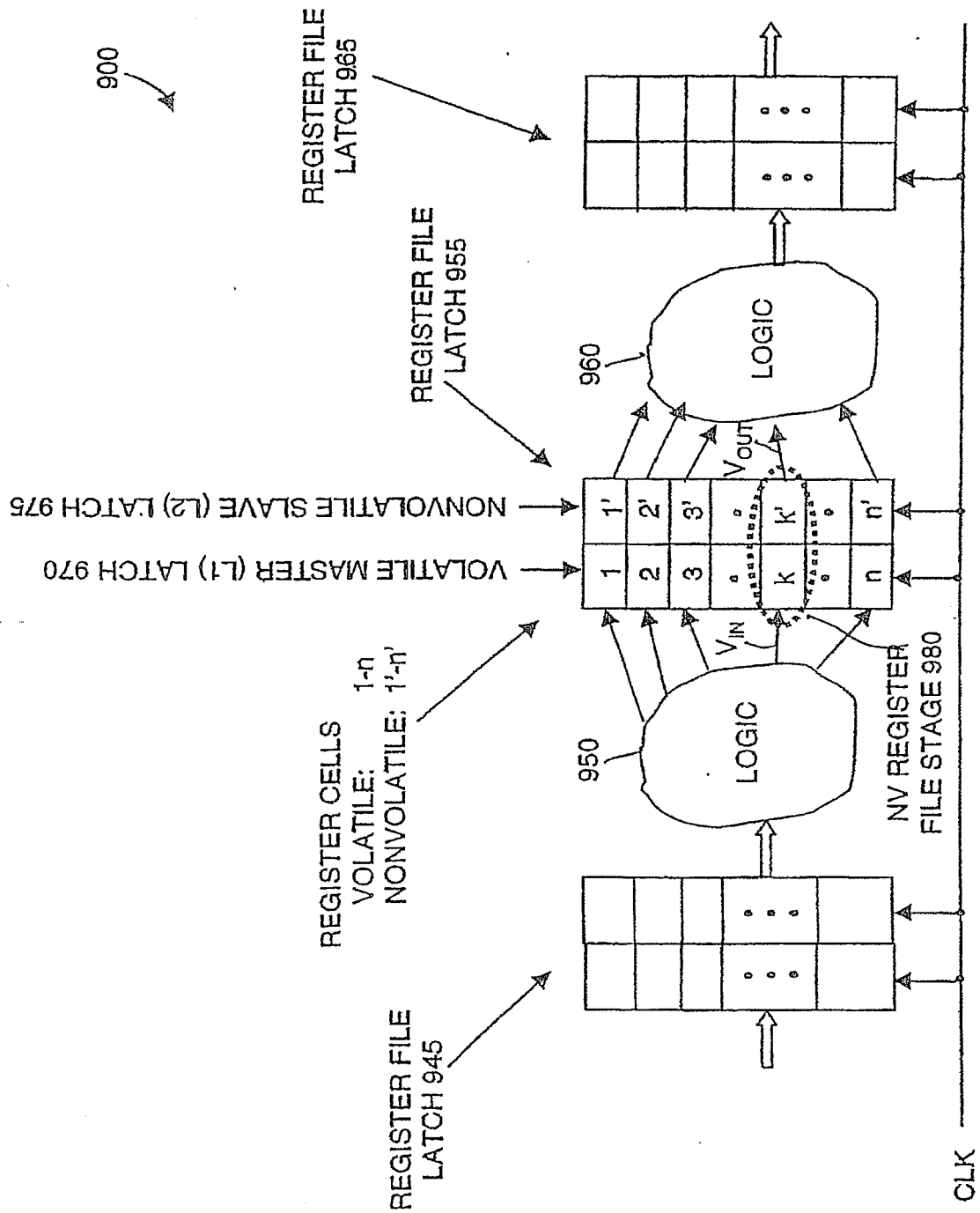


Figure 10

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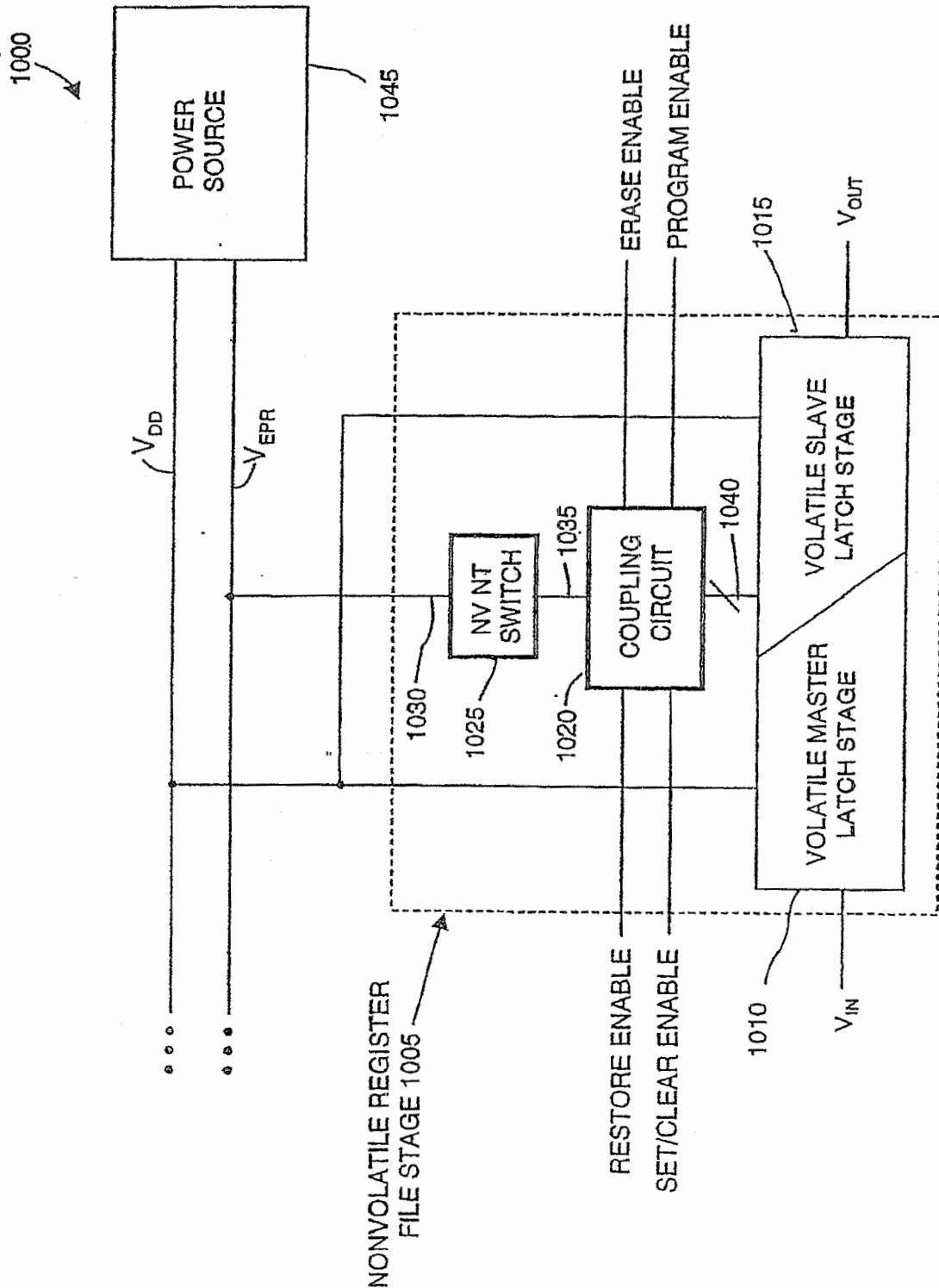


Figure 11A

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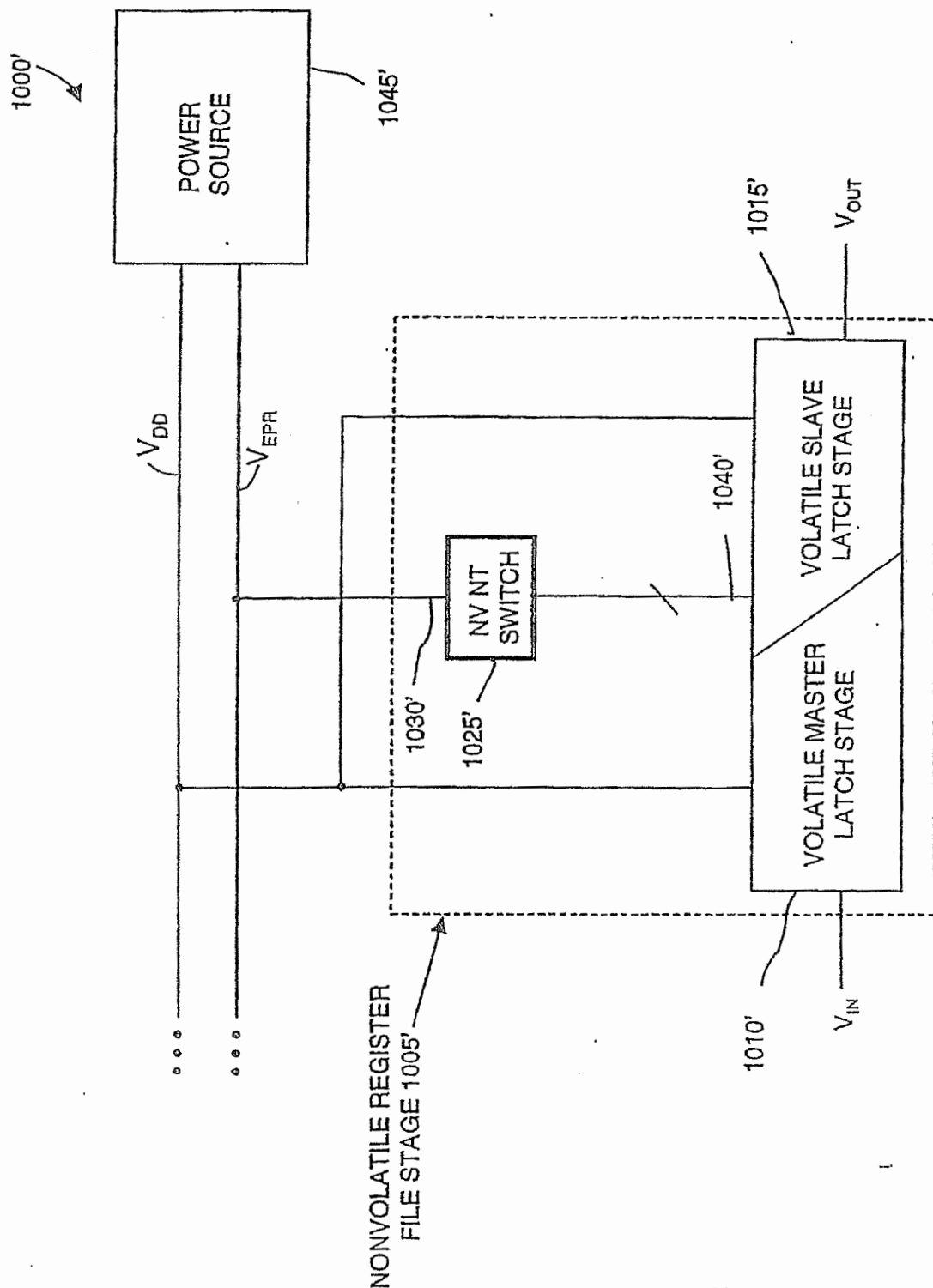


Figure 11B

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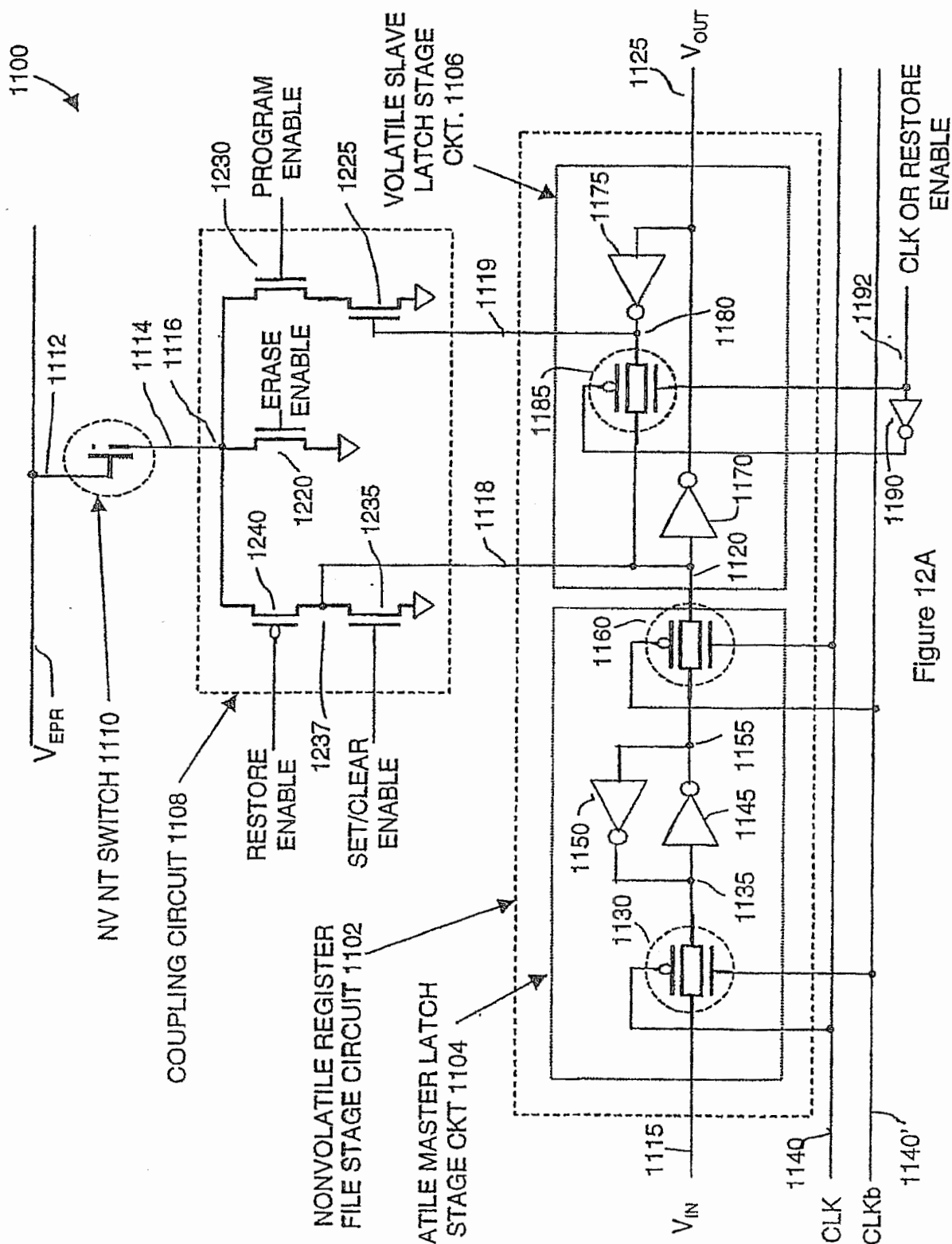


Figure 12A

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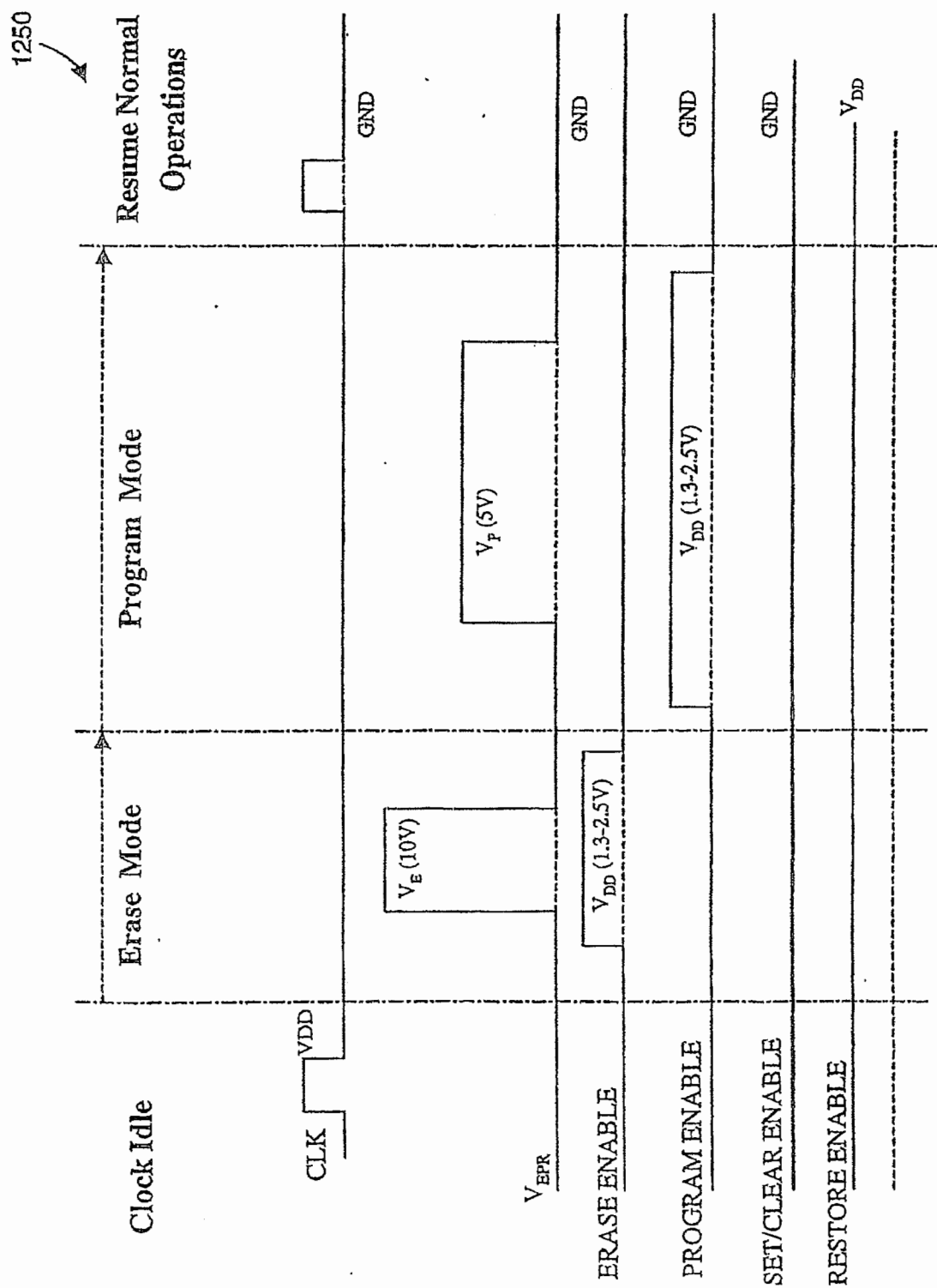


Figure 12B

1300

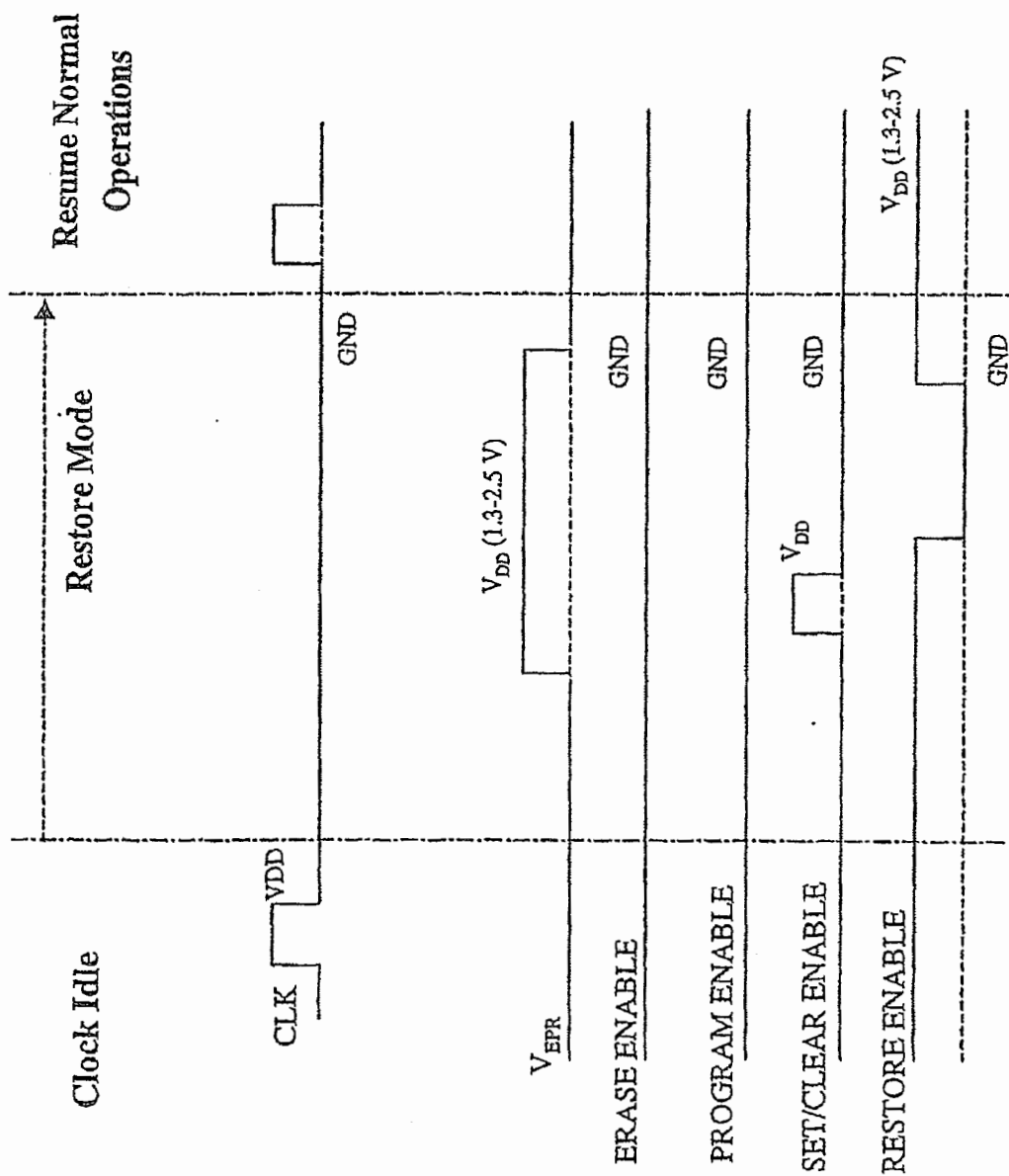


Figure 12C

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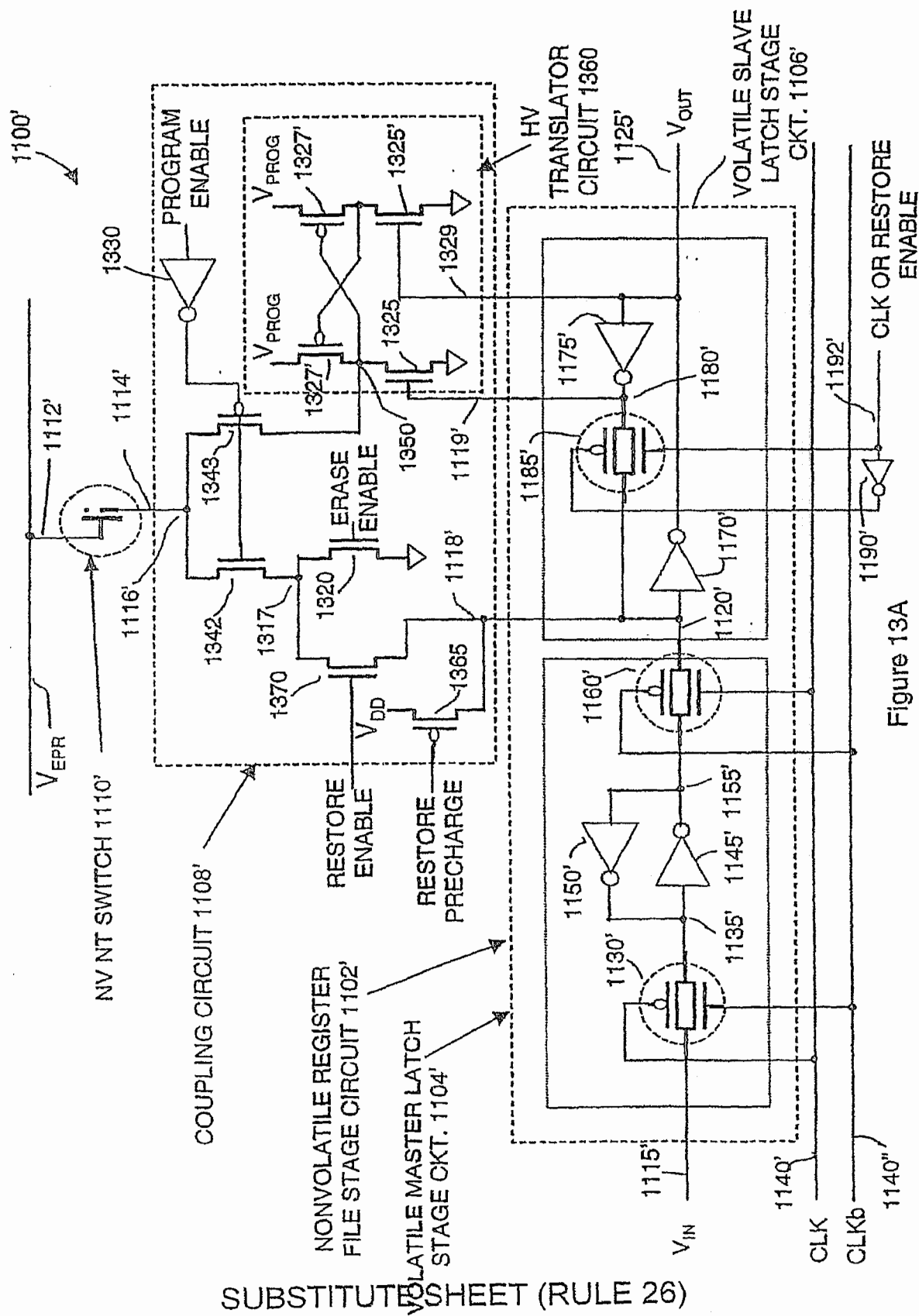


Figure 13A

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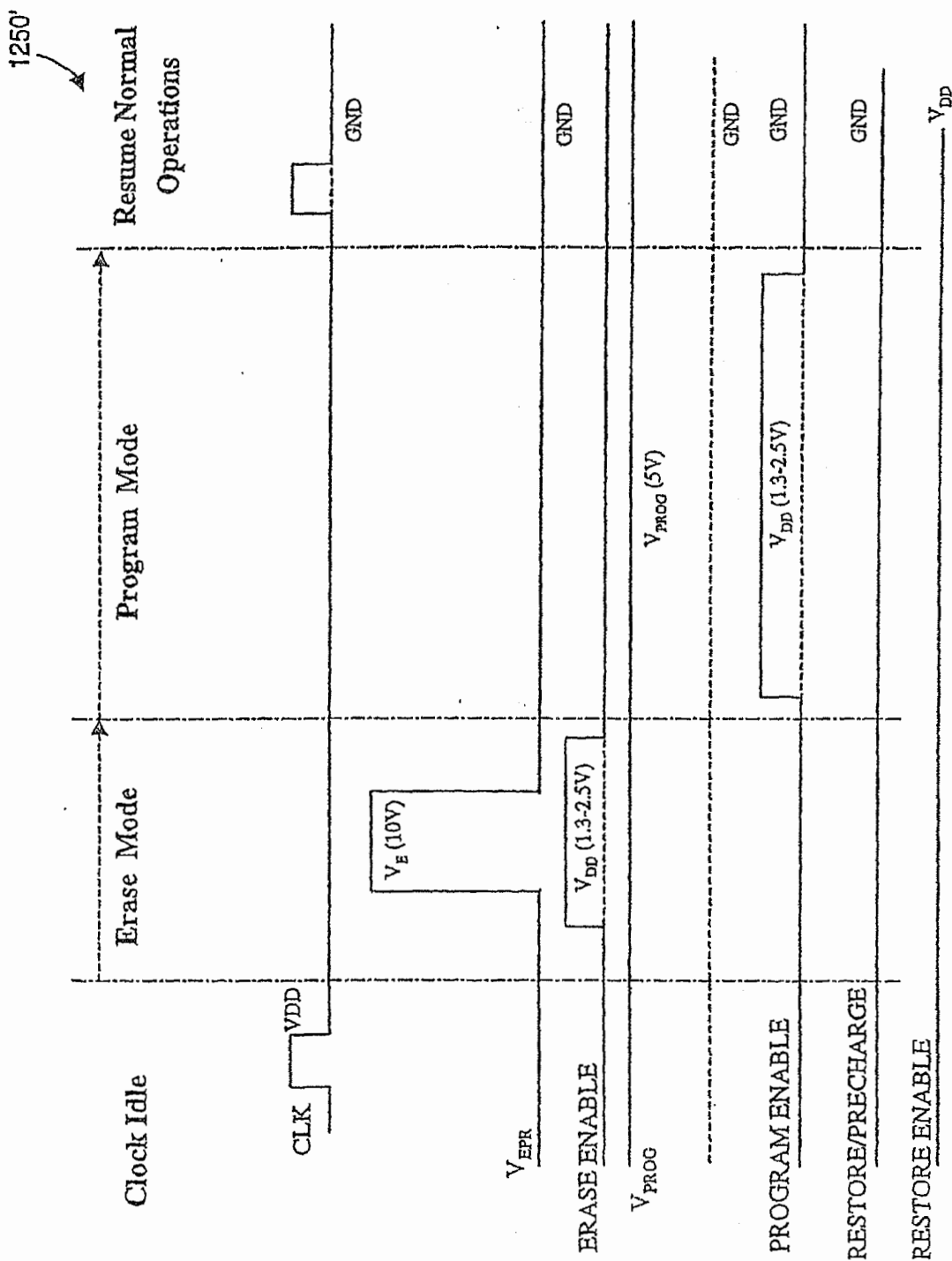


Figure 13B

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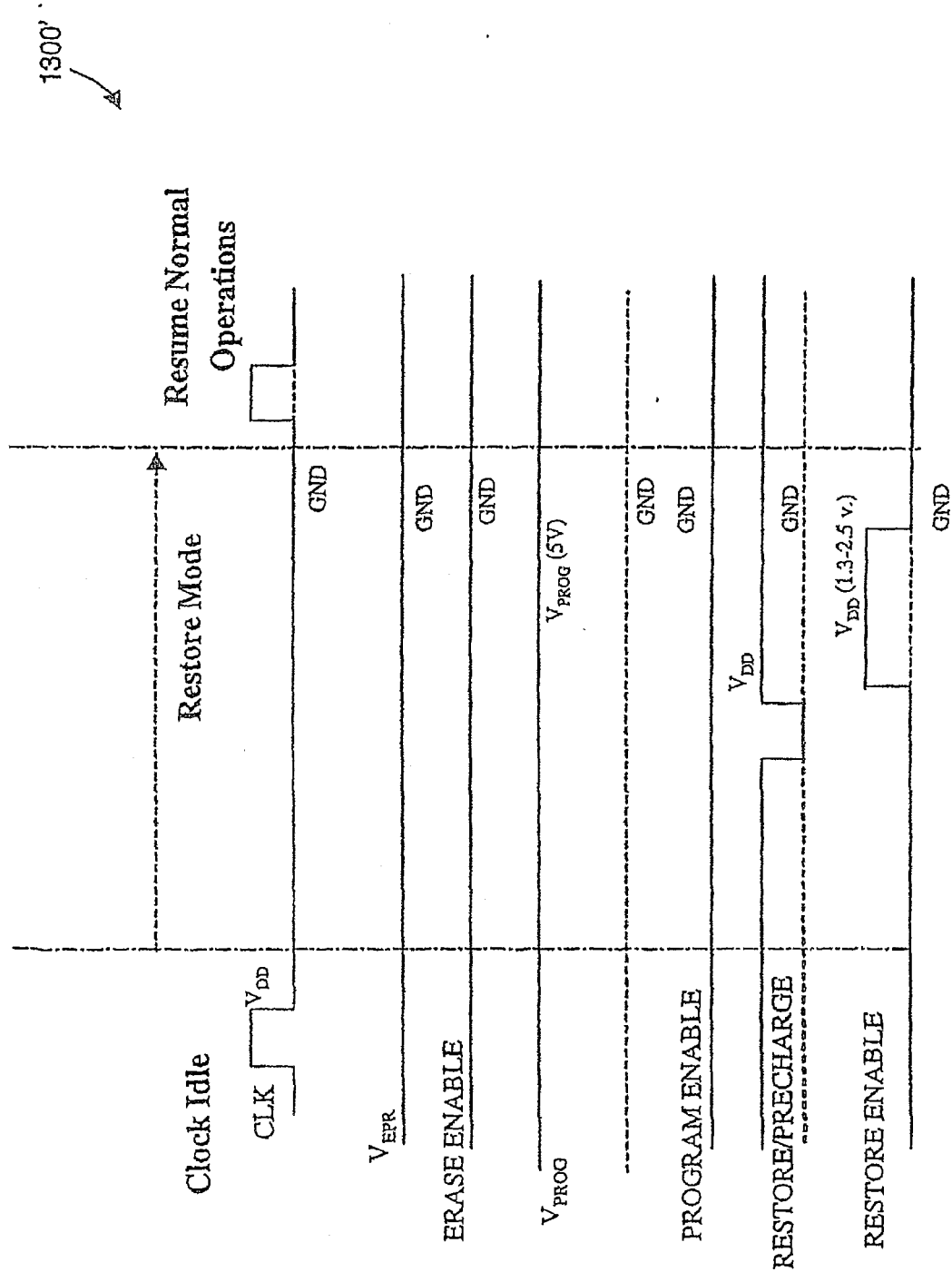


Figure 13C

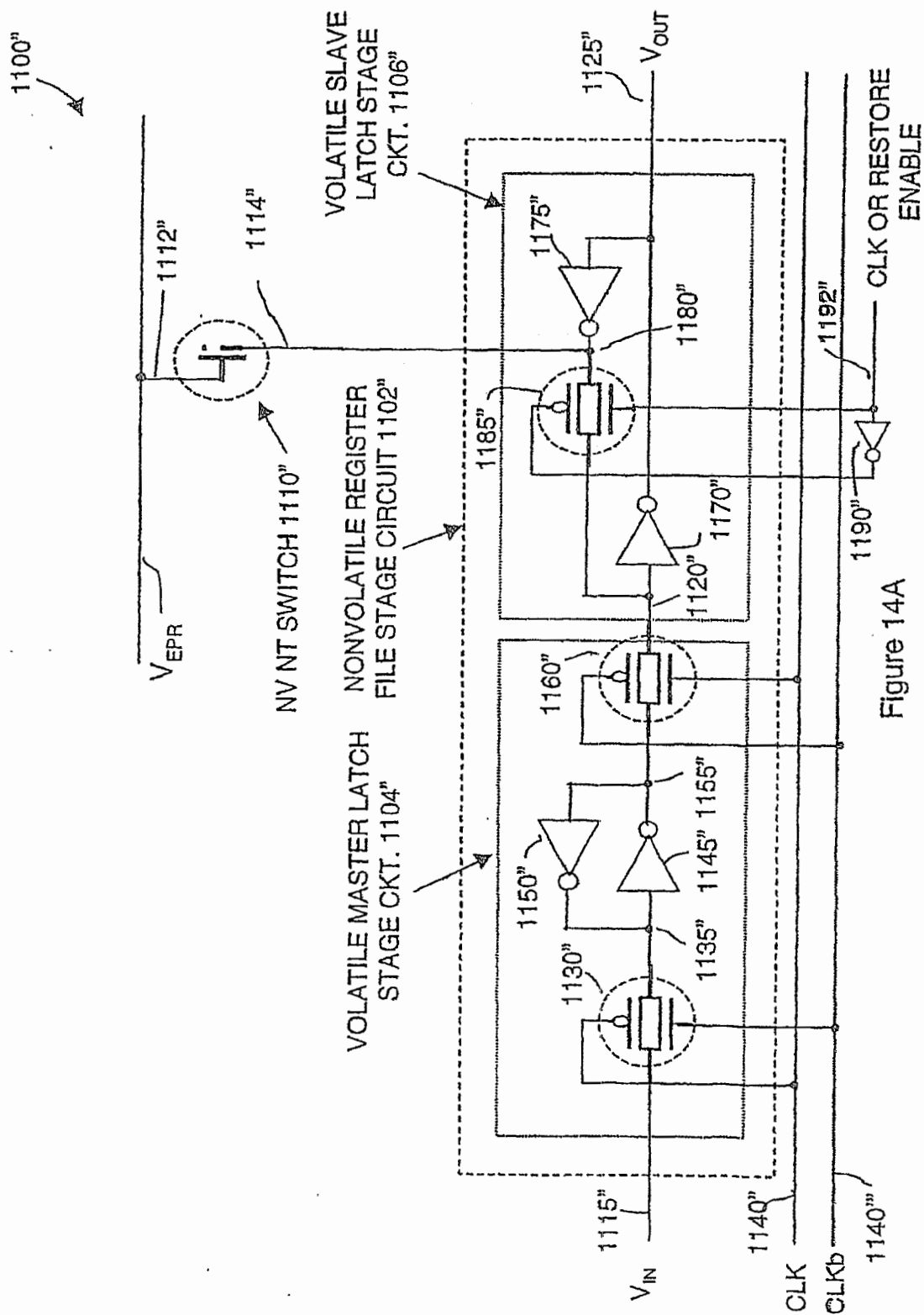


Figure 14A

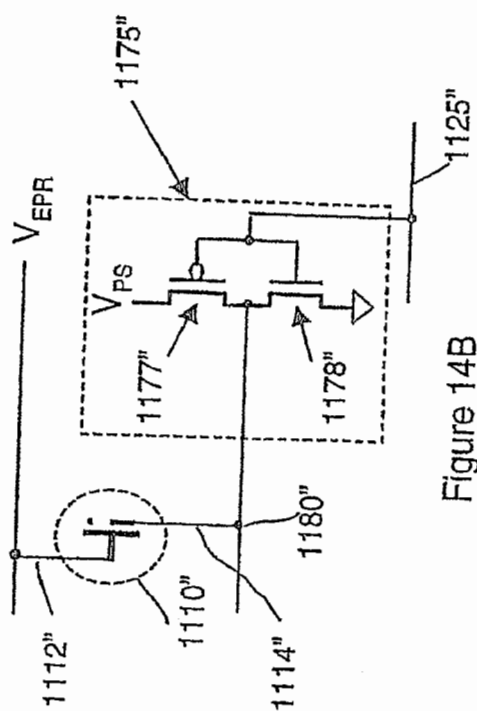


Figure 14B

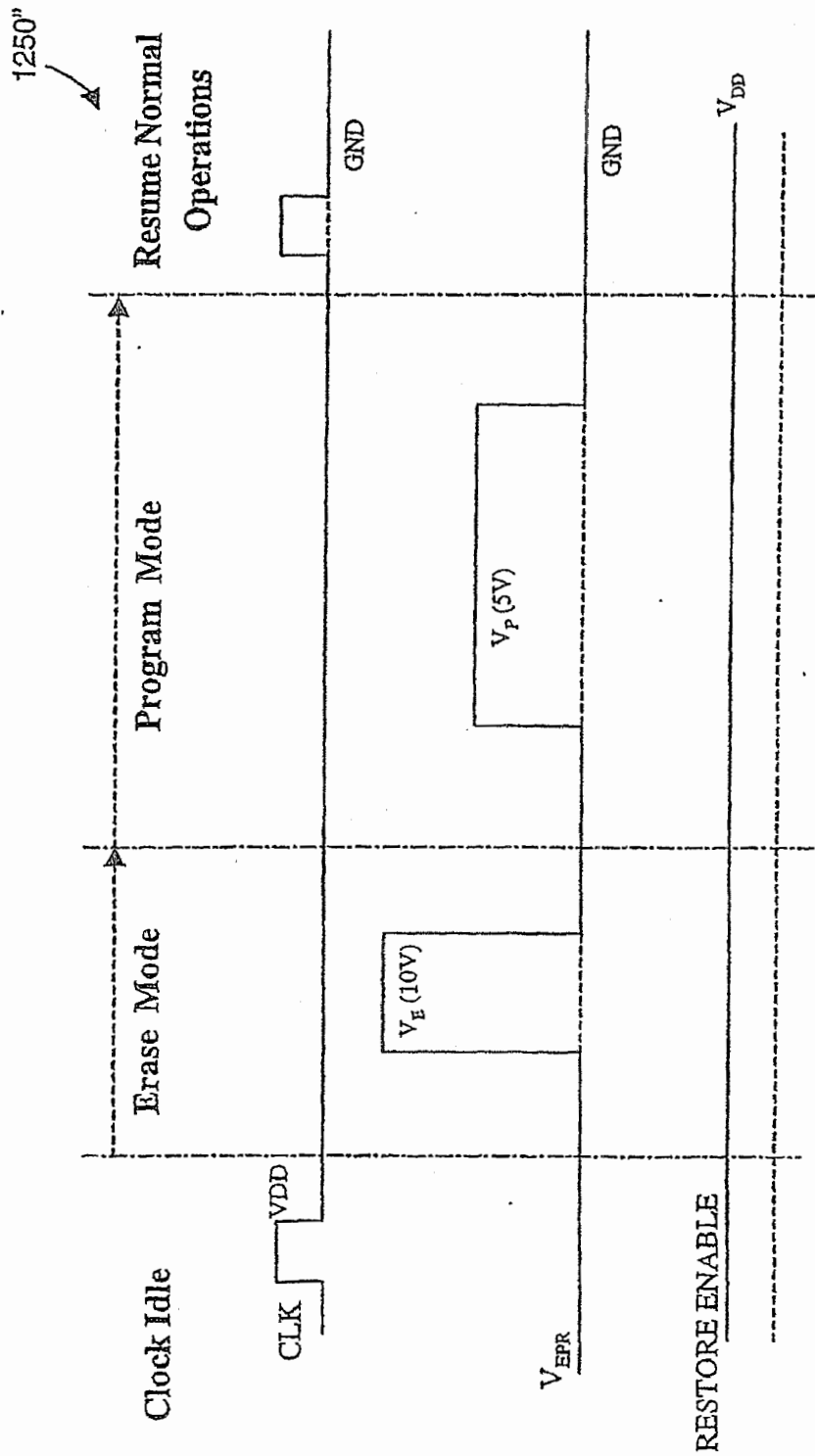


Figure 14C

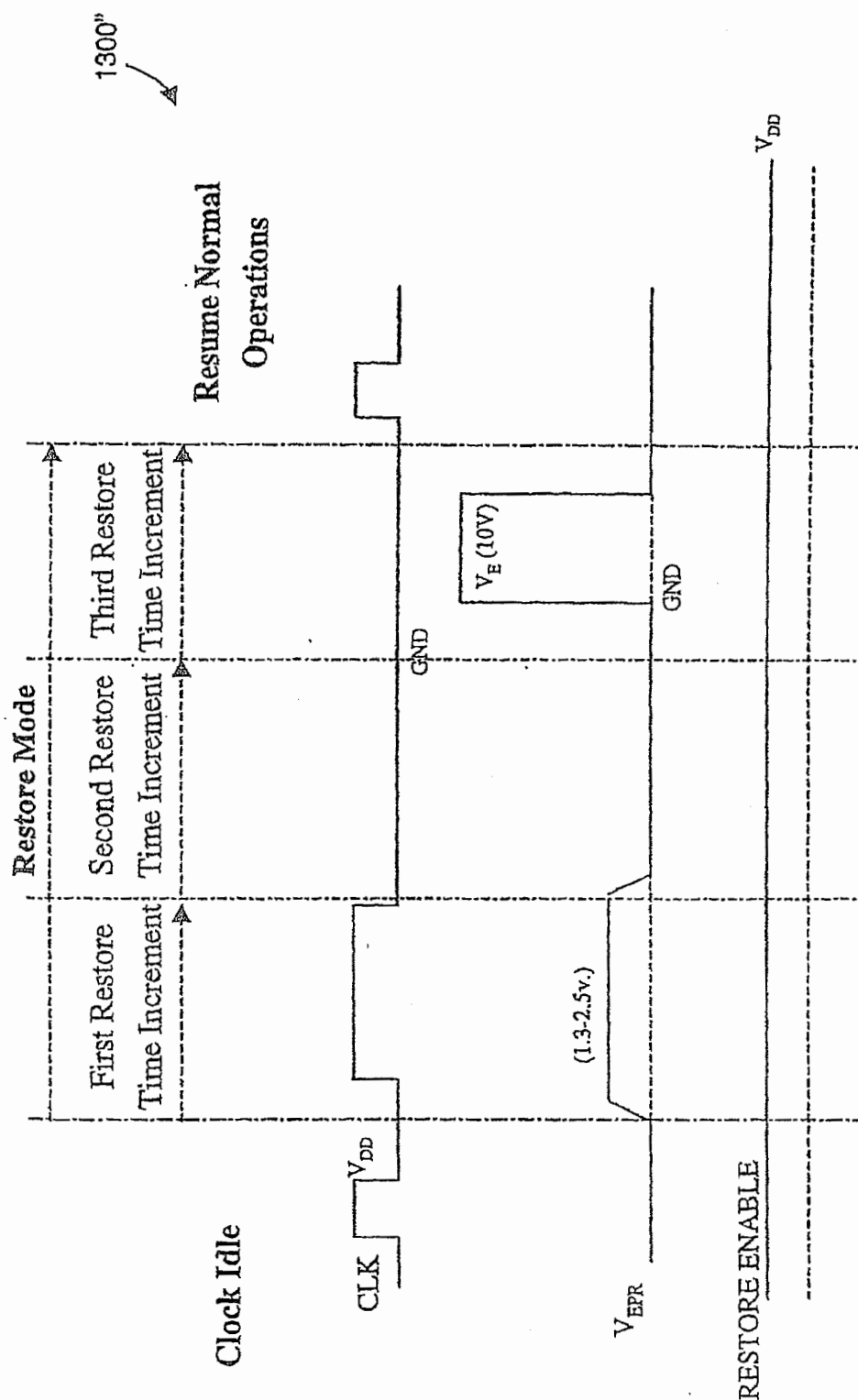


Figure 14D

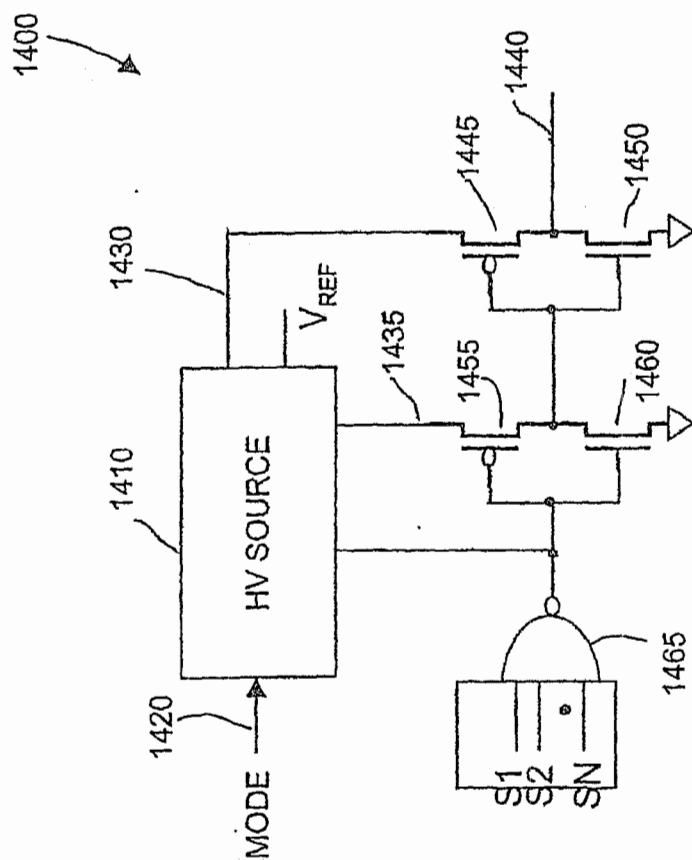
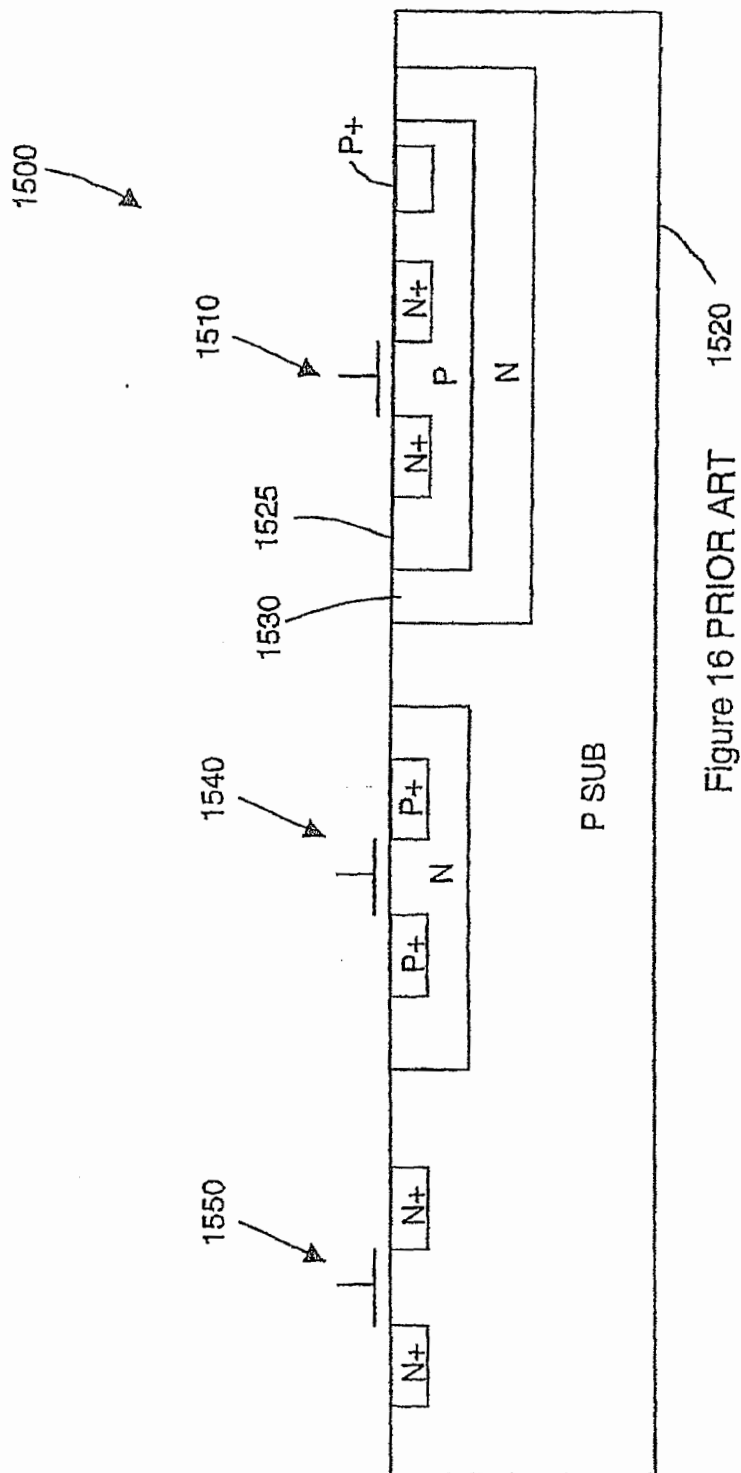


Figure 15 PRIOR ART



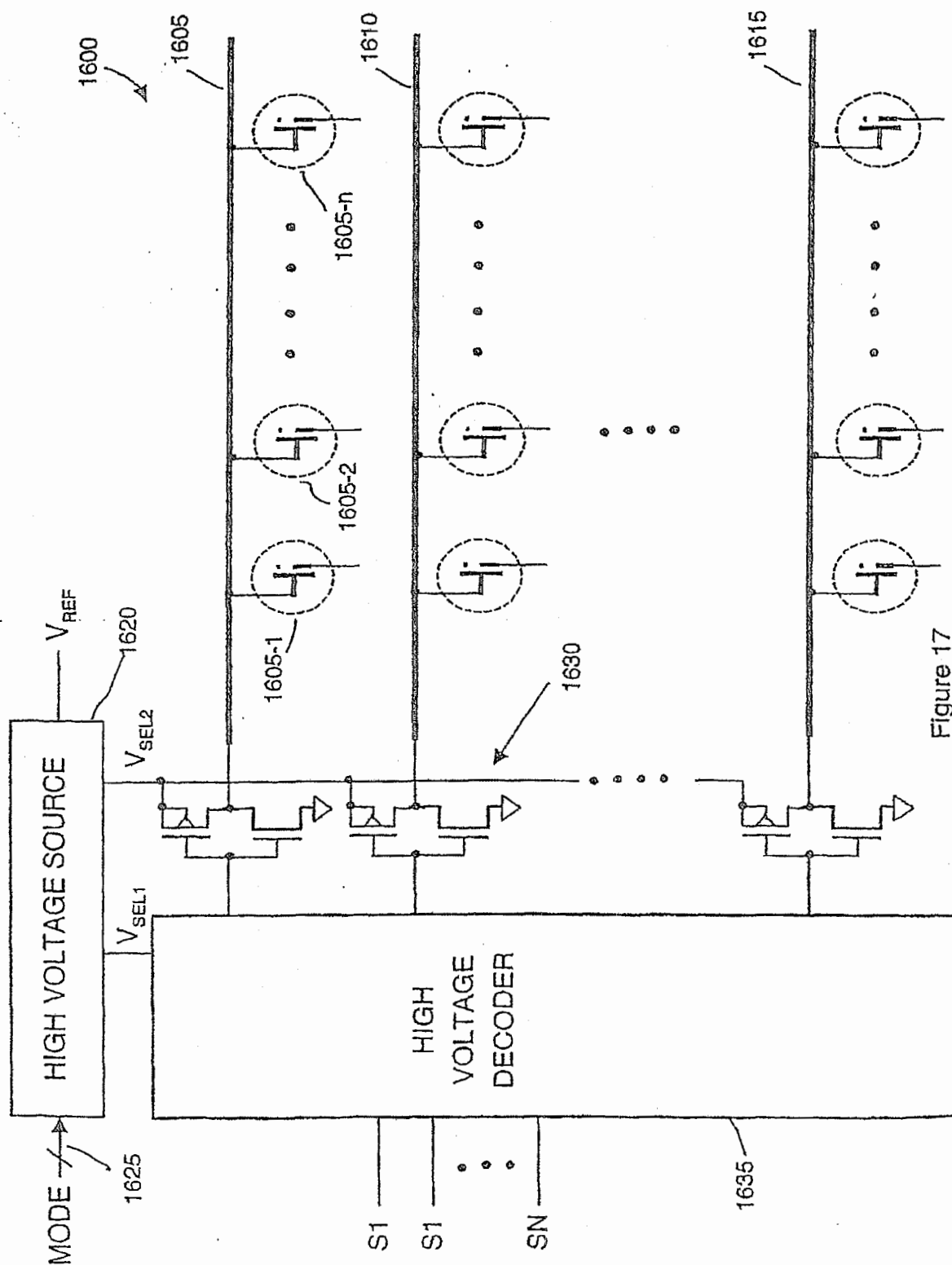


Figure 17