CLAIMS:

1. A method of fabricating an integrated device, the method comprising:
receiving a substrate with a patterned mask, wherein the patterned mask includes non-planar mask features formed in the patterned mask itself; wherein the mask comprises multiple masking material layers, including a first mask material layer disposed above the substrate and under a second mask material layer, wherein the second mask material layer is of different composition than the first mask material layer;
etching a pattern in at least a portion of one or more layers, wherein the etched pattern includes non-planar substrate features formed in the substrate itself;
backfilling the etched pattern with a sacrificial material, wherein the sacrificial material has the same composition as the first mask layer;
removing at least a top portion of the mask with the scarification material present; and
removing the sacrificial material selectively to the non-planar substrate features of the patterned one or more layers.

2. The method of claim 1, wherein:
etching the pattern in one or more layers further comprises etching a layer of the substrate disposed below the patterned mask;
backfilling the etched pattern further comprises:
filling the pattern in the mask with the sacrificial material completely covering the etched substrate layer; and
planarizing the sacrificial material over a top surface of the mask;
removing the top portion of the mask further comprises:
etching through the entire thickness of the sacrificial material disposed over the top surface of the mask; and
etching through only a partial thickness of the mask; and
removing a remainder of the sacrificial material also removes remaining mask material.

3. The method of claim 1, wherein:
etching the pattern in one or more layers further comprises etching a layer of the substrate disposed below the mask;
backfilling the etched pattern further comprises filling the pattern in the mask with the sacrificial material completely covering the etched substrate layer;

removing the top portion of the mask further comprises etching through at least the second mask material layer; and
removing a remainder of the sacrificial material also removes the first mask material layer.

4. The method of claim 1, wherein:
etching the pattern in one or more layers further comprises etching a layer of the substrate disposed below the mask;
backfilling the etched pattern further comprises filling the pattern in the mask with the sacrificial material completely covering the etched substrate layer;
removing the top portion of the mask further comprises etching through at least the second mask material layer; and
removing a remainder of the sacrificial material also removes the first mask material layer.

5. The method of claim 1, wherein:
etching the pattern in one or more layers further comprises etching a layer of the substrate disposed below the mask, wherein the etched substrate layer has the same composition as the second mask material layer;
backfilling the etched pattern further comprises filling the pattern in the mask with the sacrificial material completely covering the etched substrate layer;
removing the top portion of the mask further comprises etching through at least the second mask material layer; and
removing a remainder of the sacrificial material also removes the first mask material layer.

6. The method of claim 1, wherein:
the mask comprises multiple masking material layers, including one or more photo-definable mask material layers disposed over one or more non-photo-definable hard mask material layers;
etching the pattern in one or more layers further comprises:
etching through the one or more hard mask material layers; and
etching a layer of the substrate disposed below the patterned mask;
backfilling the etched pattern further comprises filling the pattern in the mask with the sacrificial material to completely cover the etched substrate layer; and
removing the top portion of the mask further comprises etching through at least one of the hard mask material layers.

7. A method of fabricating an integrated microelectronic device, the method comprising:
receiving a substrate with a mask having multiple masking material layers, the mask including one or more patterned photo-definable mask material layers and a plurality of unpatterned non-photo-definable hard mask material layers, the plurality or hard mask layers disposed above the substrate and below the one or more patterned photo-definable mask material layers further including a first hard mask material layer disposed above the substrate and below a second hard mask material layer; wherein the second mask material layer is of different composition than the first mask material layer;
patterning the hard mask material layers by etching through the plurality of hard mask material layers to form non-planar mask features; and
patterning the substrate by etching at least a portion of a substrate layer disposed below the first hard mask material layer to form non-planar substrate features;
backfilling the etched pattern with a sacrificial material completely covering the etched substrate layer, wherein the sacrificial material has the same composition as the first mask layer;
etching through the second hard mask material layer while the sacrificial material is present, the etching terminated on the first hard mask material layer; and
concurrently removing a remainder of the sacrificial material and the first hard mask material layer selectively relative to the substrate layer.

8. The method of claim 7, further comprising:
forming a plurality of transistor gate electrodes on the substrate;
depositing the substrate layer over the gate electrodes; and
wherein patterning the substrate further comprises forming a gate contact opening in the substrate layer over at least one of the gate electrodes by etching through the substrate layer to expose a top surface of the gate electrode.

9. The method of claim 7, wherein:
backfilling the etched pattern with the sacrificial material further comprises planarizing the sacrificial material over a top surface of the mask; and
the method further comprises
etching through the entire thickness of the sacrificial material disposed over the top surface of the mask.

10. The method of claim 7, wherein:
backfilling the etched pattern with the sacrificial material further comprises applying a carbon-based material with a spin-on process; and
etching through the second hard mask material layer comprises etching the carbon-based material at a rate at least equal to etch rate of the second hard mask material layer.

11. The method of claim 7, wherein:
backfilling the etched pattern with the sacrificial material further comprises applying the sacrificial material with a spin-on process.

12. The method of claim 7, wherein:
the substrate layer is a silicon-containing dielectric material;
the first hard mask material layer is a carbon-based material deposited on the substrate layer, the carbon-based material having more than 80 wt % carbon;
the second hard mask material layer is a silicon-containing dielectric material and is deposited on the first hard mask material layer; and
backfilling the etched pattern with the sacrificial material further comprises applying the carbon-based material over the etched mask materials with a spin-on process.

13. The method of claim 7, wherein:
the substrate layer is SiC;
the first hard mask material layer is a carbon-based material deposited on the substrate layer, the carbon-based material having more than 80 wt % carbon;
the second hard mask material layer is a silicon-containing dielectric material and is deposited on the first hard mask material layer; and
backfilling the etched pattern with the sacrificial material further comprises applying the carbon-based material over the etched mask materials with a spin-on process.

14. A microelectronic device structure, comprising:
a patterned substrate layer having patterned non-planar substrate features formed in the substrate layer itself;
a patterned mask disposed over the patterned substrate layer, the mask including a first hard mask material layer of a first composition that is patterned with non-planar mask features that

are formed in the first patterned mask itself and aligned to the non-planar substrate features; and

a sacrificial material disposed over the non-planar substrate features and backfilling the non-planar mask features, wherein the sacrificial material and the first hard mask material are of the same carbon-based non-photo-definable material.

15. The device structure of claim 14, wherein the patterned substrate layer comprises one or more gate contact openings passing through the substrate layer and exposing a top surface of a transistor gate electrode.

16. The device structure of claim 14, further comprising a second hard mask material layer of a second composition disposed over the first hard mask material layer, wherein the second hard mask material layer is also patterned with the non-planar mask features.

17. The device structure of claim 14, further comprising a second hard mask material layer of a second composition disposed over the first hard mask material layer, wherein the second hard mask material layer is also patterned with the non-planar mask features; and
wherein the patterned substrate layer and the second hard mask material are both silicon-containing dielectric materials.

18. The device structure of claim 14, further comprising a second hard mask material layer of a second composition disposed over the first hard mask material layer, wherein the second hard mask material layer is also patterned with the non-planar mask features; and
wherein the sacrificial material has a top surface planarized over the second hard mask material.

19. The device structure of claim 14, wherein the sacrificial material is recessed within the non-planar mask features, with a top surface of the sacrificial material recessed below a top surface of the first hard mask material.

20. The device structure of claim 14, wherein:
the first hard mask layer is carbon-based material having more than 80 wt % carbon and has a thickness of 100-200 nm;

the patterned substrate layer comprises a silicon-containing dielectric material; and the non-planar substrate features have a critical dimension of 20-50 nm.