

ABSTRACT

A semiconductor device includes a substrate including an active pattern, a gate electrode crossing the active pattern in a plan view, and a ferroelectric pattern interposed between the active pattern and the gate electrode. The gate electrode includes a work function metal pattern disposed on the ferroelectric pattern, and an electrode pattern filling a recess formed in an upper portion of the work function metal pattern. A top surface of a topmost portion of the ferroelectric pattern is lower than a bottom surface of the recess.

FIG. 2A