

"SPEED CONTROL DEVICE FOR A STEPPING MOTOR"

This invention relates to speed control devices for stepping motors, and in particular, although not so restricted to closed loop speed control devices for stepping motors used to drive print
5 heads of printers.

It is known to use open loop driving methods for stepping motors wherein no detector is provided for detecting the position or rate of rotation of the rotor of the stepping motor. The "phase change" timing (as used herein, the term "phase change" refers to a change
10 in the coil or coils of the stepping motor to which driving current is applied to effect driving) required for acceleration of the motor from a rest position, deceleration of the motor from a moving state or constant speed operation, is determined in advance by calculation from a control curve experimentally determined and
15 stored in a memory. Thus, by way of example, where a microprocessor or micro-computer controlled circuit is provided for driving the stepping motor, data for speed control is stored in a ROM. At the time that the driving of the stepping motor is to start, a first predetermined stored time period is read from the memory and at
20 the time that the first stored time period comes to an end, phase change (driving) of the motor is performed and, simultaneously, the next time period is read from the memory. This procedure is followed repetitively with the interval between successive phase changes following the program of stored time periods. In this
25 way, the motor speed is raised to a constant speed.

A driving force f_{sT} required to rotate a stepping motor for one step may be defined as follows:

$$f_{sT} = m \frac{d^2 x}{d(t_{sT})^2} + f_u \quad \dots (1)$$

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where x represents the amount of rotation, m is the mass of the load, t_{sT} is the time necessary to rotate the motor for the amount x , and f_u is the kinetic friction force of the load.

Integrating equation (1) above, the following equation is
10 obtained:

$$f_{sT} = \frac{2mx}{(t_{sT})^2} + f_u \quad \dots (2)$$

During a constant speed period, the time period of the phase
15 change required for constant speed rotation is set. Each time that the time period comes to an end, the phase is changed. The above action is repeated to drive the motor at a constant speed.

During deceleration, as noted above, the calculated time period between phase changes is stored in memory. As the motor enters
20 the deceleration condition, the first calculated time period is read out of the memory. At the end of that first time period, phase change is effected and the next time period is read out from the memory. This procedure is repeated until the motor slows and finally comes to rest.

25 In such open loop control, where the motor is to be advanced

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only a slight incremental angle, half of a predetermined number of steps or phase changes are used for acceleration control and the remaining steps are used for deceleration control.

Accordingly, the known open loop stepping motor driving methods are characterised by calculated intervals of phase change based on anticipated acceleration and deceleration characteristics of the stepping motor. However, this approach has certain disadvantages. First, vibration during acceleration or deceleration caused by variations in the power supply or variations of the load on the stepping motor is not prevented. Figure 1 illustrates this vibration, wherein the ordinate represents the step distance (incremental advance) of the stepping motor while the abscissa represents elapsed time. Times T_a to T_{a+9} each represent one of the predetermined time periods calculated in advance for acceleration or deceleration control and stored in the memory.

Another disadvantage of the known stepping motor driving method is that the speed of the stepping motor cannot respond to driving pulses of the predetermined time period when the driving system of the stepping motor is locked for a period of time. This results from the fact that the interval between phase changes (driving) of the stepping motor is fixed by the pre-calculated time periods and does not take into account intervals where the driving system of the stepping motor is locked.

In U.S. Patent Specification No. 3 863 118, a closed-loop speed control device for a stepping motor is disclosed wherein,

after initial driving by an external pulse, the motor is driven by feedback pulses from a transducer connected to the output of the stepping motor, the transducer being in the form of an optical position detecting device. An adjustable time delay
5 is provided in the feedback loop for adjusting the effective switching angle or phase change time interval, the interval being in turn controlled by a comparator, which compares an external timing signal with the feedback signal.

The present invention seeks to provide a speed control device
10 for a stepping motor for detecting and storing the time intervals between the phase changes during acceleration and using the same time intervals in reverse order to control phase changes during deceleration. The application of the phase
change signal ^{may be controlled} in response to the later of the end of a predetermined
15 time period and a timing pulse representative of an incremental advance of the stepping motor, whereby the aforementioned disadvantages are overcome. Preferably, by providing a driving circuit for the stepping motor having a diode for checking inverse current inserted between an excitation coil and a current switching circuit
20 provided for controlling the supply of current to the excitation coil of each phase, where said drive circuit includes a spike-suppressor circuit, an improved speed control device for a stepping motor is achieved.

According to the present invention there is
25 provided a speed control device for a stepping motor comprising:

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first detector means for producing timing pulses representative of the incremental advance of the stepping motor in a first direction of traverse; motor driving means for advancing the stepping motor; speed control means periodically actuating
5 said motor driving means at least in part in response to said timing pulses during acceleration of said stepping motor, said speed control means including memory means for storing the time intervals between respective actuations of said motor driving means during acceleration of said stepping motor, said speed
10 control means being adapted to actuate said motor driving means during deceleration of said stepping motor at intervals which are a function of the stored acceleration intervals in said memory means applied in reverse order; and second detector means for producing timing pulses representative of the incre-
15 mental advance of said stepping motor in a direction of traverse opposite to the first direction, said speed control means being adapted to detect the direction of traverse and periodically to actuate said motor driving means at least in response to the timing pulses from the one of said detector means associated
20 with the direction of traverse of said stepping motor.

Preferably said speed control means is adapted so that the intervals of actuation of said motor driving means during deceleration bear a fixed functional relationship to the stored acceleration intervals. Said speed control means may be adapted
25 so that the intervals of actuation of said motor driving means

during deceleration are substantially equal to the stored acceleration intervals.

Alternatively in the case where said stepping motor is to be incrementally advanced over a short distance without a constant speed period, said speed control means is adapted periodically to actuate said motor driving means in response to said timing pulses during acceleration of said stepping motor after an initial actuation of said motor driving means. Said short distance of incremental advance of said stepping motor may be represented by an even number of timing pulses, said speed control means being adapted to provide a number of actuations to said motor driving means including said first actuation equal $\lceil \frac{t}{2} \rceil$ (total number of timing pulses in desired incremental advance of stepping motor) $\lceil \frac{t}{2} \rceil + 1$ during acceleration, and being further adapted during deceleration to actuate said motor driving means at intervals which are respective functions of the intervals between said first actuation and a second actuation and between successive actuations except for the last actuation during acceleration, applied in reverse order, so that the number of actuations during deceleration is equal to $\lceil \frac{t}{2} \rceil$ (total number of timing pulses in desired incremental advance of stepping motor) $\lceil \frac{t}{2} \rceil - 1$.

Said speed control means preferably includes pulse generator means for producing periodic pulses; and deceleration counter means coupled to said memory means for setting by the stored interval data to a value representative of the next interval

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between motor driving means actuation during deceleration and coupled to said pulse generator means for counting down thereby, said speed control means being adapted so that the next actuation of said motor driving means during deceleration is in response to the counting down to a predetermined level of said deceleration counter means.

The speed control device may be in combination with a stepping motor which includes at least one pair of coils, each coil of said pair having a first end commonly connected to the first end of the other coil of the pair and a second end, a change in the coil being energized effecting a phase change to advance said stepping motor, said motor driving means including current switching circuit means respectively coupled to the second end of each pair of coils for controlling the supply of current to said coils, spike-suppressor circuit means coupled between said first and second ends of said pair of coils, and a diode connected intermediate the second end of each coil of said pair of coils and the respective current switching circuit means for stopping inverse current.

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Figure 1 is a waveform illustrating the vibration of a stepping motor driven by a conventional driving method, the ordinate representing step distance and the abscissa representing elapsed time;

5 Figure 2 is a fragmentary perspective view of a dot head carrier driving mechanism of a dot printer having a stepping motor driven by a speed control device according to the present invention;

10 Figure 3 is a timing chart illustrating operation of the dot head carrier driving mechanism of Figure 2;

Figures 4 and 5 are timing charts illustrating two embodiments of methods of driving the dot head carrier driving mechanism of Figure 2 along incremental shorter distances than in Figure 3;

15 Figure 6 is a block diagram of a speed control device according to the present invention;

Figure 7 is a circuit diagram of the speed control device of Figure 6; and

20 Figure 8 depicts waveforms at various points in the circuit of Figure 7.

Referring now to Figure 2, a dot head carrier driving mechanism for a dot printer comprises a stepping motor 1 having a timing disc 2 mounted on an output shaft 1a of the stepping motor. The timing disc 2 is provided with a plurality of radially extending slits 2a therethrough, one such slit generally being

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provided for each "step" required for one revolution of the stepping motor 1. The distance between each slit is determined by dividing the timing disc into equal parts, corresponding to the number of steps necessary for one revolution of the stepping motor 1. The respective slits are detected by an optical-type timing detector 3 of conventional construction, generally consisting of a light source, such as a light emitting diode, positioned on one side of the timing disc and a light sensitive device such as a photodiode, on the opposite side of the timing disc. The detector 3 is mounted on a substrate or base 4. A plurality of mounting holes are provided on the base so that it may be mounted in a plurality of positions displaced in the direction represented by arrow A. A driving gear 5a is mounted on the shaft 1a and is in driving engagement with a driven gear 5b. The driven gear 5b is coupled for rotation with a belt-driving gear 5c which supports one end of and drives a timing belt 6. The other end of the timing belt 6 is supported on a freely rotatable gear 5d. A dot head carrier 7 is coupled to the timing belt 6 for lateral displacement in response to the rotation of the stepping motor 1. A dot head 8 usable for printing is mounted on the dot head carrier for displacement thereby.

In the arrangement of Figure 2, it is possible to detect more precisely the position of the dot head carrier 7 during the reciprocal displacement thereof, by providing two detectors 3, either associated with the same timing disc 2, a different group

of slits on the timing disc 2 or a separate timing disc.
This permits separate control of the displacement of the dot
head carrier in each direction of its displacement, either by
alternative control of a common speed control device according
5 to the present invention (see Figure 6) or by provision of separate
speed control devices. The need for two detectors 3 arises from
the fact that there is a difference in the most suitable phase
change timing between the two directions of reciprocal travel of
the dot head carrier caused by various factors. Accordingly,
10 ^{are provided; this is} two such detectors ^{advantageous} particularly where
the driving frequency of the stepping motor is high.

Figure 3 is a timing chart for a speed control device
according to the present invention as particularly adapted to
the dot head carrier driving mechanism of Figure 2. The left-
15 most region of Figure 3 represents a period 9 at which the
stepping motor is at rest. Reference numeral 10 represents the
drive starting time at which the stepping motor is actuated for
the first time. Reference numeral 11 refers to a period of
acceleration, reference numeral 12 refers to a period of constant
20 speed drive and reference numeral 13 refers to a period of
deceleration, all of these periods being under the control of
the speed control device as more particularly described below.

The stepping motor 1 is of the type which, when at
rest, is excited with a certain phase, a selected one or more
25 of the coils thereof being energised. To actuate the stepping

motor to commence displacement, this phase is changed, a different coil or coils is energised, each change being represented by an arrow head in waveform b of Figure 3 which represent phase change timing. At the starting time 10, the first actuation of the

5 stepping motor 1 (phase change) is effected and the stepping motor 1 begins to rotate. At the same time as the phase is changed, a timer, as will be more particularly described below, is set to be actuated for measuring a timing pulse interval t_c . The interval t_c is the interval between actuation or phase changes during the constant

10 speed control period 12. Waveform a of Figure 3 shows the timing pulses produced by the detector 3. If the first timing pulse t_1 is not produced during the time t_c as measured from starting time 10, phase change and therefore the further actuation of the stepping motor 1, is effected upon the output of the timing pulse T_1 . In other

15 words, during the acceleration period 11, the interval between phase changes is determined by the later of the period t_c and the occurrence of the next timing pulse. Simultaneous with each phase change, the timer is reset to measure, once again, the time period t_c . The above procedure is repeated until the motor enters

20 the condition where timing pulse T_n is produced during the pre-determined period t_c , at this stage, the constant speed control period 12 is reached and phase change is effected at the end of each period t_c , since the timing pulse occurs prior to the end of the period.

During the acceleration period 11, the respective time

25 intervals $t_1, t_2, \dots, t_{n-1}$ between the starting time 10 and the

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first timing pulse T_1 and between said first timing pulse and successive timing pulses until timing pulse T_{n-1} , respectively, are stored in a memory as more particularly described below.

These time intervals may be referred to as time t_m where $m = 1, 2, \dots, n-1$.

As noted above, in the constant speed control period 12, it is usual that the timing pulse is produced during the time period t_c , so that the motor phase change is effected at the end of the time period t_c , the timer being reset at that time. However, it is possible that the timing pulse is not produced during the period t_c because motor speed has decreased due to a rapid increase in motor load. In this case, phase change is synchronised with the output of the timing pulse and the timer is reset at this later time, as is the case during the acceleration period. During the constant speed control period 12, the time interval between timing pulses is not stored in the memory, so that constant speed control for stepping motor 1 can be achieved by repeating the above-mentioned process.

When the number of steps (generally timing pulses) from the starting time 10 reaches value $L-(n-1)$, where L equals the predetermined total number of steps required for driving the stepping motor over the prescribed distance, the stepping motor 1 enters the deceleration period 13. In the deceleration period, the ideal brake force f_{sp} required for one step of the stepping motor 1 in the carriage driving mechanism of Figure 2 may be

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defined as follows:

$$f_{sp} = m \frac{d^2 x}{d(t_{sp})^2} - f_u \quad \dots (3)$$

5 where m equals the mass of the load, in this case of the carriage driving mechanism, x equals the distance that the motor is rotated in one step during deceleration, t_{sp} equals the time required to decelerate over the distance x, and f_u is the kinetic friction force on the load, in this case the carriage driving mechanism.

10 When equation (3) is integrated, the time t_{sp} may be expressed as follows:

$$t_{sp} = \sqrt{\frac{2mx}{f_u + f_{sp}}} \quad \dots (4)$$

15 If factors other than kinetic friction force are ignored, the ideal braking condition is obtained when f_{st} = f_{sp}. From equations (2) and (4), the following relationship between t_{sp} and, t_{st} is obtained.

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$$t_{sp} = t_{st} \sqrt{\frac{mx}{mx + (t_{st})^2 \cdot f_u}} \quad \dots (5)$$

Accordingly, it has been found that there is a definite functional relationship, as indicated by equation (5), between the time t_{st} necessary for one step rotation of the motor in the acceleration
25 period and the time t_{sp} necessary for one step rotation of the

motor in the course of the desired speed control during deceleration. If the kinetic friction force $\underline{f_u}$ is so small as to be disregarable, it is possible to consider t_{sp} to be approximately equal to t_{ST} .

Taking the foregoing into consideration, at the time that

5 the last phase change is accomplished in the constant speed control period, the timer resets the actuator for the time period $F(t_{n-1})$, expressed as a definite function of the last time interval t_{n-1} of the timing pulses detected and stored during the acceleration period. At the expiration of this stored time period $F(t_{n-1})$, the

10 phase change is effected and the timer is reset to the period $F(t_{n-2})$, also expressed as a function of the time interval t_{n-2} between timing pulses T_{n-3} and T_{n-2} of the acceleration period 11 as stored in the memory. Accordingly, during the deceleration period, phase change is effected at intervals which are a function

15 of the intervals between the starting time 10 and the first timing pulse T_1 and between the successive timing pulses $T_1, T_2, \dots, T_{n-1}$, taken in inverse order, all said time periods having been stored in the memory during the acceleration period 11. This process is repeated until the last phase change is carried out at the end

20 of the time period $F(t_1)$ which is a function of the time period t_1 , bringing the deceleration period to an end. By virtue of the above-described method, the dot head 8 of Figure 2 can be smoothly driven through both acceleration and deceleration without being influenced by variations in the supply voltage or variations in the load.

25 Moreover, extremely good print quality can be realised, since the

print timing of the dot head is synchronised with the rise of the timing pulses and with the timing obtained by dividing the time interval between the timing pulses during constant speed drive into periods of equal length.

5 When dot head carrier 7 is incrementally traversed over only a short distance, it is necessary to drive the stepping motor in accordance with one of the timing charts illustrated in Figures 4 and 5, wherein there is no period of constant speed. This results from the fact that the stepping motor would be
10 advanced over too great a distance if the constant speed period is incorporated in the cycle.

 Figure 4 illustrates a speed control based on the actuating of the stepping motor in an even-numbered number of steps, in this example, six steps. Waveform c depicts the timing pulses
15 while waveform d depicts the phase change signal as represented by arrowheads. When the phase is changed at a drive starting time, as indicated by reference numeral 14, the stepping motor enters an acceleration period 15. The time period t_{c1} between the starting time 14 and the first timing pulse is detected and stored
20 in a memory. Phase change is effected by the first timing pulse and the intervals between said first timing pulse and the second timing pulse t_{c2} is stored in the memory when phase change is next effected by the second timing pulse. The foregoing process is repeated until the $\lfloor (\text{total number of steps})/2 \rfloor + 1$ 'th (fourth,
25 for example in the embodiment of Figure 4) phase change is effected.

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This marks the end of the acceleration period 15 and the beginning of a deceleration period 16. In the deceleration period 16, a number of phase changes equal to $\lfloor (\text{total number of steps}) / 2 \rfloor - 1$ phase changes are effected, in the example of Figure 4, two phase changes. Specifically, a timer would be set at a period which is a function of the time interval before the last time interval, t_{c2} , a time interval designated as $F(t_{c2})$. In other words, the stored time period t_{c2} is utilised to determine the period after which the next phase change is effected, and the time period prior to period t_{c2} , period t_{c1} , is used to determine the period when the last phase change is effected, a period represented by $F(t_{c1})$. In summary, each of the time periods during the acceleration period 15 is stored, except the last period, and each of the stored periods is used in inverse order to determine the period between phase changes in the deceleration period 16 until deceleration is complete.

Figure 5 illustrates the method of speed control utilised where the stepping motor is driven by an odd numbered number of steps. In this embodiment, the number of steps of an acceleration period 18 and a deceleration period 19 are equal. The first phase change is performed at a drive starting time 17, at which time the stepping motor begins to rotate. In the acceleration period, the time interval is between the starting time 17 and the first timing pulse and between successive timing pulses thereafter is detected and stored in a memory. During the deceleration period,

the time intervals thus stored are utilised as the basis of the time period between successive phase changes, in inverse order. By way of example, where seven steps constitute a cycle of rotation necessary for the incremental advance of the stepping motor the desired distance, after the initial phase change at the starting time 17, three further phase changes at intervals of t_{d1} , t_{d2} and t_{d3} are effected. Thereafter, deceleration is effected by the application of three phase changes at intervals defined as $F(t_{d3})$, $F(t_{d2})$ and $F(t_{d1})$. This process is illustrated by the timing signals of waveform e and the phase change signals as represented by arrowheads in waveform f of Figure 5.

In Figure 6, there is shown a speed control device according to the present invention. The stepping motor 1 and the timing disc 2 are shown in conjunction with two optical timing detectors 3 and 3', both coupled to a comparator 30. Each detector 3, 3' produces an output signal when each slit 2a is in registration therewith. The detector 3 is associated with the forward direction of traverse of the dot head carrier 7 while the detector 3' is associated with the reverse or return traverse of said dot head carrier. The comparator 30 distinguishes between the two detectors by counting the timing pulses from the rest position at one end of the traverse, although, in an alternative embodiment, the direction of rotation can be detected by the order of pulse detection dependent upon the position of the respective detectors. A timing pulse signal, in digital form if desired, representative

of the position of the stepping motor, and therefore of the dot head carrier, may be applied to an output terminal 50 by the comparator 30.

Start/stop signals and reset signals may be respectively applied to terminals 22 and 21, either from an external source or from the comparator 30, which can produce such signals in response to counting of the timing pulses. The reset pulse is applied in order to put the various counters into a starting condition simultaneous with the start of the stepping motor 1. The start signal applied to the terminal 22 represents a change in state from "Low" to "High" at the terminal 22. The reset signal at the terminal 21 is applied to counters 33, 40 and 47 to reset these counters to "zero" simultaneous or immediately before the application of the start signal to the terminal 22. The start signal applied to terminal 22 is applied to a differentiation circuit 23 which produces a pulse output responsive to the change from the "Low" to the "High" state. The output of differentiation circuit 23 is applied to an OR gate 60, the output of the OR gate 60 being applied to a pulse distribution circuit 24 which produces a driving signal for the stepping motor 1 which is shown as a four phase stepping motor. Each pulse output from the OR gate 60 causes an output from the pulse distribution circuit 24 to a driving circuit 25, which in turn actuates one phase of driving coils 26 of the stepping motor 1. Each driving signal represents a phase change sufficient to actuate the stepping motor. The operation of

the stepping motor driving circuit 25 is discussed below in connection with Figures 7 and 8, it being sufficient to state here that the current in the respective coils is turned "on" and "off" in response to the driving signal.

5 Because of the actuation of the stepping motor, the timing disc 2 advances so that a timing pulse is generated by the detector 3 which is applied to the comparator 30 as discussed above.

 A pulse generator 31 is adapted to have its pulse output controlled by an output 32 from an AND gate 61. At the starting
10 time, a pulse is generated by the pulse generator 31 and fed to the counter 33 through an AND gate 62, the other input to AND gate 62 being the "High" start signal from the terminal 22.

 The output of the counter 33 is applied to a decoder 34 adapted to produce a "High" output when the count value of the counter 33
15 equals a period t_c as determined by the pulse period of the pulse generator 31. The output of the decoder 34 is applied to a differentiation circuit 35 which serves to produce a pulse when the output from the decoder 34 changes from a "Low" to a "High" state, representative of the passage of the period t_c .

20 A differentiation circuit 36 produces a pulse output coincident with the leading edge of each timing pulse, in other words, when the timing signal changes from a "Low" to a "High" state. The pulse output of the differentiation circuits 35, 36 is applied to an OR gate 63, the output of which is applied to a D-type
25 flip-flop 37 which in turn, produces one pulse when the output

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of both differentiation circuits 35, 36 is fed thereto. The output of the flip-flop 37 is applied to the pulse distribution circuit 24 through the OR gate 60, whereby the stepping motor 1 is stepped in response to the detection of both the passage of the time period t_c and the next timing pulse.

A differentiation circuit 38 produces a pulse output in coincidence with the trailing edge of the output pulse from the flip-flop 37. At this time, if the output from position "12" of the decoder 44 is not "High", i.e., the count value of the counter 40 is not 12, the output pulse from the differentiation circuit 38 is input to the counter 40 for up counting. The "12" output of the decoder 44 is coupled through an inverter and an AND gate 64 to the "UP" terminal of the counter 40, the other input to the AND gate 64 being from the Q output terminal of the flip-flop 37 through the differentiation circuit 38. The output of the differentiation circuit 38, when passed by the AND gate 64, is also applied through a delay circuit 42 to a WRITE terminal of a RAM 43. It should also be noted that this signal is applied through an OR gate 65 as a clock circuit to the counter 40. Also, at this time, the output of a three-state buffer 41 is enabled, so that the output of the counter 33, representing elapsed time for the period between phase changes, is applied through the buffer 41 to a data bus $D_0 - D_7$ of the RAM 43. The period represented by the count of the counter 33 is read into the data bus at an address as determined by the count of the counter 40. After the data is

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written in to the RAM 43, the output of the differentiation circuit 38 is applied through a delay circuit 51 to the clear terminal of the counter 33 to clear the counter for the next cycle.

5 The foregoing describes a sequence during the rotation of the stepping motor 1 by one step. During the acceleration period 11, as discussed in connection with Figure 3, a period t_c passes so as to produce an output from the flip-flop 37 through the differentiation circuit 35, causing the flip-flop 37 to change
10 from a "Low" to a "High" output. However, the second actuation of the flip-flop 37 required to produce a phase change does not occur until the next leading edge of a timing signal is received, at which point the output of the flip-flop 37 changes from "High" to "Low" and the count value of the counter 33 is written in
15 the RAM 43 as described above. The counter 33 is then cleared and the phase change is effected by means of the driving pulse distribution circuit 24. In this manner, during the acceleration period, the count values of the counter 33 between one step change and the next step change are successively stored in the RAM 43.

20 While the circuit of Figure 6 is provided with only 12 steps in the acceleration period, this is merely by way of example in order to simplify the circuit and any number of acceleration steps may be incorporated depending on the characteristics of the stepping motor. Even if full acceleration is achieved earlier,
25 12 steps are memorized in the RAM 43. At the end of the step

change for the twelfth step, the output from position "12" in the decoder 44 becomes "High", applying a signal through the inverter to the AND gate 64 to prevent the application of pulses to the WRITE terminal of the RAM 43 and to the clock input of the counter 40.

After the acceleration period is over, the leading edge of the respective timing pulses, as indicated by the output signal of the differentiation circuit 36, appears earlier than the output pulse of the differentiation circuit 35 representative of the passing of the period t_c . In this case, the step change of the stepping motor 1 is performed at the end of the predetermined period t_c , so that the stepping motor 1 rotates at a constant speed. In the course of such constant speed rotation, if too much load is applied to the stepping motor 1, step change may not occur even if the time period t_c passes. This case is analogous to the acceleration period where the step change does not occur until the leading edge of the next timing pulse appears. This makes it possible for the motor speed to respond to the predetermined time period, albeit after a delay, despite the application of a load to the motor.

The motor enters the deceleration control period when there are twelve steps remaining in the traverse of the step motor. The transition to the deceleration mode is achieved by the "stop" signal at the terminal 22, which may be produced by the comparator 30 as discussed above. Specifically, the signal at the

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terminal 22 is changed from a "High" to a "Low" state. This change causes an output pulse to be produced by a differentiation circuit 39, the signal being applied to the differentiator through an inverter. The pulse output from the differentiation circuit 39 is applied through an OR gate 66 and through a delay circuit 45 to a READ terminal of the RAM 43. At the same time, the address desired is selected by the counter 40 which is coupled to address bus A_0-A_7 of the RAM 43, and the counter 40 is indexed by the application of the output from the OR gate 65 to the clock terminal of the counter 40. The data from the data bus D_0-D_7 at the selected address is stored in the counter 47 which is adapted to count down to zero. This counting is achieved through the output signals of the pulse generator 31 which are applied through an AND gate 67 to the clock terminal of the counter 47. The other input to the AND gate 67 is the "stop" signal at terminal 22, applied through an inverter. The counter 47 counts down the predetermined period until its output equals zero as determined by a decoder 48. When the output of the decoder 48 becomes "Low", a pulse is produced by a differentiation circuit 49, whose output forms another input to the OR gate 60 to produce a phase change through the pulse distribution circuit 24. The output of the differentiation circuit 49 is also applied through the OR gate 66 to effect indexing of the address and the writing of the contents of the next address into the counter 40.

The data in the RAM 43 which is selected counter 40 is again

set in the counter 47, wherein down-count is performed until the count value comes to 0. The contents of the counter 47 are again counted down using the pulse signal output of the pulse generator 31. This cycle produces the successive phase changes characteristic of the deceleration period 13 of Figure 3.

Figure 7 shows the driving circuit 25 for the coils 26 of the stepping motor 1 in detail. Waveforms f, g, h and i in Figure 8 represent the waveforms at the points marked with corresponding letters in the circuit of Figure 7. As is apparent from a consideration of Figure 7, two identical circuits are provided, a first driving phase A and phase B, as defined by the left-most coils in Figure 7, the other driving phase C and phase D as represented by the right-most coils in Figure 7. The two circuits are identical, like elements having the same reference numeral, only primed. A switching circuit 51 selects which of the two motor coils is to be actuated. A spike suppressor circuit 52 is connected across the coils and consists of a pair of diodes 70, 71 and a Zener diode 72. A switching circuit 53 for closed-loop constant current is common to the two phases and is connected to the commonly connected emitters of switching transistors 73 and 74 of the switching circuit 51 for switching phases A and B respectively. A common switching circuit for closed loop constant current may be provided for phases A and B since the two phases are never simultaneously actuated, in other words, current is never applied at the same time both to the coil of phase A and the coil of phase B.

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The switching circuit 53 is controlled by a control circuit 54 insuring a constant current. A diode 55 is interposed between one end of each of the coils defining phases A and B and the associated switching transistors 73, 74 for checking inverse
5 current caused by mutual inductance between the coils. Finally, a flywheel diode 56 is provided between ground and the common connection of the coils of phase A and B.

To supply current to the coil of phase A, as shown by waveform h in Figure. 8, the coil of phase A is not supplied with
10 current until the time t_g has passed. During the time t_g , the energy in the coil of phase B is consumed by the spike-suppressor circuit 52. When the time t_g has passed, current begins to be supplied to the coil of phase A by the switching circuit 53. This current gradually increases. If the current reaches level I_1
15 determined by the switching circuit 53, a transistor 75 of the switching circuit 53 is turned off. As a result, the coil of phase A is cut off from a current source V_M . The energy applied to the coil of phase A is consumed in the transistor 73 of the switching circuit 51, in the coil, and also in the closed circuit
20 of the flywheel diode 56, and gradually decreases. When the energy reaches level I_2 , the transistor 75 is turned "on" again and current applied to the coil of phase A is increased once again. The above-mentioned action repeats in order to control the current of the coil between I_1 and I_2 .

25 When a phase change is to occur, in other words, when the

current is to be cut off from phase A and to be applied to phase B, the spike-suppressor circuit 52 actuates so that the current supplied to the coil of the phase A reduces smoothly as shown in waveform h. The current to the coils of phase B is also constantly controlled
5 between the current values I_1 and I_2 . Further, the current to the coils of phases C and D are also constantly controlled between the current values I_1 and I_2 . During the time t_s , inverse current produced by mutual inductance is prevented from flowing to the coil, as shown in waveform h of Figure 8, by means of the diode 55.
10 Accordingly, there is no fear of destruction of the circuit and it is possible to provide a stable switching circuit for closed-loop constant current.

It is possible to change readily the constant current value by changing the level of waveforms shown in Figure 8 between I_1
15 and I_2 in the control circuit 54. This makes it unnecessary to prepare special motor current sources. Finally, with respect to the energy output of the motor, it is possible to reduce, as small as possible, the vibration generated by excessive input, which is normally a characteristic of stepping motors. It is also possible
20 to reduce as small as possible the heat generated in the coil. This may be realised by the step of making the constant current value variable so that the value most properly assigned in accordance with the rotation speed of the motor is used.

In summary, the speed control device according to the present
25 invention and described above may control the stepping motor, even



where the stepping motor is driven over relatively short incremental distances, defined by only a few steps, at high speed. Vibration of the motor is thus minimized so that extremely good print quality can be realized from a dot printer incorporating a stepping motor and a speed control system according to the present invention. The timing pulses produced may be used to coordinate the printing of characters with the displacement of the dot head carrier. The vibration of the stepping motor usually experienced during acceleration and deceleration can be avoided. Even if too much load is applied to the stepping motor, so that the stepping motor is stopped during a driving period, when the load is removed, the rotor begins to rotate again. This is because the phase is never changed until a timing pulse is produced.

Accordingly, the illustrated embodiment of the present invention overcomes the defects of the prior art. It should be noted that the present invention is applicable, not only to the carrier driving mechanisms of printers, but also to other devices incorporating stepping motors, where it is desirable to drive the stepping motor at high speed without any vibration through use of predetermined steps, for example, magnetic head driving devices.

Attention is directed to the fact that this application describes matter for which protection is sought by Application No. 8423502.



CLAIMS

1. A speed control device for a stepping motor comprising:
first detector means for producing timing pulses representative
of the incremental advance of the stepping motor in a first
direction of traverse; motor driving means for advancing the
stepping motor; speed control means periodically actuating said
5 motor driving means at least in part in response to said timing
pulses during acceleration of said stepping motor, said speed
control means including memory means for storing the time
intervals between respective actuations of said motor driving
10 means during acceleration of said stepping motor, said speed
control means being adapted to actuate said motor driving means
during deceleration of said stepping motor at intervals which
are a function of the stored acceleration intervals in said
memory means applied in reverse order; and second detector means
15 for producing timing pulses representative of the incremental
advance of said stepping motor in a direction of traverse
opposite to the first direction, said speed control means being
adapted to detect the direction of traverse and periodically
to actuate said motor driving means at least in response to
20 the timing pulses from the one of said detector means associated
with the direction of traverse of said stepping motor.
2. A speed control device as claimed in claim 1 in which said
speed control means is adapted so that the intervals of actuation
of said motor driving means during deceleration bear a fixed
25 functional relationship to the stored acceleration intervals.



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3. A speed control device as claimed in claim 2 in which said speed control means is adapted so that the intervals of actuation of said motor driving means during deceleration are substantially equal to the stored acceleration intervals.

5 4. A speed control device as claimed in claim 1 in which in the case where said stepping motor is to be incrementally advanced over a short distance without a constant speed period, said speed control means is adapted periodically to actuate said motor driving means in response to said timing pulses during
10 acceleration of said stepping motor after an initial actuation of said motor driving means.

5. A speed control device as claimed in claim 4 in which said short distance of incremental advance of said stepping motor is represented by an even number of timing pulses, said speed
15 control means being adapted to provide a number of actuations to said motor driving means including said first actuation equal to $\lceil (\text{total number of timing pulses in desired incremental advance of stepping motor}) / 2 \rceil + 1$ during acceleration, and being further adapted during deceleration to actuate said motor driving means
20 at intervals which are respective functions of the intervals between said first actuation and a second actuation and between successive actuations except for the last actuation during acceleration, applied in reverse order, so that the number of actuations during deceleration is equal to $\lceil (\text{total number of timing pulses in desired incremental advance of stepping motor}) / 2 \rceil - 1$.
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6. A speed control device as claimed in claim 4 in which the

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desired incremental advance of said stepping motor is represented by an odd number of timing pulses, said speed control means being adapted so that the number of intervals between actuations of the motor driving means during acceleration equals the number of intervals between actuations during deceleration, said speed control means being adapted so that all of the intervals between actuations of the motor driving means during acceleration are stored including the interval between the first actuation and the first timing pulse.

10 7. A speed control device as claimed in any preceding claim in which each said detector means includes a disc member mounted for rotation by said stepping motor and having circumferentially spaced apertures therethrough, and an optical detector in registration with said apertures for detecting the presence or absence of said aperture as said disc member rotates.

15 8. A speed control device as claimed in any preceding claim in which said speed control means includes measuring means for measuring the passage of a predetermined time period, said speed control means being adapted for periodically actuating said motor driving means during the acceleration of said stepping motor in response to the later of the expiration of said predetermined time period and the application thereto of the next timing pulse, said speed control means being adapted to reset said measuring means upon each actuation of said motor driving means during acceleration.

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9. A speed control device as claimed in any preceding claim
in which said speed control means includes counter means for counting
the timing pulses from initial actuation, said speed control
means being adapted to actuate said motor drive means during
5 deceleration a number of times equal to the number of timing
pulses defining the acceleration period.

10. A speed control device as claimed in claim 9 in which the
traverse of said stepping motor includes an acceleration period,
a period of desired constant speed and a deceleration period,
10 said speed control means being adapted during the period of
constant speed control to actuate said motor driving means in
response to the later of said predetermined time period and
the next timing pulse.

11. A speed control device as claimed in claim 10 in which
15

said speed control means includes comparator
means for counting timing pulses

for determining the initiation of deceleration.

12. A speed control device as claimed in any of claims 9 to
20 11 in which said counter means is an up-down counter for counting
up at least in part in response to timing pulses during the
acceleration period and for counting down at least in part in
response to motor driving means actuation during deceleration,
said up-down counter means being coupled to said memory means
25 for controlling the reading in to said memory means during acceler-
ation and the writing out of said memory means during deceleration.

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13. A speed control device as claimed in claim 12 in which
said speed control means includes pulse generator means for
producing periodic pulses; and deceleration counter means coupled
to said memory means for setting by the stored interval data
5 to a value representative of the next interval between motor
driving means actuation during deceleration and coupled to said
pulse generator means for counting down thereby, said speed
control means being adapted so that the next actuation of said
motor driving means during deceleration is in response to the
10 counting down to a predetermined level of said deceleration
counter means.

14. A speed control device as claimed in claim 13 including
acceleration counter means coupled to said pulse generator means
for being counted up thereby and coupled to said memory means
15 during acceleration for writing into said memory means a value
representative of a count upon the next actuation of said motor
driving means, said speed control means being adapted to reset
said acceleration counter means upon said next actuation of
said motor driving means.

20 15. A speed control device as claimed in claim 14 in which
said measuring means includes said acceleration counter means
and decoder means for detecting a count of said acceleration
counter means representative of said predetermined time period.

25 16. A speed control device as claimed in any preceding claim
in combination with a stepping motor which includes at least
one pair of coils, each coil of said pair having a first end



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commonly connected to the first end of the other coil of the pair and a second end, a change in the coil being energized effecting a phase change to advance said stepping motor, said motor driving means including current switching circuit means
5 respectively coupled to the second end of each pair of coils for controlling the supply of current to said coils, spike-suppressor circuit means coupled between said first and second ends of said pair of coils, and a diode connected intermediate the second end of each coil of said pair of coils and the
10 respective current switching circuit means for stopping inverse current.

17. A speed control device as claimed in claim 16 in which said spike-suppressor circuit means includes a Zener diode coupled at its anode to said commonly-connected first ends of said pair
15 of coils and a pair of diodes connected at their respective cathodes to each other and to the cathode of said Zener diode and each being connected at its respective anode to the second end of one of said coils, said diode for storing inverse current being positioned between said spike-suppressor circuit means
20 and said switching circuit means.

18. A speed control device as claimed in claim 17 including a flywheel diode coupled between ground and said commonly connected first ends of said pair of coils with the cathode thereof coupled to said first ends of the coils.

25 19. A speed control device as claimed in any of claims 16 to 18 including closed-loop constant current means for maintaining



the level of current in a coil actuated by said current switching means between first and second current levels.

20. A speed control device substantially as herein described with reference to and as shown in Figures 6 and 7 of the
- 5 accompanying drawings.