CLAIMS

1. A normally OFF field effect transistor (FET) comprising:

a plurality of contiguous nitride semiconductor layers having a plurality of heterojunctions, a Fermi energy and~~,~~ conduction bands~~; and~~ ;

a source (SRC) and a drain (DRN) overlying a top nitride layer (112) of the plurality of nitride layers and having source and drain access regions respectively comprising regions of at least two of the heterojunctions near the source and drain;

a first gate (G1) between the source (SRC) and drain (DRN); and

a set of nitride layers comprised in the plurality of nitride layers, the set comprising:

a first nitride layer (105) having a first band gap;

a second nitride layer (106) that forms a first heterojunction of the plurality of heterojunctions with the first layer and having a second band gap wider than the first band gap and polarization that generates an electrostatic field (E106) in the second layer having a direction that causes electron drift towards the first heterojunction;

a third nitride layer (108) located on a same side of the first nitride layer as the second nitride layer having polarization that generates an electrostatic field (E108) in a direction opposite to the electric field in the second nitride layer which raises the conduction band at the first heterojunction under the first gate above the Fermi energy;

a fourth nitride layer (109) formed from GaN having band gap greater than the third layer that forms a second heterojunction of the plurality of heterojunctions with the third layer having a two dimensional electron gas (2DEG) (108eG2) in the source and drain access regions but not in a region (108G1) below the first gate; and

a fifth nitride layer (111) formed from InA1GaN having band gap greater than the fourth nitride layer and polarization that generates an electrostatic field in the fifth nitride layer that causes electron drift towards the fourth layer and wherein the fourth nitride layer forms a third heterojunction (109G2, 109G3) with the fifth nitride layer or with a nitride layer intermediate the fourth and fifth nitride layers that has a 2DEG (109eG2, 109eG3) in the source and drain access regions but not in a region below the first gate (G1);

wherein the plurality of layers is formed having a recess (130) which extends into and has a recess surface (131) in the fourth layer (109) that is covered by an insulating layer (113) on which the first gate is located;

11. A FET according to claim 10 wherein the third layer has thickness between about 3 nm and 20 nm

12. A FET according to claim 10 or claim 11 wherein x has a value between about 0.08 and about 0.22

13. A FET according to claim 12 wherein the fourth layer comprise GaN.

14. A FET according to any of the preceding claims wherein the insulating layer is negatively charged.

15. A FET according to any of the preceding claims wherein the fourth layer on either side of the recess has thickness between about 1 nm and about 17 nm.

16. A FET according to any of the preceding claims and comprising second and third gates on opposite sides of the first gate that respectively overlie the fifth nitride layer and access regions for the source and drain.

17. A FET according to claim 16 wherein the ~~plurality of contiguous nitride layers is formed having a~~ recess ~~that extends into and~~ has a second recess surface (132) located in the fifth nitride layer.

18. A FET according to claim 17 wherein the second recess surface is covered by the insulating layer, and the third gate is located on ~~an~~ a portion of the insulating layer covering the second recess surface in the fifth nitride layer.

19. A FET according to claim 18 wherein the insulating layer is negatively charged.

20. A FET according to any of the preceding claims wherein if the voltage applied to the first gate is less than about 1 volt the FET does not turn ON.

21. A FET according to claim 19 and comprising a power supply that applies voltages V1, V2~~V1~~, and V3, to the first, second, and third gates to turn the FET ON, wherein the voltages are related by a relationship V2 > V1 > V3.

22. A FET according to claim 26 wherein V3 is negative.

23. A FET according to any of the preceding claims wherein the plurality of nitride semiconductor layer is formed on an insulating substrate layer.

24. A FET according to claim 23 wherein the plurality of nitride semiconductor layers comprises a buffer layer contiguous with the substrate layer.

25. A FET according to claim 24 and comprising a superlattice structure of thin epitaxial semiconductor layers embedded in the buffer layer.

26. A FET according to claim 25 wherein the superlattice structure comprises layers of GaN interleaved with layers of $Al_LGa_{1-L}N$.

27. A FET according to claim 26 wherein each of the layers in the superlattice has thickness between about 1 nm and about 30 nm.

28. A FET according to any of claims 24-27 wherein the buffer layer is doped with compensation impurities.

~~29. A monolithic array comprising a plurality of FETs having their sources and drains configured in a checkerboard pattern comprising a plurality of rows and a plurality of columns wherein each row comprises interleaved sources and drains and each column comprises interleaved sources and drains.~~

~~30. A monolithic array according to claim 29 wherein the array comprises a square array having a number of rows comprising interleaved sources and drains equal to a number of columns comprising interleaved sources and drains.~~

~~31. A monolithic array according to claim 30 and comprising a first conducting layer having ohmic electrical contact with each of the sources.~~

32. A monolithic array according to claim 31 and comprising a second conducting layer electrically isolated from the first layer and having ohmic electrical contact with each of the drains.

33. A monolithic array according to any of claims 32 and comprising a chip carrier that supports the array and has electrical contact pads connected to the array.

34. A monolithic array according to claim 33 wherein the contact pads comprise source pads on opposite sides of the array electrically connected to the first conducting layer.

35. A monolithic array according to claim 34 wherein a plurality of wire bonds electrically connects the source pads to the first conducting layer.

36. A monolithic array according to claim 34 or claim 35 wherein the contact pads comprise drain pads on opposite sides of the array electrically connected to the second conducting layer.

37. A monolithic array according to claim 36 wherein a plurality of wire bonds electrically connects the drain pads to the second conducting layer.

38. A monolithic array according to claim 37 wherein the drain pads and source pads are on different sides of the array.

39. A monolithic array according to any of claims 36-38 and comprising a ball grid array that electrically connects the sources and drains to an interconnection substrate which supports the array and provides electrical contacts for connecting the array to an external circuit.

40. A monolithic array according to claim 39 wherein the FETs are epitaxially formed on a non-conducting substrate on which the FETs are epitaxially formed.

41. A monolithic array according to claim 40 and comprising a first heat sink contiguous with the interconnecting array and a second heat sink contiguous with the substrate.