METHODS FOR ETCHING THE EDGE OF A SILICON WAFER

FIELD OF THE DISCLOSURE

[0001] The present disclosure generally relates to the manufacture of silicon wafers, and more particularly to apparatus and methods for etching the edge of a silicon wafer.

BACKGROUND OF THE DISCLOSURE

[0002] Semiconductor wafers are generally prepared from a single crystal ingot (e.g., a silicon ingot) which is trimmed and ground to have one or more flats or notches for proper orientation of the wafer in subsequent procedures. The ingot is then sliced into individual wafers. The individual wafers are subjected to a number of processing operations to reduce the thickness of the wafer, remove damage caused by the slicing and/or other processing operations, and to create at least one highly reflective surface (e.g., on a front surface of the wafer).

[0003] In addition to having at least one highly reflective surface, semiconductor wafers for advanced applications preferably have edges that are smooth, damage-free, and polished. Damaged edges may cause edge slip during thermal processing of the wafer. In addition, rough or pitted edges may trap particles that can be later released in a wet cleaning bath. The released particles may then undesirably migrate to the surface of the wafer. Furthermore, various films are deposited onto the wafer surface in some applications, which may deposit at the edge of the wafer. If the edge is not sufficiently smooth, residual film deposits at the edge may flake off. The flakes may come into contact with the surface of the wafer thereby causing surface defects. Conventional silicon wafer processing typically includes an edge treatment operation (e.g., polishing or etching) to provide edges that are sufficiently smooth.

[0004] Prior to edge treatment, silicon wafers are typically subjected to a lapping or grinding operation to provide a wafer of the desired flatness, followed by an etching operation (acidic or caustic) to produce a wafer having desired surface roughness. After the flattening and etching operations, the wafers are typically subjected to a double-sided polishing operation to provide smooth front and back wafer surfaces.

[0005] In edge polishing operations, wafer edges, including any orientation notch or flat, are typically polished by applying silica to a polishing pad or other surface that is pressed against the wafer edge. Generally, these polishing operations are carried out at a separate station and involve removing dry wafers from a process cassette, aligning the notches in the wafers, polishing the notch in the wafers, polishing the edge of the wafers, scrubbing and/or cleaning the wafers, spin drying the wafers, and then returning the dry wafers to the process cassette where the wafer can be moved to the next station. While edge polishing has proven effective, this operation increases processing time and cost.

[0006] Edge etching operations typically include directing an etchant to the edge of the silicon wafer, typically to that portion of the surface extending from the peripheral edge to the flat portion of the wafer surface. Prevention of significant contact of the etchant with the flat portion of the wafer surface is addressed by various methods. These methods include supporting the wafer on a chuck and directing the etchant to the edge of the wafer surface. However, in these types of methods, it may be difficult to etch the peripheral edge of the wafer within the contour of a wafer notch. Various other methods involve stacking wafers together, often including gaskets between adjacent wafers, and directing the etchant to the exposed edge portion of the wafer. One disadvantage of these types of edge etching operations is difficulty in separating the wafers after etching.

[0007] Recent advances in grinding technology provide flatter wafers with improved nanotopology, and the grinding surface depth has

become more uniform and shallow. In addition, recent double-sided polishing operations offer the advantage of removal of small amounts of subsurface damage on both sides of the wafer. In fact, increased stock removal by double-sided polishing may increase the burden on the edge treatment (e.g., polishing) operation.

[0008] Thus, there remains an unfulfilled need for a wafer edge treatment method that addresses the disadvantages of current edge treatment operations and is suitable for use in wafer processing operations utilizing recent developments in various aspects of wafer processing (e.g., grinding and/or double-sided polishing).

SUMMARY OF THE DISCLOSURE

[0009] Briefly, therefore, the present disclosure generally relates to a method for treating (e.g., etching) the edge of a silicon wafer.

[0010] In particular, the present disclosure is directed to methods for removing silicon from a surface of a silicon wafer. The wafer comprises a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a radius, R, extending from the central axis to a point along the peripheral edge of the wafer, a point along the peripheral edge of the wafer nearest the central axis, and edge portions of the front and back surfaces of the wafer. The edge portions extend from the nearest peripheral edge point to a point between the nearest peripheral edge point and the central axis and no more than about 15 mm from the nearest peripheral edge point. The method includes contacting with an etchant (i) the peripheral edge of the wafer, (ii) the edge portion of the front surface of the wafer, and (iii) the edge portion of the back surface of the wafer.

[0011] In various embodiments, the contacting of the wafer with the etchant occurs prior to reducing the flatness of the wafer by more than about 50%.

[0012] In other embodiments, the wafer has a total thickness variation of at least about 20 microns prior to contacting the wafer with the etchant.

[0013] In various other embodiments, the method further comprises reducing the total thickness variation of the edge-etched wafer to less than about 3 microns.

[0014] In still further embodiments, the edge portion of the front and back surfaces extend from the nearest peripheral edge point and a point between the nearest peripheral edge point and the central axis and between about 1 mm and about 15 mm from the nearest peripheral edge point.

[0015] In even further embodiments, the method further comprises reducing the flatness of the edge-etched wafer by at least about 50%; contacting the peripheral edge, front surface, and back surface of the edge-etched wafer with a caustic etchant in the form of an aqueous solution comprising a source of hydroxide ions; polishing the front surface and back surface of the edge-etched wafer; and polishing the peripheral edge of the edge-etched wafer.

[0016] The present disclosure is further directed to a silicon wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a radius, R, extending from the central axis to a point along the peripheral edge, a point along the peripheral edge nearest the central axis, edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral point and the central axis and no more than about 15 mm from the nearest peripheral edge point, and central portions of the front and back surfaces of the wafer that extend from the point between the nearest peripheral point and the central axis and the central axis. The front and back surfaces of the wafer have a total thickness variation of at least 20 microns. The central portions of the front and back surfaces of the wafer

have a surface roughness of at least about 0.3 μm Ra. The edge portions of the front and back surfaces of the wafer have a surface roughness of less than about 0.3 μm Ra.

[0017] In another aspect of the present disclosure a silicon wafer comprises a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a radius, R, extending from the central axis to a point along the peripheral edge, a point along the peripheral edge nearest the central axis, edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral point and the central axis, and central portions of the front and back surfaces of the wafer that extend from the point between the nearest peripheral point and the central axis and the central axis. The front and back surfaces of the wafer have a total thickness variation of at least 20 microns. The central portions of the front and back surfaces of the wafer have a surface roughness of at least about 0.3 μm Ra. The edge portions of the front and back surfaces of the wafer have a surface roughness of less than about 0.2 μm Ra.

[0018] The present disclosure is also directed to an edge etching apparatus that comprises a casing and a plurality of rollers disposed within the casing. Each roller includes a central axis and a plurality of annular grooves in generally parallel alignment with the annular grooves of each adjacent roller.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Figs. 1 and 2 are block diagrams illustrating processing steps in traditional wafer processing;

[0020] Fig. 3 is a block diagram illustrating processing steps in a wafer processing method of one embodiment of the present disclosure;

[0021] Fig. 4 is a perspective of a wafer that may be treated by the method of the present disclosure;

[0022] Fig. 5 is a partial perspective of the wafer of Fig. 4 with a portion of the wafer cut away;

[0023] Fig. 6 is a side view of an edge etching apparatus according to one embodiment of the present disclosure;

[0024] Fig. 7 is a top view of the edge etching apparatus of Fig. 6 illustrating the apparatus without wafers;

[0025] Fig. 8 is a top view of the edge etching apparatus of Fig. 6 illustrating the apparatus with wafers loaded therein;

[0026] Fig. 9 is a side view of the edge apparatus of Fig. 6 illustrating the apparatus with a lid in an open position;

[0027] Fig. 10 schematically illustrates surfaces and thicknesses of a silicon wafer prior to edge etching and after edge-etching;

[0028] Fig. 11 is a side view of a roller of one embodiment of the present disclosure;

[0029] Fig. 12 is an enlarged side view illustrating a groove of the roller of Fig. 11;

[0030] Fig. 13 is an enlarged side view of a wafer edge that may be treated by the method of the present disclosure;

[0031] Fig. 14 is an enlarged side view illustrating a wafer engaged with the groove of Fig. 12;

[0032] Fig. 15 is an enlarged side view illustrating a wafer engaged with a groove according to a second embodiment of the present disclosure;

[0033] Fig. 16 is an enlarged side view illustrating a wafer engaged with a groove according to a third embodiment of the present disclosure;

[0034] Fig. 17 is an end view of the roller of Fig. 11;

[0035] Fig. 18 is a side view of a roller of a second embodiment of the present disclosure; and

[0036] Fig. 19 is an end view of the roller of Fig. 18.

[0037] Corresponding reference characters indicate corresponding parts throughout the drawings.

DETAILED DESCRIPTION

[0038] The present disclosure provides a method for treatment of an edge portion of a silicon wafer with an acidic or caustic etchant. In accordance with the present disclosure, the edge of the wafer is etched to remove wafer damage caused by prior treatment (e.g., edge grinding). In particular, the method of the present disclosure involves treating the edge of the wafer prior to any significant reduction in flatness of the wafer. For example, in various embodiments of the present disclosure the edge etching operation is conducted prior to a lapping or grinding operation (e.g., prior to reducing the flatness of the wafer by at least about 50% as measured by the GBIR method).

[0039] In one embodiment, treating an edge portion of the wafer includes contacting a portion of the front and/or back surface of the wafer with the caustic etchant and, in another embodiment, with an acidic etchant. It should be noted that use of a caustic or an acidic etchant may degrade the flatness of the wafer edge and any other portion of the wafer surface contacted with the etchant. However, this potential negative of the edge

etching operation may be addressed by conducting the edge etching operation prior to flatness treatment of the wafer, which is suitable for addressing any wafer flatness degradation caused by edge etching (e.g., double-sided polishing).

[0040] Fig. 1 depicts a traditional wafer processing flow. As shown, the surface of the wafer is etched (acidic or caustic) to remove mechanical damage to the wafer during wafer shaping operations (e.g., the wafer lapping and/or grinding operation), and to remove edge damage to the wafer caused during the edge grinding operation. Regardless of the particular etching operation, the etched wafer is typically subjected to an edge polishing operation, followed by a double-sided polishing operation. As noted, double-sided polishing operations generally do not treat the edge of the wafer surface. Fig. 2 depicts an additional example of conventional wafer processing flow in which a wafer is treated by a double-sided grinding operation, caustic etching, followed by edge polishing.

[0041] Fig. 3 depicts one embodiment of a wafer processing flow in accordance with the present disclosure. As shown, the wafer is subjected to edge etching prior to double-sided grinding flatness treatment. As noted, wafer surface damage caused by edge etching is addressed by subsequent wafer treatment. In addition, edge etching in accordance with embodiments of the present disclosure provides advantages over prior edge treatment methods, including edge polishing as shown in Fig. 2. Namely, as previously noted, conventional edge polishing operations generally require multi-step treatment of the wafer that increases wafer processing time and cost whereas the edge etching process of embodiments of the present disclosure is simpler and more economical than these conventional edge polishing operations. For example, equipment and material costs of the edge etching method are generally lower than those associated with conventional multi-stage edge polishing operations.

[0042] In addition, the method of the present disclosure avoids excessive material costs as the entire wafer surface is not contacted with the etchant. Moreover, as noted elsewhere herein, the present method avoids the need for separation of stacked wafers upon completion of edge etching associated with various conventional edge etching operations that is often difficult and/or time-consuming. The edge etching methods disclosed herein may also reduce edge polishing times thus increasing throughput of the treatment process.

[0043] An edge portion of a silicon wafer surface to be treated by the present method is generally contacted with an etchant by immersing the edge portion of the wafer in the etchant. In various embodiments, the wafer is rotated to continuously contact an edge portion of the wafer by immersing the edge portion in a bath comprising the etchant. For example, an edge portion may be contacted with the etchant by rotating a wafer around an axis generally parallel to a top surface of the etchant or a bath comprising the etchant (e.g., around an axis generally parallel to the etchant or bath or at an angle ranging from 0° to 89°, with respect to a top surface of the etchant or bath). For example, the wafer is typically rotated about an axis oriented at an angle from about 0° to about 60°, from about 0° to about 40°, from about 0° to about 20°, or from about 0° to about 10° with respect to a top surface of the etchant.

I. Starting Material

[0044] The processes of embodiments of the present disclosure generally employ as a starting material a silicon wafer that has been sliced from a single crystal silicon ingot and further processed, for example, using conventional grinding apparatus to profile and/or chamfer the peripheral edge of the wafer. This processing reduces the risk of wafer damage during further processing, reduces the non-uniform damage caused by the slicing process and roughly improves the general flatness and parallelism and flatness of the front and back surfaces. The wafer may be sliced from the ingot using any

means known to persons skilled in the art, such as, for example, an internal diameter slicing apparatus or a wiresaw slicing apparatus. Wafer slicing and grinding processes are well-known to those skilled in the art.

[0045] Regardless of the precise combination of prior processing, the silicon wafer starting material may have any conductivity type, resistivity, diameter, crystal orientation and target thickness appropriate for the intended semiconductor application. For example, the wafer diameter is generally at least about 100 mm and may be about 150 mm, about 200 mm, about 300 mm, about 450 mm or greater, and the thickness of the wafer may be from about 475 µm to about 900 µm or greater, with the thickness typically increasing with increasing diameter. Stated another way, the radius of the wafer may be at least about 25 mm or at least about 50 mm, and even may be about 75 mm, about 100 mm, about 150 mm, about 225 mm or greater. The wafer may have any crystal orientation including, for example, <100>, <110>, and <111> crystal orientations.

II. Edge Etching

[0046] Generally, the methods of embodiments of the present disclosure comprise treating the peripheral edge and an edge portion of a silicon wafer by removing silicon from the peripheral edge and the edge portion of the wafer to provide a smooth edge surface. Typically, a point along the peripheral edge of the wafer nearest the central axis is defined by a notch. As used herein, the term "notch depth" refers to that point along the radius toward the central axis to which an orientation notch extends. In accordance with these embodiments, an edge portion of the wafer contacted with the etchant is defined by the peripheral edge of the wafer and a point between the notch depth and the central axis (e.g., a point no more than about 15 mm from the peripheral edge, between about 1 mm and about 15 mm from the peripheral edge, or from the peripheral edge point nearest the central axis within any of the above-noted limits).

[0047] Referring now to Fig. 4, silicon wafers treated by the present method generally include a central axis X, a front surface 3 and a back surface 5 that are generally perpendicular to the central axis, and a radius (R) extending from the central axis to a point on the peripheral edge of the wafer. The wafer also includes a peripheral edge 7 and an edge portion 11. The edge portion extends from the peripheral edge point 13 most near the edge 7 to a second point 15 that is more near the central axis than the peripheral edge point 13. The points may extend around the wafer to form a circle, and are depicted in Fig. 4 as dashed line circles.

[0048] The wafers to be treated also generally include one or more flats or orientation notches 9 at the peripheral edge 7 of the wafer 1. The peripheral edge may include a plurality of flats, but generally includes one point along the peripheral edge of the wafer 1 nearest to the central axis X. The edge portion 11 of the wafer surface contacted with the etchant corresponds to a portion of the wafer surface extending from the point along the peripheral edge nearest the central axis to a point between the nearest peripheral edge point and the central axis. Generally, the edge portion is defined by a point no more than about 15 mm from the nearest peripheral edge point. In various embodiments, the edge portion is defined by a point no more than about 12 mm, no more than about 10 mm, no more than about 8 mm, or no more than about 6 mm from the nearest peripheral edge point (e.g., a point no more than about 5 mm, no more than about 4 mm, no more than about 3 mm, no more than about 2 mm, or no more than about 1 mm from the nearest peripheral edge point). The edge portion contacted with the etchant generally includes the peripheral edge of the wafer and a portion of the front surface and back surface of the wafer.

[0049] In these and various other embodiments, the edge portion of the wafer surface is defined by a point between about 1 mm and about 15 mm from the nearest peripheral edge point, between about 1 mm and about 12 mm from the nearest peripheral edge point, or between about 1 mm and about 10 mm from the peripheral edge point. Typically, the edge

portion is defined by a point between about 1 mm and about 8 mm from the nearest peripheral edge point, more typically between about 1 mm and about 6 mm from the nearest peripheral edge point and, more typically, between about 1 mm and about 5 mm from the nearest peripheral edge point (e.g., between about 1 mm and about 4 mm, between about 1 mm and about 3 mm, or between about 1 mm and about 2 mm from the nearest peripheral edge point).

[0050] As shown in Fig. 5 the edge 7 of the wafer includes two bevels 7a and an apex 7b intermediate the bevels.

[0051] As noted, contact of an edge portion of the wafer surface with the etchant includes contact of the peripheral edge and a portion of the front and/or back surface of the wafer. However, contact of a substantial portion of the wafer surface (e.g., total submersion of the wafer) is generally avoided to minimize unnecessary consumption of etchant. In this regard it is to be noted that the radial distance to which the front surface and back surface are contacted with etchant are generally similar, but may vary based on processing conditions and apparatus limitations.

[0052] Processes of embodiments of the present disclosure are generally conducted by immersing an edge portion of one or more wafers in a bath, or pool of etchant. Other processes are contemplated within the scope of this disclosure. Generally one or more wafers are positioned so that rotation of the wafer(s) immerses them in a pool, or bath, of etchant. As previously noted, conventional edge polishing typically involves a multi-step operation. Process of embodiments of the present disclosure is a single-step operation and may be easily incorporated into the overall silicon wafer processing operation including, for example, between wafer shaping operations (e.g., edge grinding) and caustic etching of the wafer surface as shown in Fig. 3. It is to be further noted that the present process provides a further benefit with respect to process efficiency since it is amenable to concurrent treatment of a plurality of wafers. More particularly, the present

process may be easily adapted to treatment of edge portions of at least 2, at least 4, at least 5, at least 6, at least 8, at least 10, or more wafers. For example, the present process may be adapted to treatment of at least 10 wafers, at least 20 wafers, at least 30 wafers, at least 40 wafers, or at least 50 wafers.

[0053] In one embodiment, wafers undergo a light caustic etch immediately proceeding or immediately following the edge etch. The light caustic etch relieves stress in the wafer and helps prevent any bowing or warp caused by the edge etch. The light etch may remove from about 0.5 μm to about 2 μm and more typically from about 0.8 μm to about 1.2 μm of material from the surfaces of the wafer. In another embodiment, the wafers undergo a double-sided grind following the edge etch to reduce the wafer flatness.

III. Edge Etching Apparatus

[0054] Figs. 6-9 illustrate one embodiment of an edge etching apparatus or etcher 20 suitable for use in the processes of the present disclosure. As shown in Fig. 6 the edge etcher 20 generally includes a casing 25. Within the casing 25 are rollers 35 that may support a number of wafers 45. It is to be understood that rollers 35 may be located in various other arrangements besides that shown in Fig. 6. For example, the etcher 20 may include more, or less, rollers 35 than depicted in Fig. 6. In addition, the etcher may include one continuous section of rollers around an outer edge of the wafer 45 (e.g., rollers extending between the sections of rollers 35 shown in Fig. 6). A driving mechanism (not shown) drives rotation of the rollers 35. The driving mechanism may include a gear that rotates to drive each of the rollers of the edge etching apparatus. The gear may be driven by, for example, an electric motor.

[0055] The apparatus 20 may also include top rollers 46 within the casing 25. The top rollers 46 help the wafer 45 to more precisely rotate about its axis. For purposes of the present disclosure, “top rollers” includes

rollers positioned to engage wafers at a point on the uppermost 180 degrees of the wafer circumference. The top rollers 46 may adjustably move up and down relative to the casing 25 such that the top rollers "float" above the wafers 45. Weights may be attached to the top rollers 46 to assist the rollers in engaging and securing the wafers 45. The upper rollers 46 may be attached to a lid 60 that may open and shut as appropriate for loading and unloading of wafers.

[0056] Fig. 7 is a top view of the etching apparatus 20 without wafers loaded therein. Further, the etching apparatus 20 is illustrated without a lid and top rollers for purposes of illustration. As shown, each of the rollers 35 include grooves 40 that are generally in alignment with the grooves of adjacent rollers 35. In this manner, multiple wafers in generally parallel alignment may be secured by the rollers. The casing 25 may include an opening 50. A valve (not shown) may be formed within the opening 50 to regulate the flow of etchant into and out of the casing 25. Fig. 8 is a top view of the etching apparatus 20 including a plurality of wafers 45 secured by the roller/groove arrangement shown in Fig. 7. Fig. 9 is a side view of the apparatus 20 illustrating the apparatus with a lid 60 open. The top rollers 46 are attached by suitable means to the lid 60.

[0057] In conventional apparatus, one must separate each wafer after etching from a stack of wafers. This process can be labor-intensive, difficult and time consuming. Use of the etching apparatus 20 as depicted in Figs. 6-9 eliminates this separation step.

[0058] In one embodiment of a method of this disclosure, wafers are added to the edge etching apparatus 20 such that the wafers are pinched between the grooves 40 of the rollers 35. The lid 60 is closed to seat the wafers 45 in the grooves of top rollers 46. For contact of the wafers 45 with the etchant, the edge etching apparatus 20 may be immersed in a pool of etchant (not shown) to cause etchant to enter the etching apparatus through the opening 50 shown in Fig. 7. Alternatively, etchant may be introduced

directly into the casing 25 through a second opening (not shown). The valve within the opening 50 is closed to cause the etchant level to rise until etchant contacts the edge of the wafers 45 (Fig. 6). The final etchant level is designated by dashed line 52.

[0059] The depth of the reservoir of etchant in the etching apparatus is determined by the amount of etchant in the pool of etchant, the depth to which the etcher is immersed in the pool and/or the amount of etchant directly added into the casing 25. The apparatus 20 may also include an overflow hole (or "slot" or "weir") (not shown) with the lowest point of the overflow hole defining the depth of etchant in the apparatus. In one embodiment, etchant that exits the overflow hole may be returned back to the apparatus 20.

[0060] The depth of etchant in the edge etching apparatus 20 generally corresponds to the distance from the peripheral edge along the radius of the wafer to which the wafer is contacted with the etchant.

[0061] Once the etcher is immersed in the etchant, the rollers 35 are driven by a central gear (not shown) to rotate the wafers and immerse the wafers in the pool, or bath, of etchant.

[0062] After etching, the apparatus 20 may be removed from the pool of etchant. In embodiments, where etchant is added directly to the casing 25, the valve in the opening 50 may be opened to cause etchant to exit or be expelled from the casing. The lid 60 is opened and the wafers 45 may be removed from the etching apparatus 20.

[0063] Fig. 11 depicts a roller 305 that may be used in the edge etching apparatus as depicted in Figs. 6-9 and may also be used in various other embodiments. The roller 305 shown in Fig. 11 includes a central axis X and includes a plurality of annular grooves 310 about the axis X. As shown in Fig. 11, each roller 305 includes ends 315. A side view of an end 315 is illustrated in Fig. 17.

[0064] Fig. 12 shows the annular groove 310 of the roller 305 shown in Fig. 11. The annular groove 310 is defined by a first annular edge 311 and a second annular edge 312. Both edges 311, 312 extend radially inward towards the central axis of the roller. As can be seen from Fig. 12, as the first and second annular edges 311, 312 extend radially inward, the first annular edge and the second annular edge extend axially toward each other. The first annular edge 311 has a most radially inward point 317 and the second annular edge 312 also includes a most radially inward point 319.

[0065] Fig. 13 illustrates an edge of a wafer 45 according to one embodiment of the present disclosure. The illustrated wafer edge is known in the art as being "T-shaped" but other profiles including, for example, "R-shaped" profiles may be used without departing from the scope of the present disclosure. The edge 45 includes an upper bevel 72 and a lower bevel 74. Between the bevels 72, 74 is an apex 75. The apex 75 defines a width W.

[0066] In one embodiment, the distance between the most radially inward point 317 and the most radially inward point 319 of the grove 310 is less than an apex width W of the wafers that the grooves are sized and shaped to receive. As illustrated in Fig. 14, this arrangement allows the wafer 45 to become pinched within the taper of the groove which allows the wafer 45 to more precisely rotate about its axis. A more precise rotation results in a smoother etch about the circumference of the wafer 45.

[0067] In another embodiment, the distance between the most radially inward point 317 of the first edge 311 and the most radially inward point 319 of the second edge 312 is less than an average thickness of the wafer.

[0068] In one embodiment, the distance between the most radially inward point 317 of the first edge 311 and the most radially inward point 319 of the second edge 312 is less than 200 μm. In another embodiment, the distance is less than about 100 μm and, in other

embodiments, from about 50 μm to about 200 μm or from about 50 μm to about 100 μm.

[0069] As illustrated in Fig. 12, a floor 333 extends between the most radially inward point 317 of the first edge 311 and the most radially inward point 319 of the second edge 312. The width of the floor 333 may be less than an apex width W of the wafers that the grooves are sized and shaped to receive (Fig. 14). The apex width W of the wafers may be determined by use of an edge profiling inspection tool. Suitable equipment for edge profile inspecting include the LEP-2200 Edge Profile Monitor (Kobelco, Japan).

[0070] In one embodiment, the width of the floor is from about 50 μm and about 200 μm and, in another embodiment, from about 50 μm and about 100 μm.

[0071] The groove 310 may also include a third annular edge 319 and a fourth annular edge 320. In one embodiment and as illustrated in Fig. 15, the groove does not include the third edge and fourth edge but rather only includes a first edge 311' and second edge 312'.

[0072] Referring now to Fig. 16, in one embodiment, the first edge and the second edge intersect to form a vertex point 315''. The vertex point 315'' defines the most radially inward point of the first edge 311'' and the most radially inward point of the second edge 312''.

[0073] Fig. 18 illustrates a roller 405 that may be used in an edge etching apparatus as depicted in Figs. 6-9 and in various other embodiments. The roller 405 includes an end 415 that differs in design from the end 315 of Fig. 11. The roller 405 includes grooves 410. The grooves 410 may have the same configuration as any one of the grooves illustrated in Figs. 14-16.

[0074] The conditions of edge etching may be selected by one skilled in the art depending on the particular circumstances (e.g., the number of wafers to be treated and the desired characteristics of the edge-etched wafer(s)). For example, generally the one or more wafers are rotated at a rate that prevents etchant from flowing inward beyond the edge portion to the inner, or central portion of the wafer surface (e.g., at least about 10 revolutions per minute (rpm)), but generally below rates that may result in equipment damage and/or movement of wafers (e.g., speeds in excess of about 200 rpm). Thus, generally the wafers are rotated at a rate of at least about 10 revolutions per minute (rpm), at least about 20 rpm, at least about 30 rpm, at least about 50 rpm, at least about 75 rpm or even at least about 90 rpm. Typically, the wafers are rotated at a rate of from about 10 rpm to about 60 rpm, from about 20 rpm to about 50 rpm, or from about 30 rpm to about 45 rpm. In other embodiments the wafers are rotated from about 75 rpm to about 125 rpm or from about 90 rpm to about 110 rpm. Other conditions may be used within the scope of this disclosure.

[0075] In one embodiment, the direction of rotation of the wafers may be reversed such that the wafers are rotated in both clockwise and counter-clockwise directions while being contacting with etchant. In one embodiment, the wafers are rotated in a clockwise direction for about 60 seconds at a speed of about 100 rpm and in a counter-clockwise direction for about 60 seconds at a speed of about 100 rpm.

[0076] The time for which the edge portion is immersed in the etchant may be selected in view of, for example, the starting edge surface roughness and/or the desired finished edge surface features. Regardless of the particular circumstances, the peripheral edge and edge portions of the wafer surface are generally immersed in the etchant for at least about 30 seconds, at least about 1 minute, at least about 2 minutes, at least about 3 minutes, at least about 4 minutes, or at least about 5 minutes. In accordance with these and various other embodiments, the peripheral edge and edge portions of the wafer are immersed in the etchant for no more than about 30

minutes, no more than about 20 minutes, or no more than about 10 minutes. For example, the peripheral edge and edge portions of the wafer may be contacted with the etchant for a time of from about 1 minute to about 20 minutes, from about 1 minute to about 15 minutes, or from about 2 minutes to about 10 minutes.

[0077] The amount of silicon removed from the peripheral edge and edge portions of the wafer surfaces varies depending on the particular circumstances and conditions, but generally processes of embodiments of the present disclosure provide sufficient removal to provide a peripheral edge and edge portions that are sufficiently smooth in view of the fact that double-sided polishing does not address edge roughness. Generally, the peripheral edge and edge portions of the wafer are immersed in the etchant for a time such that at least about 10 μm, at least about 20 μm, at least about 30 μm, at least about 40 μm, or at least about 50 μm of silicon, in terms of total thickness, is removed from the edge portions of the wafer surface. Typically, the peripheral edge and edge portions of the wafer are immersed in the etchant for a time such that from about 10 to about 100 μm, more typically from about 20 to about 90 μm and, still more typically, from about 30 to about 80 μm (e.g., from about 40 to about 60 μm of silicon), in terms of total thickness is removed from the edge portion of the wafer surface.

[0078] In one embodiment, the peripheral edge and edge portions of the wafer are immersed in the etchant for a time such that the diameter of the wafer is reduced by at least about 10 μm, at least about 20 μm, at least about 30 μm, at least about 40 μm, or at least about 50 μm. Typically, the peripheral edge and edge portions of the wafer are immersed in the etchant for a time such that the diameter of the wafer is reduced by from about 10 to about 100 μm, more typically from about 20 to about 90 μm and, still more typically, from about 30 to about 80 μm.

IV. Edge Etched Wafers

[0079] As noted elsewhere herein and depicted in Fig. 3, the edge etching method of embodiments of the present disclosure is conducted prior to wafer flatness treatment (e.g., lapping or grinding). Accordingly, edge etching is typically conducted prior to reducing the flatness of the front and back surface of a wafer cut from a silicon ingot by at least about 50%, at least about 60%, at least about 70%, at least about 80% and, even more typically, at least about 90% (e.g., at least about 95%) as determined by the GBIR method. Thus, generally front and back surfaces of the wafer to be edge-etched exhibit a total thickness variation of at least about 10 microns, typically at least about 20 microns and, more typically, at least about 25 microns. Edge etching may impact overall wafer flatness. Accordingly, the surfaces of edge-etched wafers typically exhibit total thickness variations in excess of 20 microns or in excess of about 25 microns (e.g., greater than about 30 microns, or greater than about 35 microns).

[0080] Wafer treatment processes that are performed after the edge etch such as, for example, grinding, double-sided polishing and/or finish polishing) typically reduce the flatness of the front surface of the wafer (as measured after being cut from the ingot and after the treatment process) by at about 50%, at least about 60%, at least about 70%, at least about 80% and, even, at least about 90% as determined by the GBIR method. In other embodiments, the flatness of the back surface of the wafer is reduced by the above-noted amounts.

[0081] Also shown in Fig. 3, edge etching of the present method is typically conducted prior to surface roughness treatment of the front and back surfaces of the wafer (e.g., acidic or caustic etching of the entire wafer surface). Accordingly, a portion of the front surface of edge-etched wafers and, particularly, the portions of the wafers not contacted with etchant (i.e., a central potion of the surfaces that extends from the most radially inward point to which etchant contacts the wafer and the central axis), will typically exhibit

an average surface roughness of at least about 0.3 μm Ra (at least about 3 μm Rt), at least about 1 μm Ra (at least about 10 μm Rt), or at least about 1.5 μm Ra (at least about 15 μm Rt). Typically, the central portion of the front surface of the edge-etched wafer exhibits surface roughness of from about 0.3 to about 2.5 μm Ra (from about 3 to about 25 μm Rt), from about 0.7 to about 2 μm Ra (from about 7 to about 20 μm Rt), or from about 1 to about 1.5 μm Ra (from about 10 to about 15 μm Rt).

[0082] Additionally or alternatively, a portion of the back surface of edge-etched wafers (i.e., the corresponding central portion of the back surface of the wafer) typically exhibits an average surface roughness of at least about 0.3 μm Ra (at least about 3 μm Rt), at least about 1 μm Ra (at least about 10 μm Rt), or at least about 1.5 μm Ra (at least about 15 μm Rt). Typically, the central portion of the back surface of an edge-etched wafer exhibits surface roughness of from about 0.3 to about 2.5 μm Ra (from about 3 to about 25 μm Rt), from about 0.7 to about 2 μm Ra (from about 7 to about 20 μm Rt), or from about 1 to about 1.5 μm Ra (from about 10 to about 15 μm Rt). Regardless of the initial surface roughness of a portion of the front and/or back surface it is to be noted that edge etching in accordance with the present disclosure generally has little, if any effect on the roughness of these surfaces. For example, typically the surface roughness of either or both of a front and back surface changes by no more than about 5%, no more than about 2%, and preferably no more than about 1% (e.g., no more than about 0.5%).

[0083] Since edge etching removes edge damage, the edge surface roughness of edge-etched wafers is less than the overall front surface and back surface roughness. For example, the surface roughness of an edge portion of edge-etched wafers is typically less than about 1 μm Ra, less than about 0.5 μm Ra, less than about 0.3 μm Ra, less than about 0.2 μm Ra, or less than about 0.1 μm Ra. Typically, edge surface roughness of edge-etched wafers is from about 0.05 to about 1 μm Ra, from about 0.1 to about 0.6 μm Ra, or from about 0.2 to about 0.5 μm Ra.

[0084] In various embodiments, after edge etching is complete, typically the total thickness variation of the surfaces of the edge-etched wafer is reduced (e.g., by grinding or lapping) to less than about 3 microns, less than about 2 microns, or less than about 1 micron.

[0085] Fig. 10 illustrates a wafer 200 prior to edge etching having an initial thickness T_0 defined by a front surface 205 and a back surface 210. Wafer 200 also includes a notch 215 extending from the peripheral edge of the wafer 220 to a notch depth 225 defining an edge portion P_e of the wafer surface. Wafer 200 also has an immersion region I extending from the peripheral edge 220 to a depth D that includes the edge portion P_e of the wafer surface and a portion of the front surface 205 and back surface 210 of the wafer.

[0086] Fig. 10 also illustrates an edge-etched wafer 250 including an edge-etched region 255 that includes an etched notch portion 260 and an etched portion of the front surface 205' and an etched portion of the back surface 210'. Contact with the etchant provides silicon removal R from the front and back surface of the wafer for a total silicon removal from the immersion region of 2R and a final thickness of the immersion region of T_f (T_0 - 2R).

V. Acidic Etchant

[0087] Acidic etchants suitable for edge etching in accordance with the present disclosure include those generally known in the art including, for example, those described in U.S. Patent Nos. 3,964,957; 5,340,437; 5,211,794; 4,388,140; 5,236,548; 5,246,528; 4,971,645; 4,251,317; 4,849,701; 6,294,469; 5,233,218; 6,482,749; 6,046,117, the entire contents of which are incorporated herein by reference for all relevant purposes. Generally, the acidic etchant is in the form of an aqueous solution comprising a source of hydrogen ions. The source of hydrogen ions may be selected from the group consisting of hydrofluoric acid, nitric acid, phosphoric acid, acetic acid, sulfuric acid, hydrochloric acid, citric acid, oxalic acid, propionic

acid, permanganic acid, and combinations thereof. Typically, the source of hydrogen ions is present in the etchant at a concentration of at least about 40 wt%, more typically at least about 50 wt%, still more typically at least about 60 wt% and, even more typically, at least about 70 wt% (e.g., at least about 80 wt%, or at least about 90 wt%).

[0088] In various embodiments, the acidic etchant consists essentially of water and the source of hydrogen ions. In various other embodiments, the acidic etchant comprises one or more additives along with the source of hydrogen ions. For example, the acidic etchant may comprise a surfactant selected from the group consisting of ammonium fluoroalkylsulfonate (e.g., Novec™ 4300), potassium perfluorooctanesulfonate, dodecylbenzene sulfonic acid, alkyl aryl sulfonic acid, and combinations thereof. In various embodiments the acidic etchant may comprise a fluorochemical surfactant (e.g., Fluorad® FC-95). Whether a surfactant is the lone additive, or other additives are included in the etchant, the volumetric ratio of additive to source of hydrogen ions is generally at least about 0.001:1, typically at least about 0.002:1 and, more typically, at least about 0.003:1. For example, in various embodiments the volumetric ratio of additive to source of hydrogen ions is from about 0.001 to about 1:1, from about 0.002:1 to about 0.5:1, or from about 0.003:1 to about 0.25:1.

VI. Caustic Etchant

[0089] Caustic etchants suitable for edge etching in accordance with the present disclosure include those generally known in the art including, for example, those described in U.S. Patent Nos. 7,323,421; 6,110,839; 6,383,060; and 6,503,363, the entire contents of which are incorporated herein by reference for all relevant purposes. Generally, the caustic etchant is in the form of an aqueous solution comprising a source of hydroxide ions. The source of hydroxide ions generally comprises an alkali metal hydroxide selected from the group consisting of sodium hydroxide, potassium hydroxide, tetramethyl ammonium hydroxide, and combinations thereof.

EXAMPLES

Example 1: Evaluation of Edge Quality of Edge Etched Wafers

[0090] Edge portions of 15 P^- 300 mm wafers were etched utilizing an edge etcher of the type shown in Figs. 6-9. The edge portions were immersed in a pool of 300 ml of acidic etchant from the following mixture: 2.4 l of HNO_3 (69 wt. %), 2 l of H_3PO_4 (85 wt %) and 0.55 l of HF (49 wt %).

[0091] Two runs were carried out, one in which an edge portion of 7 wafers were etched with the edge portion extended from the nearest peripheral edge point to a point approximately 8.5 mm from the nearest peripheral edge point. In the second run 8 wafers were etched with the edge portion extending to a point approximately 8.5 mm from the nearest peripheral edge point.

[0092] The etch time of the first, 7 wafer run was 300 seconds, with rotation reversal after 150 seconds. Silicon removal, based on OGP diameter (a comparison of wafer diameter prior to and after etching) was approximately 30 μm.

[0093] The etch time of the second, 8 wafer run was 360 seconds, with rotation reversal after an etch time of 150 seconds. Silicon removal, based on OGP diameter, was also approximately 30 μm.

[0094] Both runs were conducted at a wafer spin speed of from 25 to 30 rpm.

[0095] At the end of each etching cycle, the tank containing the pool of etchant was emptied and the wafers were rinsed with a spray of water for approximately 2 minutes to remove residual acid. The rinsed wafers were removed from the tank and dried. Wafers were then ground, double-sided polished, edge polished and evaluated for edge quality.

[0096] Edge quality, as measured by Chapman roughness was comparable to standard product. Edge measurements showed little residual damage.

Example 2: Determination of the Amount of Material Removed by Edge Etching

[0097] 300 mm wafers (75) were cut from a single crystal silicon ingot. After edge grinding, the edge portions of the wafers were etched utilizing an edge etcher of the type shown in Figs. 6-9.

[0098] The wafers were split into a first group of 39 wafers and a second group of 36 wafers. The first group of wafers was edge polished (EP-300-X, SpeedFam) for 11 seconds and the second group was edge polished for 8 seconds.

[0099] A third group (75) of wafers was cut from a single wafer and subjected to edge grinding and edge polishing (EP-300-X, SpeedFam). The edge polish was a conventional 13 seconds in length.

[00100] The edge etched wafers were then combined and double-sided polished. The wafers of the third group were also double-sided polished (AC-2000-P2, PeterWolters). The cassettes of all batches of wafers were combined and a finish polish was performed (LapMaster). The double-sided polish removed approximately 15 μm of material from the wafer surfaces.

[00101] The average diameter (OGP) of the edge etched wafers was 299.9946 mm after finish polishing and the average diameter (OGP) of the wafers that were not edge etched was 300.0211 mm after finish polishing. This corresponds to a 13.5 μm reduction in material from the wafer edge for edge etched wafers relative to edge polished wafers.

Example 3: Flatness Comparison between Wafers that were and were not Edge Polished

[00102] The flatness of the three batches of wafers of Example 2 was determined by both GBIR, SBIR and SFQR methods after finish polishing. The results are shown in Table 1 below.

	Average IR	Average SBIR Max	Average SFQR Max
Non-Edge Etched (13 sec)	308.7	118.7	29.8
Edge Etched (11 sec)	315.9	124.5	41.3
Edge Etched (8 sec)	299.8	108.5	37.0

Table 1: Flatness data for edge etched wafers and non-edge etched wafers after double-sided polishing and finish polishing

As can be seen from Table 1, edge etching did not significantly degrade the flatness of finish polished wafers.

Example 4: Edge Quality Comparison between Wafers that were and were not Edge Polished

[00103] The edge quality of the wafers was then tested on a Raytex edge inspection system (Raytex-300) the system outputs were averaged for each group. The results of the analysis are shown in Table 2 below.

	Average DC	Average AC
Non-Edge Etched (13 sec)	488.3	145.3
Edge Etched (11 sec)	492.2	133.6
Edge Etched (8 sec)	491.7	130.1

Table 2: Raytex measurements for edge etched and non-edge etched wafers after finish polishing

As can be seen from Table 2, the DC output (which is indicative of the amount of pits/chips/bumps) was only slightly worse for etched wafers and the AC

output for edge etched wafers (indicative of a smooth surface finish) was better than non-edge etched wafers.

[00104] The edge quality of the wafers was then determined by measuring the roughness by use of a Chapman profiler. The roughness was measured across the front bevel, back bevel and apex of the edge. The roughness was measured on three wafers from each batch at four points per wafer for a total of 12 points for each batch. The results were then averaged. The roughness measurements (Ra and RMS) are shown in Table 3.

	Front Bevel Ra (average)	Front Bevel RMS (average)	Back Bevel Ra (average)	Back Bevel RMS (average)	Apex Ra (average)	Apex RMS (average)
Non-Edge Etched (13 sec)	4.95	6.22	5.18	6.56	11.56	14.51
Edge Etched (11 sec)	5.22	6.47	5.10	6.46	10.35	12.89
Edge Etched (8 sec)	5.47	7.10	4.76	5.97	11.10	13.91

Table 3: Ra and RMS edge roughness for edge etched wafers and non-edge etched wafers

As can be seen from Table 3, edge etching does not significantly increase the roughness of the edge of the wafer.

[00105] The present disclosure is not limited to the above embodiments and can be variously modified. The above description of the embodiments, including the Examples, is intended only to acquaint others skilled in the art with the disclosure, its principles, and its practical application so that others skilled in the art may adapt and apply the disclosure in its numerous forms, as may be best suited to the requirements of a particular use.

[00106] With reference to the use of the word(s) comprise or comprises or comprising in this entire specification (including the claims below), unless the context requires otherwise, those words are used on the basis and clear understanding that they are to be interpreted inclusively, rather than exclusively, and applicants intend each of those words to be so interpreted in construing this entire specification.

[00107] When introducing elements of the present disclosure or the embodiment(s) thereof, the articles "a", "an", "the" and "said" are intended to mean that there are one or more of the elements. The terms "comprising", "including" and "having" are intended to be inclusive and mean that there may be additional elements other than the listed elements.

[00108] In view of the above, it will be seen that the several objects of the disclosure are achieved and other advantageous results attained.

WHAT IS CLAIMED IS:

1. A method for removing silicon from a surface of a silicon wafer, the wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a peripheral edge, a radius, R, extending from the central axis to a point along the peripheral edge of the wafer, a point along the peripheral edge of the wafer nearest the central axis, and edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral edge point and the central axis and no more than about 15 mm from the nearest peripheral edge point, the method comprising:

contacting with an etchant (i) the peripheral edge of the wafer, (ii) the edge portion of the front surface of the wafer, and (iii) the edge portion of the back surface of the wafer, wherein the peripheral edge and the edge portions of the front surface and back surface are contacted with the etchant prior to reducing the flatness of the front surface of the wafer by more than about 50%.

2. A method for removing silicon from a surface of a silicon wafer, the wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a peripheral edge, a radius, R, extending from the central axis to a point along the peripheral edge of the wafer, a point along the peripheral edge of the wafer nearest the central axis, and edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral edge point and the central axis and no more than about 15 mm from the nearest peripheral edge point, the method comprising:

contacting with an etchant (i) the peripheral edge of the wafer, (ii) the edge portion of the front surface of the wafer, and (iii) the edge portion of the back surface of the wafer, wherein the wafer has a total thickness variation on

the front surface of the wafer of least about 20 microns prior to said contacting.

3. A method for removing silicon from a surface of a silicon wafer, the wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a peripheral edge, a radius, R, extending from the central axis to a point along the peripheral edge of the wafer, a point along the peripheral edge of the wafer nearest the central axis, and edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral edge point and the central axis and no more than about 15 mm from the nearest peripheral edge point, the method comprising:

contacting with an etchant (i) the peripheral edge of the wafer, (ii) the edge portion of the front surface of the wafer, and (iii) the edge portion of the back surface of the wafer, thereby producing an edge-etched wafer; and

reducing the total thickness variation of the edge-etched wafer to less than about 3 microns.

4. The method of any one of claims 1 to 3 wherein the edge portions of the front and back surfaces of the wafer extend from the nearest peripheral edge point to a point no more than about 10 mm from the nearest peripheral edge point.

5. The method of any one of claims 1 to 3 wherein the edge portions of the front and back surfaces of the wafer extend from the nearest peripheral edge point to a point no more than about 4 mm from the nearest peripheral edge point.

6. The method of any one of claims 1 to 3 wherein the edge portions of the front and back surfaces of the wafer extend from the nearest peripheral edge point to a point no more than about 1 mm from the nearest peripheral edge point.

7. A method for removing silicon from a surface of a silicon wafer, the wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a peripheral edge, a radius, R, extending from the central axis to a point along the peripheral edge of the wafer, a point along the peripheral edge of the wafer nearest the central axis, and edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral edge point and the central axis and between about 1 mm and about 15 mm from the nearest peripheral edge point, the method comprising:

contacting with an etchant (i) the peripheral edge of the wafer, (ii) the edge portion of the front surface of the wafer, and (iii) the edge portion of the back surface of the wafer.

8. The method of claim 7 wherein the edge portions of the front and back surfaces of the wafer extend from the nearest peripheral edge point to a point between 1 mm and about 10 mm from the nearest peripheral edge point.

9. The method of claim 7 wherein the edge portions of the front and back surfaces of the wafer extend from the nearest peripheral edge point to a point between 1 mm and about 4 mm from the nearest peripheral edge point.

10. The method of any one of claims 2 to 9 wherein said contacting occurs prior to reducing the flatness of the front and back surface of the wafer by more than about 50%.

11. The method of any one of claims 2 to 9 wherein said contacting occurs prior to reducing the flatness of the front and back surfaces of the wafer by more than about 70%.

12. The method of any of claims 1 to 11 wherein R is at least about 150 mm.

13. The method of any of claims 1 to 12 wherein the peripheral edge and front and back edge portions of the wafer are contacted with the etchant by rotating the wafer.

14. The method of claim 13 wherein the wafer is rotated at a rate of at least about 10 revolutions per minute (rpm).

15. The method of any one of claims 1 to 14 wherein the peripheral edge and front and back edge portions of the wafer are contacted with the etchant for at least about 1 minute.

16. The method of any one of claims 1 to 15 wherein the rotation of the wafer is reversed to cause the wafer to be rotated in both a clockwise and counter-clockwise rotation while the peripheral edge and front and back edge portions of the wafer are contacted with the etchant.

17. The method of any one of claims 1 to 16 wherein the peripheral edge and front and back edge portions of the wafer are contacted with the etchant for a time such that at least about 10 μm, in terms of total thickness, is removed from the front and back edge portions of the wafer.

18. The method of any one of claims 1 to 16 wherein the peripheral edge and front and back edge portions of the wafer are contacted with the etchant for a time such that the diameter of the wafer is reduced by at least about 10 μm.

19. The method of any of claims 1 to 18 wherein peripheral edges and edge portions of a plurality of wafers are concurrently contacted with the etchant.

20. The method of any one of claims 1 to 19 wherein the etchant is an acidic etchant in the form of an aqueous solution comprising a source of hydrogen ions.

21. The method of claim 20 wherein the etchant comprises a source of hydrogen ions selected from the group consisting of hydrofluoric acid, nitric acid, phosphoric acid, acetic acid, sulfuric acid, hydrochloric acid, citric acid, oxalic acid, propionic acid, permanganic acid, and combinations thereof.

22. The method of claim 20 or 21 wherein the etchant further comprises a surfactant selected from the group consisting of ammonium fluoroalkylsulfonate, potassium perfluorooctanesulfonate, dodecylbenzene sulfonic acid alkyl aryl sulfonic acid, and combinations thereof.

23. The method of claim 22 wherein the volumetric ratio of surfactant to the source of hydrogen ions is at least about 0.001:1.

24. The method of any one of claims 1 to 23 wherein the etchant is a caustic etchant in the form of an aqueous solution comprising a source of hydroxide ions.

25. The method of claim 24 wherein the source of hydroxide ions is selected from the group consisting of sodium hydroxide, potassium hydroxide, tetramethyl ammonium hydroxide, and combinations thereof.

26. The method of any one of claims 1 to 25 further comprising contacting the front surface of the wafer with a caustic etchant to relieve stress in the wafer.

27. The method of claim 26 wherein the caustic etchant removes from about 0.5 μm to about 2 μm of material from the surface of the wafer.

28. The method of any one of claims 1 to 27 comprising grinding the front surface and back surface of the edge-etched wafers to reduce the flatness of the wafer.

29. A method for removing silicon from a surface of a silicon wafer, the wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a peripheral edge, a radius, R,

extending from the central axis to a point along the peripheral edge of the wafer, and a point along the peripheral edge of the wafer nearest the central axis, and edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral edge point and the central axis and no more than about 15 mm from the nearest peripheral edge point, the method comprising:

contacting with an etchant (i) the peripheral edge of the wafer, (ii) the edge portion of the front surface of the wafer, (iii) the edge portion of the back surface of the wafer;

reducing the flatness of the edge-etched wafer by at least about 50%;

contacting the peripheral edge, front surface, and back surface of the edge-etched wafer with a caustic etchant in the form of an aqueous solution comprising a source of hydroxide ions;

polishing the front surface and back surface of the edge-etched wafer; and

polishing the peripheral edge of the edge-etched wafer.

30. A silicon wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a radius, R, extending from the central axis to a point along the peripheral edge, a point along the peripheral edge nearest the central axis, edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral point and the central axis and no more than about 15 mm from the nearest peripheral edge point, and central portions of the front and back surfaces of the wafer that extend from the point between the nearest peripheral point and the central axis and the central axis; wherein:

the front and back surfaces of the wafer have a total thickness variation of at least 20 microns;

the central portions of the front and back surfaces of the wafer have a surface roughness of at least about 0.3 μm Ra; and

the edge portions of the front and back surfaces of the wafer have a surface roughness of less than about 0.3 μm Ra.

31. A silicon wafer comprising a central axis, a front surface and a back surface that are generally perpendicular to the central axis, a radius, R, extending from the central axis to a point along the peripheral edge, a point along the peripheral edge nearest the central axis, edge portions of the front and back surfaces of the wafer that extend from the nearest peripheral edge point to a point between the nearest peripheral point and the central axis, and central portions of the front and back surfaces of the wafer that extend from the point between the nearest peripheral point and the central axis and the central axis; wherein:

the front and back surfaces of the wafer have a total thickness variation of at least 20 microns;

the central portions of the front and back surfaces of the wafer have a surface roughness of at least about 0.3 μm Ra; and

the edge portions of the front and back surfaces of the wafer have a surface roughness of less than about 0.2 μm Ra.

32. The silicon wafer of claim 30 or 31 wherein the front and back surfaces of the wafer have a total thickness variation of at least about 25 microns.

33. The silicon wafer of claim 30 or 31 wherein the front and back surfaces of the wafer have a total thickness variation of at least about 35 microns.

34. The silicon wafer of any one of claims 30 to 33 wherein the central portions of the front and back surfaces of the wafer have a surface roughness of from about 0.3 to about 2.5 μm Ra.

35. The silicon wafer of any one of claims 30 to 33 wherein the central portions of the front and back surfaces of the wafer have a surface roughness of from about 0.7 to about 2 μm Ra.

36. The silicon wafer of any one of claims 30 to 33 wherein the central portions of the front and back surfaces of the wafer have a surface roughness of from about 1 to about 1.5 μm Ra.

37. An edge etching apparatus, the apparatus comprising:

a casing; and

a plurality of rollers disposed within the casing, each roller including a central axis and a plurality of annular grooves in generally parallel alignment with the annular grooves of each adjacent roller.

38. The edge etching apparatus of claim 37 wherein the annular grooves are defined by a first annular edge and a second annular edge, the first annular edge and second annular edge both extending radially inward toward the central axis, the first annular edge extending axially toward the second annular edge as the first annular edge extends radially inward.

39. The edge etching apparatus of claim 38 wherein the distance between the most radially inward point of the first edge and the most radially inward point of the second edge is less than an apex width of the wafers that the grooves are sized and shaped to receive.

40. The edge etching apparatus of claim 38 wherein the second annular edge extends axially toward the first annular edge as the second annular edge extends radially inward.

41. The edge etching apparatus of claim 38 wherein the groove is defined by a floor between the most radially inward point of the first edge and the most radially inward point of the second edge and the distance of the width of the floor is less than an apex width of the wafers that the grooves are sized and shaped to receive.

42. The edge etching apparatus of claim 41 wherein the width of the floor is from about 50 μm and about 200 μm.

43. The edge etching apparatus of claim 41 wherein the width of the floor is from about 50 μm and about 100 μm.

44. The edge etching apparatus of claim 41 wherein the second annular edge extends axially toward the first annular edge as the second annular edge extends radially inward.

45. The edge etching apparatus of claim 37 wherein the annular grooves are defined by a first annular edge and a second annular edge, the first annular edge and second annular edge both extending radially inward toward the central axis, the first annular edge extending axially toward the second annular edge as the first annular edge extends radially inward, wherein the distance between the most radially inward point of the first edge and the most radially inward point of the second edge is less than about 200 μm.

46. The edge etching apparatus of claim 45 wherein the distance between the most radially inward point of the first edge and the most radially inward point of the second edge is less than about 100 μm.

47. The edge etching apparatus of claim 46 wherein the distance between the most radially inward point of the first edge and the most radially inward point of the second edge is at least about 50 μm.

48. The edge etching apparatus of claim 45 wherein the distance between the most radially inward point of the first edge and the most radially inward point of the second edge is at least about 50 μm.

49. The edge etching apparatus of claims 37 wherein the first edge and the second edge intersect to form a vertex point that defines the most radially inward point of the first edge and the most radially inward point of the second edge.

50. The edge etching apparatus of claim 49 wherein the second annular edge extends axially toward the first annular edge as the second annular edge extends radially inward.

51. The edge etching apparatus of claim 37 wherein the casing includes an opening for discharging contaminated etchant from the casing.

52. The edge etching apparatus of claim 37 wherein the apparatus includes top rollers within the casing.