

ABSTRACT

According to one embodiment, there is provided a storage device including a control chip and a plurality of memory chips. The control chip has an input buffer common to the control chip and the plurality of memory chips and electrically connected to an external terminal. A first transmission path going through the input buffer and a second transmission path not going through the input buffer are provided between the external terminal and the plurality of memory chips. In a first mode, the control chip enables the input buffer so as to activate the first transmission path and, in a second mode, disables the input buffer so as to activate the second transmission path.