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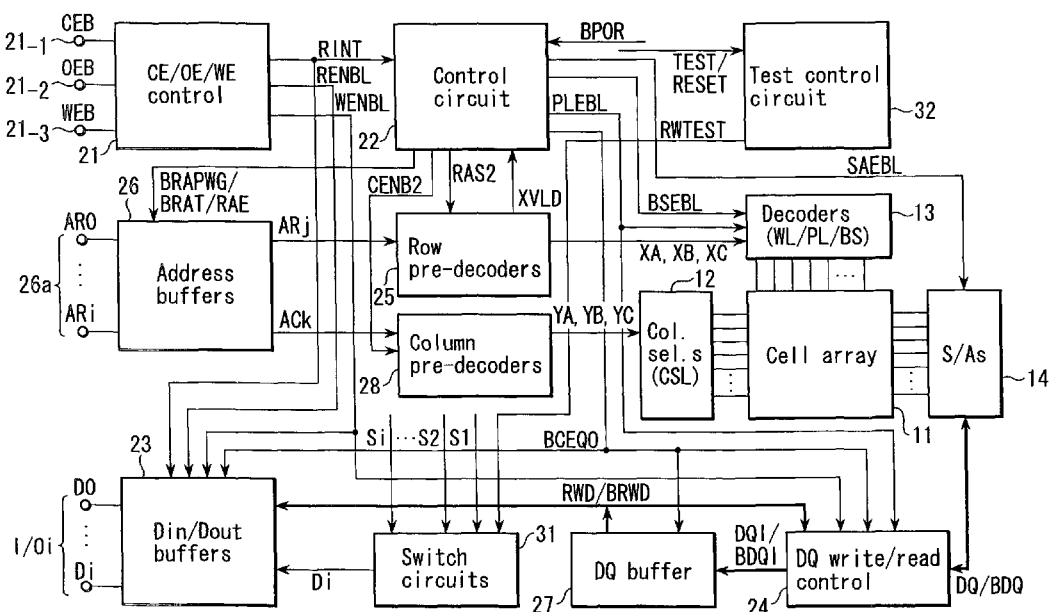
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(54) Title: SEMICONDUCTOR MEMORY DEVICE WITH TEST MODE TO MONITOR INTERNAL TIMING CONTROL SIGNALS AT I/O



(57) Abstract: A semiconductor memory device includes a memory cell array, a plurality of input/output terminals to input cell data written to the memory cell array and output cell data read from the memory cell array, a test mode setting circuit which sets a test mode to monitor a plurality of timing signals which control input/output operation timing of the cell data, and switch circuits connected to the plurality of input/output terminals. The switch circuits simultaneously output the plurality of timing signals from the plurality of input/output terminals in the test mode.



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