

What is Claimed is:

1. A method performed by at least one processor, the method comprising:

receiving a first video coding layer (VCL) network abstraction layer (NAL) unit of a first slice of a coded picture and a second VCL NAL unit of a second slice of the coded picture, the first VCL NAL unit having a first VCL NAL unit type and the second VCL NAL unit having a second VCL NAL unit type that is different from the first VCL NAL unit type; and

decoding the coded picture, the decoding comprising determining a picture type of the coded picture based on the first VCL NAL unit type of the first VCL NAL unit and the second VCL NAL unit type of the second VCL NAL unit, or based on an indicator, received by the at least one processor, indicating that the coded picture includes mixed VCL NAL unit types.
2. The method of claim 1, wherein

the determining comprises determining the coded picture is a trailing picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a trailing picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit contains an instantaneous decoding refresh (IDR) picture coded slice or a clean random access (CRA) picture coded slice.
3. The method of claim 1, wherein

the determining comprises determining the coded picture is a random access decodable leading (RADL) picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a RADL picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit contains an instantaneous decoding refresh (IDR) picture coded slice or a clean random access (CRA) picture coded slice.

4. The method of claim 1, wherein

the determining comprises determining the coded picture is a step-wise temporal sub-layer access (STSA) picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains an STSA picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit does not contain an instantaneous decoding refresh (IDR) picture coded slice.

5. The method of claim 1, wherein

the determining comprises determining the coded picture is a trailing picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a step-wise temporal sub-layer access (STSA) picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit does not contain a clean random access (CRA) picture coded slice.

6. The method of claim 1, wherein

the determining comprises determining the coded picture is a trailing picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a gradual decoding refresh (GDR) picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit does not contain an instantaneous decoding refresh (IDR) picture coded slice or a clean random access (CRA) picture coded slice.

7. The method of claim 1, wherein

the indicator is a flag, and

the determining comprises determining the coded picture is a trailing picture based on the flag indicating that the coded picture includes mixed VCL NAL unit types.

8. The method of any one of claims 1 to 6, wherein
the indicator is a flag, and
the decoding the coded picture further comprises determining a temporal ID of the coded picture is 0 based on the flag indicating that the coded picture includes mixed VCL NAL unit types.

9. The method of any one of claims 1 to 6, wherein,
the indicator is a flag, and
the method further comprises receiving the flag in a picture header or a slice header.

10. The method of any one of claims 1 to 6, wherein,
the indicator is a flag, and the coded picture is in a first layer, and
the method further comprises
receiving the flag; and
determining that an additional coded picture, that is in a second layer that is a reference layer of the first layer, includes mixed VCL NAL unit types based on the flag indicating the coded picture includes mixed VCL NAL unit types.

11. A system comprising:
memory configured to store computer program code; and
at least one processor configured to receive at least one coded video stream, access the computer program code, and operate as instructed by the computer program code, the computer program code comprising:
decoding code configured to cause the at least one processor to decode a coded picture from the at least one coded video stream, the decoding code comprising determining

code configured to cause the at least one processor to determine a picture type of the coded picture based on a first video coding layer (VCL) network abstraction layer (NAL) unit type of a first VCL NAL unit of a first slice of the coded picture, and a second VCL NAL unit type of a second VCL NAL unit of a second slice of the coded picture, or based on an indicator, received by the at least one processor, indicating that the coded picture includes mixed VCL NAL unit types,

wherein the first VCL NAL unit type is different from the second VCL NAL unit type.

12. The system of claim 11, wherein

the determining code is configured to cause the at least one processor to determine the coded picture is a trailing picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a trailing picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit contains an instantaneous decoding refresh (IDR) picture coded slice or a clean random access (CRA) picture coded slice.

13. The system of claim 11, wherein

the determining code is configured to cause the at least one processor to determine the coded picture is a random access decodable leading (RADL) picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a RADL picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit contains an instantaneous decoding refresh (IDR) picture coded slice or a clean random access (CRA) picture coded slice.

14. The system of claim 11, wherein

the determining code is configured to cause the at least one processor to determine the coded picture is a step-wise temporal sub-layer access (STSA) picture based on the first VCL

NAL unit type indicating the first VCL NAL unit contains an STSA picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit does not contain an instantaneous decoding refresh (IDR) picture coded slice.

15. The system of claim 11, wherein

the determining code is configured to cause the at least one processor to determine the coded picture is a trailing picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a step-wise temporal sub-layer access (STSA) picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit does not contain a clean random access (CRA) picture coded slice.

16. The system of claim 11, wherein

the determining code is configured to cause the at least one processor to determine the coded picture is a trailing picture based on the first VCL NAL unit type indicating the first VCL NAL unit contains a gradual decoding refresh (GDR) picture coded slice, and the second VCL NAL unit type indicating the second VCL NAL unit does not contain an instantaneous decoding refresh (IDR) picture coded slice or a clean random access (CRA) picture coded slice.

17. The system of claim 11, wherein

the indicator is a flag, and

the determining code is configured to cause the at least one processor to determine the coded picture is a trailing picture based on the flag indicating that the coded picture includes mixed VCL NAL unit types.

18. The system of any one of claims 11 to 16, wherein

the indicator is a flag, and

the determining code is further configured to cause the at least one processor to determine that a temporal ID of the coded picture is 0 based on the flag indicating that the coded picture includes mixed VCL NAL unit types.

19. The system of any one of claims 11 to 16, wherein,

the indicator is a flag, and

the at least one processor is configured to receive the flag in a picture header or a slice header.

20. A computer-readable medium storing computer instructions that, when executed by at least one processor, cause the at least one processor to execute the method of any one of claims 1 to 10.