Claims

What is Claimed is :

1. A display having an active area from which light is emitted and an inactive area that does not emit light, comprising:

an array of pixels;

display driver circuitry;

a first set of signal lines coupled to the display driver circuitry, wherein the first set of signal lines extend in a first direction;

a second set of signal lines coupled to the display driver circuitry, wherein the second set of signal lines extend in a second direction that is perpendicular to the first direction, wherein the second set of signal lines include first and second signal lines, wherein the first signal line is coupled to a first pixel row, and wherein the second signal line is coupled to a second pixel row having more pixels than the first pixel row;

a supplemental signal line loading structure in the inactive area of the display, wherein the supplemental signal line loading structure increases loading on the first signal line; and

a bias voltage supply line that biases the supplemental signal line loading structure.

2. The display defined in claim 1 wherein the first set of signal lines comprises data lines and the second set of signal lines comprises gate lines.

3. The display defined in claim 2 further comprising a transparent conductive layer that overlaps the doped polysilicon.

4. The display defined in claim 3 further comprising a via that electrically couples the transparent conductive layer to the doped polysilicon.

5. The display defined in claim 4 wherein the transparent conductive layer is

coupled to the bias voltage supply line.

6. The display defined in claim 5 wherein the bias voltage supply line comprises multiple metal layers.

7. The display defined in claim 5 wherein the doped polysilicon has an H-shape with two vertical segments connected by a horizontal segment.

8. The display defined in claim 7 wherein the via is coupled to the horizontal segment.

9. The display defined in claim 8 wherein the two vertical segments overlap the first signal line.

10. The display defined in claim 3 wherein the pixels comprise a common voltage layer, and wherein the transparent conductive layer is formed from the same material as the common voltage layer.

11. The display defined in claim 10 wherein the pixels comprise transistors with polysilicon channels, and wherein the doped polysilicon is formed from the same material as the polysilicon channels.

12. The display defined in claim 1 wherein the second set of signal lines includes a third signal line coupled to fewer pixels than the second signal line, wherein the supplemental signal line loading structure increases loading on the third signal line.

13. The display defined in claim 1 wherein some of the signal lines in the first set of signal lines overlap the first signal line in the inactive area of the display.

14. The display defined in claim 1 further comprising a metal layer that electrically couples the supplemental signal line loading structures to the bias voltage supply line.

15. The display defined in claim 14 further wherein the metal layer is formed from the same material as the first set of signal lines.

16. A display having an active area and an inactive area, comprising:

an array of pixels in the active area, wherein the array of pixels includes first and second rows and wherein the first row has fewer pixels than the second row;

gate lines coupled to the array of pixels, wherein the gate lines include a first gate line coupled to the first row of pixels and a second gate line coupled to the second row of pixels, and wherein the first gate line has a segment in the inactive area;

dummy pixels in the inactive area that do not emit light, wherein the dummy pixels comprise doped polysilicon that overlaps the segment of the first gate line in the inactive area; and

a metal layer that electrically couples the dummy pixels to a bias voltage supply line.

17. The display defined in claim 16 further comprising data lines coupled to the array of pixels, wherein the metal layer is formed from the same material as the data lines.

18. The display defined in claim 17 wherein the dummy pixels comprise extended portions of the data lines.

19. A display having an active area and an inactive area, comprising;

an array of pixels in the active area;

a common voltage layer comprising row electrodes and column electrodes, wherein the common voltage layer is configured to serve as a ground plane for the array of pixels

in a first mode and to gather touch data in a second mode;

rows of signal lines respectively coupled to the row electrodes, wherein the rows of signal lines include first and second signal lines, and wherein the first signal line is coupled to fewer row electrodes than the second signal line; and

a conductive layer in the inactive area that overlaps the first signal line to increase loading on the first signal line.

20. The display defined in claim 19 wherein the conductive layer comprises indium tin oxide, the display further comprising:

gate lines coupled to the array of pixels, wherein the gate lines include first and second gate lines, wherein the first gate line is coupled to fewer pixels than the second gate line, and wherein the first gate line overlaps the conductive layer in the inactive area; and

gate line loading structures in the inactive area of the display that increase loading on the first gate line, wherein the gate line loading structures include data lines and doped polysilicon that overlap the first gate line in the inactive area.