

SYNCHRONOUS RECTIFIER TYPE SWITCHING CONVERTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001]

The present invention relates to a synchronous rectifier type switching converter using FETs as rectification devices on a secondary side of a transformer, and particularly, to a control circuit for the same.

2. Description of the Related Art

[0002]

Among switching converters in which a switching circuit is connected to a primary side of a transformer and a rectification circuit is connected to a secondary side thereof, there is a synchronous rectifier type switching converter that uses FETs in the rectifying circuit. Because ON-state resistances of FETs are lower as compared with conduction resistances of diodes, this synchronous rectifier type switching converter has an advantage of reduced heat loss and increased efficiency.

[0003]

Fig. 1 is a schematic circuit diagram of the synchronous rectifier type switching converter.

[0004]

To a primary side of a transformer Tr, a switching circuit (for example, a 2-transistor forward switching circuit) containing FET

devices Q1, Q2 is connected; and to a secondary side of the transformer Tr, two FET devices Q3, Q4 are connected. A first FET device Q3 is a FET device on a rectification side, and a second FET device Q4 is a FET device on a reflux side. Through ON-OFF operations of the first and the second FET devices Q3, Q4 in place of conventional diodes, power to a load side is supplied. To the load side of these FET devices Q3, Q4, a smoothing circuit consisting of a reactor L and a capacitor C is connected; and to the reactor L, a reactor current detection sensor SH is connected in series. An output from the current detection sensor SH is fed back to a control portion. The above-mentioned output from the current detection sensor SH determines ON-OFF timings of the FET devices Q1, Q2 for a constant-current control. Also, the above-mentioned output from the current detection sensor SH determines ON-OFF timings of the FET devices Q3, Q4 for a synchronous rectification.

[0005]

Fig. 2 shows a partial timing chart of the above-mentioned converter.

[0006]

$V(Q3)$ is an end-to-end voltage of the FET device Q3. $V(Q4)$ is an end-to-end voltage of the FET device Q4. I is a reactor current flowing in the reactor L.

[0007]

In a state where a load has a fixed magnitude, when a positive voltage is produced on the secondary side of the transformer Tr, a current flows in direction of the secondary side of the transformer Tr →

reactor L $\rightarrow$ capacitor C $\rightarrow$ FET device Q3 $\rightarrow$ secondary side of the transformer Tr. Also, when a negative voltage is produced on the secondary side of the transformer Tr, a reflux current flows in direction of the reactor L $\rightarrow$ capacitor C $\rightarrow$ FET device Q4 $\rightarrow$ reactor L. The FET devices Q3, Q4 undergo ON-OFF controls in synchronization with the above-mentioned current cycles. When the FET devices Q3, Q4 are turned on, their ON-state resistances are smaller than the conduction resistances of the diodes. Therefore, loss decreases, and as a result, efficiency increases.

[0008]

The reactor current exhibits a waveform as shown in Fig. 2 that contains ripples arising from the switching. When the reactor current decreases to become near zero as the load becomes a state of a light load or no load, the reactor current becomes a discontinuous current polarity of which changes. The discontinuous current is indicated by P in Fig. 2. At this time, if the FET device Q4 is turned off at a timing when the reactor current becomes negative, that is, at a timing when the current flows in direction of the reactor L $\rightarrow$ FET device Q4 $\rightarrow$ capacitor C $\rightarrow$ reactor L, a problem arises. That is, an excessive surge voltage V_s is generated between both ends of the FET device Q4 due to the energy stored in the reactor L, which results in destruction of the FET device Q4.

[0009]

On this account, among conventional synchronous rectifier type switching converters, there is proposed one in which in order for

the current not to flow in direction of the reactor $L \rightarrow$ FET device $Q4 \rightarrow$ capacitor $C \rightarrow$ reactor L a diode is connected to this current path in series (JP H11-146650 A). This circuit solves the above-mentioned problem since the current does not flow in direction of the reactor $L \rightarrow$ FET device $Q4 \rightarrow$ capacitor $C \rightarrow$ reactor L .

SUMMARY OF THE INVENTION

[0011]

However, as in the above-mentioned prior art example, in the circuit where a diode is connected in order for the reactor current not to flow in reverse direction through the FET device on the reflux side, loss at the diode becomes non-trivial enough to offset the advantage of using the FET devices $Q3$, $Q4$ to increase efficiency.

[0012]

The present invention is directed to providing a synchronous rectifier type switching converter that can maintain high efficiency while preventing surge voltages from occurring at a FET device at the time of light load or no load when rapid load fluctuations occur.

[0013]

A synchronous rectifier type switching converter of the present invention is a synchronous rectifier type switching converter including: a transformer; a switching circuit that is connected to a primary side of the transformer and performs switching of a DC power supply; a synchronous rectification circuit containing synchronous

rectification devices that consist of a rectification side FET device connected to a secondary side of the transformer in series and a reflux side FET device connected to the secondary side of the transformer in parallel; a smoothing circuit consisting of a reactor and a capacitor that are connected to an output side of the synchronous rectification circuit; a detection sensor that detects current of the reactor; and a control circuit that performs ON-OFF controls of the switching circuit, the rectification side FET device and the reflux side FET device at each sampling timing based on detection values of the detection sensor.

The control circuit includes:

a gate blocking means that, through comparison of a detection value of the detection sensor with a predetermined threshold value, outputs a gate blocking signal to stop operations of the synchronous rectification devices when the detection value becomes not greater than the threshold value; and

a correction means that, upon detecting that decrease of the reactor current is not less than a fixed level based on the detection value of the detection sensor, corrects either a present time sampling detection value of the detection sensor or the predetermined threshold value, referring to history of the detection values of the detection sensor when the gate blocking means compares the present time sampling detection value of the detection sensor with the predetermined threshold value.

[0014]

In the case where the correction means corrects the detection value of the detection sensor, the gate blocking means compares the detection value that has been corrected by the correction means with the threshold value. Also, in the case where the correction means corrects the predetermined threshold value, the gate blocking means compares the threshold value that has been corrected by the correction means with the present time sampling detection value.

[0015]

The gate blocking signal is a signal that acts as a force to stop operations of the synchronous rectification devices and is output immediately when it is detected that either the detection value of the detection sensor or the detection value that has been corrected by the correction means is below the predetermined threshold value. It is a signal to prevent the reactor current from flowing in reverse direction, that is, in direction of the reactor → reflux side FET device (FET device Q4) → capacitor → reactor when a state of light load or no load occurs, and is output from the control portion to gates of the synchronous rectification devices. When the reactor current is about to flow in reverse direction, the gate blocking signal is output to force the operations of the synchronous rectification devices to stop, thereby preventing the reflux side FET device from being destroyed by an excessive surge voltage.

[0016]

In the present invention, while the above-mentioned control portion performs the control at each sampling timing in digital processing,

the correction means corrects the present time sampling detection value of the reactor current referring to the history containing a last time sampling detection value. Otherwise, the correction means corrects the threshold value. The correction is to compensate for first-order delays in a feedback system containing the detection sensor, and this causes a difference between the present time sampling detection value and the threshold value to become close to a real value (difference). As a result, at the time of rapid decrease of the reactor current, the detection value that has been corrected can pass across the threshold value with an earlier timing, and this results in the ability to output the gate blocking signal earlier as compared with the case where the detection value is not corrected.

[0017]

Because timings to stop operations of the synchronous rectification devices are quickened as the gate blocking signal is output earlier, it is possible to stop the operations of the synchronous rectification devices before the reactor current decreases to become near zero. As a result, it no longer occurs that the reactor current flows in reverse direction through the reflux side FET device, and thus it is made possible to prevent the excessive surge voltage V_s from being applied to the reflux side FET device (device Q4). Also, instead of correcting the present time sampling detection value, the threshold value may be corrected.

[0018]

Further, fixing the threshold value at a high value so as to cause

the gate blocking signal to be output earlier also makes it possible to prevent the excessive surge voltage V_s from being applied to the reflux side FET device (FET device Q4). However, such a procedure would give rise to a monotonous control regardless of gradients of the current changes at the time when the reactor current decreases. This would result in the reduction of an output current range that can be synchronously rectified for a given overall output current range of the switching converter, which would not be desirable from the viewpoint of increasing efficiency. The present invention has an advantage of capability to prevent the occurrence of an excessive surge voltage V_s without resort to the threshold value set to a high value.

[0019]

The present invention makes it possible to achieve a high efficiency converter while preventing destruction of a reflux side FET device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020]

Fig. 1 is a circuit diagram of a conventional synchronous rectifier type switching converter.

Fig. 2 shows a partial timing chart of the above-mentioned converter.

Fig. 3 is a circuit diagram of a synchronous rectifier type switching converter according to an embodiment of the present invention.

Fig. 4 shows ON-OFF timings of gate signals G1-G4 of the

above-mentioned converter.

Fig. 5 shows a partial timing chart of the above-mentioned converter.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021]

Fig. 3 is a circuit diagram of a synchronous rectifier type switching converter according to an embodiment of the present invention.

[0022]

To a primary side of a transformer Tr, a 2-transistor forward switching circuit 2 containing FET devices Q1, Q2 is connected; and to a secondary side of the transformer Tr, a synchronous rectification circuit 3 consisting of two FET devices Q3, Q4 is connected. A first FET device Q3 of the synchronous rectification circuit 3 is a FET device on a rectification side, and a second FET device Q4 is a FET device on a reflux side. Through ON-OFF operations of the first and the second FET devices Q3, Q4 in place of conventional diodes, rectified power is supplied to a load side. To the load side of these FET devices Q3, Q4, a smoothing circuit consisting of a reactor L and a capacitor C is connected; to the reactor L, a current detection sensor SH for reactor current is connected in series; and output from the current detection sensor SH is fed back to a control portion 1. For the purpose of performing a constant-current control and a synchronous rectification, the output from the current detection sensor SH is used to determine ON-OFF timings of the FET devices Q1-Q4.

[0023]

The control portion 1 includes: a reactor current detection circuit 10 that detects a magnitude and a direction of the reactor current; a primary side gate drive circuit 11 that supplies gate drive pulses G1, G2 to the switching circuit 2 containing the FET devices Q1, Q2; a synchronous rectification gate drive circuit 12 that supplies gate drive pulses G3, G4 to the synchronous rectification circuit 3 consisting of the FET devices Q3, Q4; and a CPU 13 that performs, based on a reactor current detection value, a constant-current control of the converter, as well as a synchronous rectification control and/or an operation stop control of the synchronous rectification circuit 3. Further, the gate drive pulses G3, G4 are embodied in such a manner as to be output through a gate circuit 14, and the gate drive pulses G3, G4 are turned off with this gate circuit 14 when a below-mentioned gate blocking signal GB is generated.

[0024]

Fig. 4 shows ON-OFF timings of the gate signals G1-G4 of the FET devices Q1-Q4, and the gate blocking signal GB of the above-mentioned converter. Moreover, Fig. 5 shows a partial timing chart of the above-mentioned converter. $V(Q3)$ is an end-to-end voltage of the FET device Q3; $V(Q4)$ is an end-to-end voltage of the FET device Q4; and D is defined, based on detection values of the reactor current flowing in the reactor L that are detected within a fixed sampling period, as a locus consisting of straight lines interpolating adjacent detection values that are serially sampled (the reactor current itself is like one containing ripples as shown in Fig. 2). Further, S is

a threshold value at which the gate blocking signal GB is output in order to cause the operations of the FET devices Q3, Q4 to stop.

[0025]

The FET devices Q1, Q2 undergo ON-OFF drives at the same timing with each other, caused by the gate drive signals G1, G2 from the primary side gate drive circuit 11. The CPU 13 monitors the reactor current detection value, and outputs the gate drive signals G1, G2 that are PWM-controlled so that the reactor current becomes a constant current. Also, to the FET devices Q3, Q4, the gate drive signals G3, G4 are supplied, respectively, in synchronization with the gate drive signals G1, G2.

[0026]

Subsequently, operations are explained.

[0027]

In a state where a load has a fixed magnitude, when a positive voltage is produced on the secondary side of the transformer Tr with the FET devices Q1, Q2 of the switching circuit 2 on the primary side being turned on, a current flows through a path of the secondary side of the transformer Tr → reactor L → capacitor C → FET device Q3 → secondary side of the transformer Tr. The CPU 13 determines a time period (forward current period) at which the reactor current flows in this direction at the time of positive voltage, and turns on the gate drive signal G3. Also, when a negative voltage is produced on the secondary side of the transformer Tr, a reflux current flows through a path of the reactor L → capacitor C (C1, C2) → FET device Q4 → reactor

L, due to the energy stored in the reactor L. The CPU 13 determines a time period (reflux current period) at which the reflux current flows, and turns on the gate drive signal G4. With this cycle being repeated, ON-OFF controls of the FET devices Q1, Q2 are performed so as to achieve a constant current; ON-OFF controls of the FET devices Q3, Q4 are performed so as to achieve a synchronous rectification; and thereby the energy inputted from the primary side of the transformer Tr is supplied to the load with high efficiency.

[0028]

With the above-mentioned circuit, because ON-state resistances at the time when the FET devices Q3, Q4 are turned on are lower than conduction resistances of diodes, loss is reduced as compared with diode-based rectification circuits where diodes are connected simply in place of the FET devices Q3, Q4, and this results in increased efficiency.

[0029]

Further, a dead time dt is provided between each gate drive signal G1 (G2), G3, G4 as shown in Fig.4, thereby preventing respective FET devices from being turned on at the same time.

[0030]

Additionally, a detection signal output from the reactor current detection sensor SH is detected by the CPU 13. Here, designating present time sampling detection value by $a(n)$ and last time sampling detection value by $a(n-1)$, respectively, among detection values, a deviation δ is calculated for each detection value at each sampling.

If $a(n) < a(n-1)$ (when the reactor current decreases), determination is made as to whether or not the deviation δ (absolute value) indicating a difference between the present time sampling detection value and the last time sampling detection value is not greater than a fixed value. If the deviation δ is smaller than the fixed value, it is a case where an average current of the reactor is slowly decreasing. In that case, the present time sampling detection value $a(n)$ is directly compared with the threshold value S , and when the present time sampling detection value $a(n)$ becomes not greater than the threshold value S , the FET device Q4 is turned off with the gate blocking signal GB. Herewith, it is possible to stop the synchronous rectification devices before the negative reflux current flows, in the state of which the reactor current becomes discontinuous. In this manner, for the slow decrease of the reactor current, since the determination as to whether or not the gate blocking signal is output is made by comparing the present time sampling detection value $a(n)$ which is the latest detection value as it is with the threshold value S , there is no occurrence of stopping the synchronous rectification circuit on the secondary side of the transformer Tr too sensitively, nor occurrence of hindering thereby efficiency increase. Additionally, the threshold value S is generally set to a value not less than widths of the ripple components of the reactor current that are shown in Fig. 2.

[0031]

Subsequently, operations in a cases where the load rapidly becomes

light or a state of no load.

[0032]

As shown in Fig. 5, when the load fluctuates to the state of light load or no load, the reactor current detection value rapidly approaches zero as indicated by D1; then, at this time, the entire control circuit behaves as follows.

[0033]

In Fig. 5, D2 denotes an actual change of the reactor current detection value, and D1 shows a change of the reactor current detection value detected by the CPU 13. That is to say, because there are first-order delays for the signal processing in the reactor current detection sensor SH and in the reactor current detection circuit 10, D1 exhibits a time delay characteristic, due to these delays, as compared with D2. On account of this delay, the CPU 13 performs an ON-OFF control of the gate drive signals G3, G4 based on D1. While the detection of the reactor current is performed for each predetermined sampling period, in the case where the load gradually changes and thereby the reactor current slowly decreases, since its change is small, the reactor current detection value D can detect an average value of the reactor current almost exactly.

[0034]

In such a situation, as mentioned as a problem in the explanation of operations of the converter in Fig. 2, if the ON-OFF controls of the gate drive signals G3, G4 are performed based on D1 when the reactor current I rapidly decreases as in the diagram, it follows that the

gate blocking signal GB is output at the timing t1 of the sampling detection value a4 by the CPU 13. Then, because the negative reactor current has already been flowing (reflux current in reverse direction flows) at t1 due to the delay of detection, if at this state the FET device Q4 is turned off with the gate blocking signal GB, it is inevitable that an excessive surge voltage Vs is generated between both ends of the FET device Q4. This is due to the fact that for a control under load fluctuations the first-order delay of the control system caused by the reactor current detection sensor SH and the reactor current detection circuit 10 is large to the extent that it cannot be ignored.

[0035]

Further, Fig.5 is a depiction that is expressed with an expanded time axis, and thus the above-mentioned case where the reactor current decreases slowly to become not greater than the threshold value S is materially different from the situation depicted in Fig. 5. That is to say, the detection value D in that case would be depicted as a line changing above the threshold value S in Fig. 5 nearly in parallel therewith, gradually coming below the threshold value S, and then changing below the threshold value S nearly in parallel therewith again. In other words, if it were tried to depict the above-mentioned slow change in Fig. 5, the time axes for change are so different from each other that the detection value D would be depicted overlapping with the threshold value S. Therefore, in the case of slow decrease of the reactor current, it is sufficient to turn off the FET devices

Q3, Q4 at a timing when the sampling detection value $a(n)$ comes below the threshold value S , and thereby the problematic operation mode where the reactor current flows as a negative reflux current can be avoided.

[0036]

In the converter according to this embodiment, the CPU 13 is provided with a correction means to correct the reactor current detection value when a rapid decrease of the reactor current is detected. This correction is to be made through the operation of the CPU 13.

[0037]

That is, in Fig. 5, assuming that the present time sampling detection value is a_3 , in the case of $a_2 > a_3$ (when the reactor current decreases), if the deviation δ from the last time sampling detection value a_2 is not less than a fixed value, an operation process to correct the present time sampling detection value is performed. If a corrected detection value is given by $b(n)$, it is expressed as $b(n) = a(n) - \delta$, and then using this corrected detection value $b(n)$, the comparison with the threshold value S is made. Then, when the corrected detection value $b(n)$ becomes not greater than the threshold value S , the gate blocking signal GB is output. As stated above, calculation of the deviation δ is performed for each sampling period, and if the deviation δ becomes not less than a fixed value, that is, if a change in which a width of decrease of the reactor current becomes not less than a fixed value is detected, the correction operation to output the gate blocking signal GB is performed.

[0038]

In Fig. 5, the deviation δ which is the difference between a_3 and a_2 is calculated, and determination is made as to whether or not the deviation δ is not less than the fixed value. If the deviation δ is not less than the fixed value, a_3 is corrected to b_3 ($= a_3 - \delta$), and the corrected detection value b_3 is compared with the threshold value S . Then, when this becomes not greater than the threshold value, the gate blocking signal GB is generated to turn off the FET devices Q3, Q4. Accordingly, it follows that the gate blocking signal GB is generated at the sampling timing t_2 of the sampling detection value a_3 before the time t_1 when the negative reactor current starts to flow, so that it is possible to stop operations of the FET devices Q3, Q4 before the negative reflux current flows on the secondary side of the transformer Tr.

[0039]

Because the deviation δ becomes greater as the detection value D_1 becomes steeper in terms of slope, the timing at which the gate blocking signal GB is generated becomes even earlier.

[0040]

In the above-mentioned example, in order to calculate the correction value of a_3 , the deviation δ from the last time sampling detection value is used as a value to be subtracted; however, the deviation δ may be multiplied by a coefficient, for example, like multiplying the deviation δ by 2. By so doing, the timing of generating the gate blocking signal GB may be made even earlier, which may result in

increased responsiveness. Also, a deviation from an average value of a plurality of previous sampling detection values may be used as the value to be subtracted, and the number of previous samplings to be used for averaging may be changed depending on the slope of D1. Otherwise, various ways of historical reference may be possible. Additionally, it is necessary for the gate blocking signal GB to be output to both of the FET devices Q3, Q4, and thus to cause both thereof to stop their operations. As to how to perform the correction, adequate solution(s) thereto should be empirically determined so as not to generate an excess surge voltage V_g between both ends of the FET device Q4, and so as not to result in a too sensitive correction control.

[0041]

Further, as another embodiment, a correction means may be such that the threshold value S is corrected based on the deviation δ . In the example shown in Fig. 5, instead of making the correction as $a_3 - \delta$, the threshold value S is corrected to $S + \delta$. In this manner, the threshold value S can be dynamically corrected.

[0042]

When the load returns from the state of light load or no load to normal load, the reactor current starts to flow, so that the magnitude thereof exceeds the threshold value S ; however, then, since the gate blocking signal GB is also turned off, rectification operations by the FET device Q3, Q4 are resumed.

[0043]

Moreover, while it is possible to achieve an earlier timing (for example, from t_1 to t_2) of generating the gate blocking signal GB when the load condition changes rapidly also by setting the value of the threshold value S to a high fixed value, setting the threshold value S at a high fixed value results in having a too early timing of generating the gate blocking signal GB when the change is slow at the time of decrease of the reactor current. As a result, an overall period capable of synchronous rectification is shortened, and thus efficiency decreases. In contrast, with this embodiment, since the timing of generating the gate blocking signal GB dynamically changes depending on the pace of change when the reactor current decreases, it never occurs that the overall domain or range capable of synchronous rectification is reduced.

WHAT IS CLAIMED IS:

1. A synchronous rectifier type switching converter comprising:
a transformer; a switching circuit that is connected to a primary side of the transformer and performs switching of a DC power supply;
a synchronous rectification circuit containing synchronous rectification devices that consist of a rectification side FET device connected to a secondary side of the transformer in series and a reflux side FET device connected to the secondary side of the transformer in parallel; a smoothing circuit consisting of a reactor and a capacitor that are connected to an output side of the synchronous rectification circuit; a detection sensor that detects current of the reactor; and a control circuit that performs ON-OFF controls of the switching circuit, the rectification side FET device and the reflux side FET device at each sampling timing based on detection values of the detection sensor, wherein

the control circuit comprises:

a gate blocking means that, through comparison of a detection value of the detection sensor with a predetermined threshold value, outputs a gate blocking signal to stop operations of the synchronous rectification devices when the detection value becomes not greater than the threshold value; and

a correction means that, upon detecting that decrease of the reactor current is not less than a predetermined level based on the detection value of the detection sensor, corrects either a present time sampling

detection value of the detection sensor or the predetermined threshold value, referring to history of the detection values of the detection sensor when the gate blocking means compares the present time sampling detection value of the detection sensor with the threshold value.

2. The synchronous rectifier type switching converter according to claim 1, wherein

the correction means, when a deviation of the present time sampling detection value from a last time sampling detection value is not less than a fixed value, corrects the present time sampling detection value using the deviation; and

the gate blocking means compares the corrected present time sampling detection value with the predetermined threshold value.

3. The synchronous rectifier type switching converter according to claim 1, wherein

the correction means, when a deviation of the present time sampling detection value from a last time sampling detection value is not less than a fixed value, corrects the predetermined threshold value using the deviation; and

the gate blocking means compares the present time sampling detection value with the corrected threshold value.

4. The synchronous rectifier type switching converter according to claim 2 or 3, wherein

the correction means lets the deviation of the present time sampling detection value from the last time sampling detection value be a value obtained from multiplying said deviation by a constant coefficient.