WHAT IS CLAIMED IS:

1. An electronic device comprising a semiconductor memory, the semiconductor memory comprising:

variable resistance layers and insulating layers alternately stacked;

conductive pillars passing through the variable resistance layers and the insulating layers;

a slit insulating layer passing through the insulating layers and extending in a first direction;

conductive layers interposed between the slit insulating layer and the variable resistance layers; and

electrode layers disposed between the conductive layers and the variable resistance layers, and between the conductive layers and the insulating layers,

wherein the variable resistance layers are configured to remain in an amorphous state during a program operation.

2. The electronic device according to claim 1, wherein each of the insulating layers comprises protrusions protruding compared to a corresponding one of the variable resistance layers in a cross-sectional view, and the conductive layers are alternately stacked with the protrusions.

3. The electronic device according to claim 1, wherein each of the variable resistance layers encloses sidewalls of the conductive pillars and extends in the first direction.

4. The electronic device according to claim 1, wherein a portion of each of the variable resistance layers is interposed between a pair of the conductive pillars disposed adjacent to each other in the first direction.

5. The electronic device according to claim 1, wherein each of the variable resistance layers is interposed between a pair of the conductive layers disposed adjacent to each other in a second direction intersecting with the first direction.

6. The electronic device according to claim 1, wherein the variable resistance layers include amorphous chalcogenide.

7. The electronic device according to claim 1, wherein memory cells are disposed in respective areas in which the conductive pillars intersect with the conductive layers.

8. The electronic device according to claim 1, further comprising phase-change layers interposed between the variable resistance layers and the conductive layers, respectively.

9. An electronic device comprising a semiconductor memory, the semiconductor memory comprising:

insulating layers stacked;

first variable resistance layers alternately stacked with the insulating layers and each extending in a first direction;

vertical bit lines passing through the first variable resistance layers and the insulating layers;

a first slit insulating layer passing through the insulating layers and extending in the first direction;

a second slit insulating layer passing through the insulating layers and extending in the first direction;

first word lines each interposed between the first slit insulating layer and each of the first variable resistance layers;

second word lines each interposed between the second slit insulating layer and each of the first variable resistance layers;

first electrode layers disposed between the first word lines and the first variable resistance layers, and between the first word lines and the insulating layers; and

second electrode layers disposed between the second word lines and the first variable resistance layers, and between the second word lines and the insulating layers,

wherein first memory cells are respectively disposed between the vertical bit lines and the first word lines, second memory cells are respectively disposed between the vertical bit lines and the second word lines, and each of the first memory cells and each of the second memory cells are disposed adjacent in a second direction and share a corresponding one of the first variable resistance layers.

10. The electronic device according to claim 9, wherein a portion of each of the first variable resistance layers fills spaces defined between a pair of the vertical bit lines disposed adjacent to each other in the first direction.

11. The electronic device according to claim 9, wherein the first variable resistance layers remain in an amorphous state during a program operation.

12. The electronic device according to claim 9, further comprising second variable resistance layers include a first plurality of second variable resistance layers and a second plurality of second variable resistance layers, the first plurality of second variable resistance layers being respectively interposed between the first variable resistance layers and the first word lines, the second plurality of second variable resistance layers being respectively disposed between the first variable resistance layers and the second word lines.

13. The electronic device according to claim 12, wherein the first and second electrode layers are interposed between the first variable resistance layers and the second variable resistance layers.

14. The electronic device according to claim 12, wherein, during a

program operation, the first variable resistance layers are configured to remain in an amorphous state, and the second variable resistance layers are configured to change in phase.

15. The electronic device according to claim 12, wherein each of the first memory cells includes a corresponding one of the first plurality of second variable resistance layers and each of the second memory cells includes a corresponding one of the second plurality of second variable resistance layers.

16. A method of manufacturing an electronic device including a semiconductor memory, the method comprising:

alternately forming first variable resistance layers and insulating layers;

forming conductive pillars passing through the first variable resistance layers and the insulating layers;

forming a slit passing through the first variable resistance layers and the insulating layers and extending in a first direction;

forming openings by etching the first variable resistance layers exposed through the slit;

forming electrode layers in the respective openings; and

forming conductive layers in the respective openings,

wherein the electrode layers are disposed between the conductive layers and the first variable resistance layers, and between the conductive

layers and the insulating layers.

17. The method according to claim 16, further comprising forming a slit insulating layer in the slit after forming the conductive layers.

18. The method according to claim 16, wherein the first variable resistance layers include amorphous chalcogenide.

19. The method according to claim 16, further comprising forming second variable resistance layers in the openings before forming the conductive layers.

20. The method according to claim 19, wherein the first variable resistance layers include amorphous chalcogenide, and the second variable resistance layers include phase-change material.