

SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001] The present disclosure relates to the technical field of semiconductors, and more particularly to a semiconductor structure and a semiconductor device.

BACKGROUND

[0002] With the rapid development of semiconductor technology, as a modern electronic information industry, the complementary metal-oxide-semiconductor (CMOS) integrated circuits scale is increasing. The main reason is the continual reduction of the characteristic size of the CMOS device, and the most advanced 5 nm semiconductor process has been in mass production. However, with the continuous improvement in integration, the continuous increase in power consumption of an integrated circuit chip has become a difficult problem for the development of integrated circuits.

[0003] The short channel effect (SCE) is an important factor besides the higher requirements for manufacturing process accuracy. The short channel effects are effects that occur in the transistor in a case where the conducted channel length of the metal oxide semiconductor field effect transistor is reduced to the order of tens of nanometers or even a few nanometers. The short channel effect mainly includes threshold voltage decreasing with the channel length, drain-induced barrier lowering, carrier surface scattering, velocity saturation effect, and so on. The existence of the short channel effect makes the characteristic size of the semiconductor device can not be further reduced. To reduce the short channel effect, currently, the industry has adopted special device structures, for example, under the 14 nm node, a fin field-effect transistor (FinFET) and an all-envelop gate field-effect transistor are provided, under the 5 nm node, a gate-all-around transistor (GAA) device is provided to improve the impact of the short channel effect on the device. Currently, the GAA device is applied more widely, while the PN junction is still in the GAA device, that is, problems such as doping diffusion remain, which limits the size of the device. Moreover, as a surface channel device, the GAA device has problems such as surface mobility and the hot carrier effect.

[0004] Therefore, a semiconductor device that can further break through the characteristic size is urgently needed.

SUMMARY

[0005] To solve the above-described problems, a semiconductor structure and a semiconductor device are provided by the embodiment of the present disclosure.

[0006] The first aspect of the embodiment of the present disclosure provides a semiconductor structure at least comprising:

[0007] a gate structure region; and

[0008] a source region and a drain region disposed on two sides of the gate structure respectively; where the gate structure region at least comprises:

[0009] a channel region and a gate region disposed from inside to outside; where the channel region is surrounded by the inner cavity of the gate region and attached to the source region, the drain region, and the gate region, an ion doping type of the drain region, an ion doping type of the source region and an ion doping type of the channel region are the same.

[0010] In an alternative embodiment of the present disclosure, the gate structure region further comprises:

[0011] a dielectric layer disposed between the gate region and the channel region, and attached to the gate region, the channel region, the drain region, and the source region.

[0012] In an alternative embodiment of the present disclosure, the gate structure region further comprises:

[0013] a buffer isolation region disposed between the channel region and the dielectric layer, and attached to the dielectric layer, the channel region, the drain region, and the source region.

[0014] In an alternative embodiment of the present disclosure, an ion doping concentration of the buffer isolation region is not larger than $1e17 / \text{cm}^3$.

[0015] In an alternative embodiment of the present disclosure, the ion doping concentration of the buffer isolation region is less than an ion doping concentration of the drain region and an ion doping concentration of the source region; and/or, the ion doping concentration of the buffer isolation region is one order of magnitude less than the ion doping concentration of the channel region.

[0016] In an alternative embodiment of the present disclosure, a thickness of the buffer isolation region ranges from 0.3 nm to 5 nm.

[0017] In an alternative embodiment of the present disclosure, an ion doping concentration of the gate region ranges from $1e16 / \text{cm}^3$ to $1e20 / \text{cm}^3$; and/or, the ion doping concentration of the channel region ranges from $1e17 / \text{cm}^3$ to $5e19 / \text{cm}^3$; and/or, the ion doping concentration of the drain region and the ion doping concentration of the source region range from $1e18 / \text{cm}^3$ to $5e20 / \text{cm}^3$.

[0018] In an alternative embodiment of the present disclosure, the ion doping concentration of the drain region, the ion doping concentration of the source region, and the ion doping concentration of the channel region are equal.

[0019] In an alternative embodiment of the present disclosure, the ion doping concentration of the drain region, the ion doping concentration of the source region, and the ion doping concentration of the channel region are not less than $1e17 / \text{cm}^3$.

[0020] In an alternative embodiment of the present disclosure, the drain region, the source region,

and the channel region are made integrally.

[0021] In an alternative embodiment of the present disclosure, the semiconductor structure is an N-type device and the gate region is a metal having a metal working function ranging from 4.5 eV to 5.2 eV; or

[0022] the semiconductor structure is a P-type device and the gate region is a metal having a metal working function ranging from 4.0 eV to 4.5 eV.

[0023] In an alternative embodiment of the present disclosure, the semiconductor structure is a FinFET device or a GAA device.

[0024] The second aspect of the embodiment of the present disclosure provides a semiconductor device comprising:

[0025] any one of the semiconductor structures as described above.

[0026] In an alternative embodiment of the present disclosure, the number of the semiconductor structures is a plurality, and the conduction type of the plurality of the semiconductor structures is not identical.

[0027] In an alternative embodiment of the present disclosure, a first semiconductor structure and a second semiconductor structure are stacked along the vertical direction on a surface of the substrate layer, the first semiconductor structure comprises a plurality of semiconductor structures of a first conduction type, the second semiconductor structure comprises a plurality of semiconductor structures of a second conduction type, and the first conduction type is different from the second conduction type.

[0028] In an alternative embodiment of the present disclosure, the semiconductor device as described above further comprises:

[0029] an insulating layer, disposed between the first semiconductor structure and the second semiconductor structure, and through the semiconductor gate region.

[0030] In the first aspect, the drain region, the source region, and the channel region of the embodiment of the present disclosure are all doped with the same type of ions, are homojunction device structures, and have no interface effect between regions. By converting conventional interface conduction to body conduction, the drift velocity of the electrons or the drift velocity of holes is higher and the mobility efficiency of the carrier is higher, resulting in a higher drift velocity of the electrons or a higher drift velocity of holes and further improving the working efficiency and the device reliability of the semiconductor structure.

[0031] In the second aspect, the drain region, the source region, and the channel region in the embodiment of the present disclosure are all doped with the same type of ions, the conventional interface conduction is converted into the body conduction, and the channel region is directly controlled by the gate electrode.

[0032] In a case where no voltage or 0 V voltage applied to the gate region, due to the energy

band difference between the gate region and the channel region (the electron affinity of the Si device (the difference between the bottom of the conduction band to the vacuum energy level) is 4.05eV), the channel region of the device is self-depleted by the affecting of the gate region to form a self-depleted non-inverted semiconductor structure. That is, only in the case where a voltage is applied to the gate region, does the current flow from the high doping region of the drain region through the channel region to the source region, that is the channel region is turned on. In the case where no voltage is applied to the gate region, the channel region is in an off state, forming a normally-off device and consuming less energy than the conventional normally-on device.

[0033] In the third aspect, the semiconductor structure provided by the embodiment of the present disclosure is body conduction, and the device has no PN junction structure. The threshold voltage reduction effect caused by the PN junction can be eliminated with no PN junction depletion layer, that is, the characteristic size can be further reduced. Experiments have shown the channel length of the device can meet the requirement of less than 10 nm.

[0034] In the fourth aspect, the semiconductor structure provided by the embodiment of the present disclosure is body conduction, the conducting current away from the interface, and no problem of lowering interface mobility. The conducting current is away from the interface further reduces tunneling current and gate leakage, and improves the reliability and stability of the device structure.

[0035] In the fifth aspect, the semiconductor structure provided by the embodiment of the present disclosure is a non-inverted type device, the electrons of the channel region do not flow through the surface inversion layer, thus avoiding the gate leakage of the device. At the nanoscale, the tunneling current caused by the tunneling effect is the main source of the gate leakage, the thickness of the gate dielectric of the device is limited, and the high-k dielectric has been developed. After adopting the high-k dielectric, the gate dielectric can be thickened without decreasing the control capability of the gate. The semiconductor structure provided by the embodiment of the present disclosure can reduce tunneling current due to the current not on the surface inversion layer, and cannot adopt the high-k dielectric, providing a new technical direction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] The drawings described herein are intended to provide a further understanding of the present disclosure and are incorporated in and constitute a part of this specification, schematic embodiments of the disclosure together with the description serve to explain the principles of the present disclosure, and do not constitute an improper limitation of the present disclosure. In the drawings:

[0037] Fig. 1 is a process flow diagram of the conventional GAA;

[0038] Fig. 2 is a schematic structure diagram of the semiconductor structure provided by the

embodiment of the present disclosure;

[0039] Fig. 3 is a schematic simulation structure diagram of the semiconductor structure provided by the embodiment of the present disclosure;

[0040] Fig. 4 is a sectional view of the gate structure of the semiconductor structure provided by the embodiment of the present disclosure;

[0041] Fig. 5 is a data graph of the semiconductor structure provided by the embodiment of the present disclosure in an on state, illustrating simulation results of the electron concentration of the vertical channel region;

[0042] Fig. 6 is an energy band diagram and an electron distribution diagram of the buffer isolation region and the channel region of the case where the semiconductor structure provided by the embodiment of the present disclosure is an N-type device in an off state;

[0043] Fig. 7 is a transfer characteristic curve graph and a gate leakage curve graph of the case where the semiconductor structure provided by the embodiment of the present disclosure is an N-type device with a total gate width of 1 mm;

[0044] Fig. 8 is a transfer characteristic curve graph for different V_d of the case where the semiconductor structure provided by the embodiment of the present disclosure is an N-type device with a total gate width of 1 mm;

[0045] Fig. 9 is an energy band diagram and a hole distribution diagram of the buffer isolation region and the channel region of the case where the semiconductor structure provided by the embodiment of the present disclosure is a P-type device in an off state;

[0046] Fig. 10 is a transfer characteristic curve graph and a gate leakage curve graph of the case where the semiconductor structure provided by the embodiment of the present disclosure is a P-type device with a total gate width of 1 mm;

[0047] Fig. 11 is a transfer characteristic curve graph for different V_d of the case where the semiconductor structure provided by the embodiment of the present disclosure is a P-type device with a total gate width of 1 mm; and

[0048] Fig. 12 is a schematic device diagram of the semiconductor device provided by the embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0049] With the rapid development of semiconductor technology, as a modern electronic information industry, the complementary metal-oxide-semiconductor (CMOS) integrated circuits scale is increasing. The main reason is the continual reduction in the characteristic size of the CMOS device, and the most advanced 5 nm semiconductor process now is in mass production. However, with the continuous increase in integration, the continuous increase in power consumption of an integrated circuit chip has become a difficult problem for the development of

integrated circuits.

[0050] The short channel effect (SCE) is an important factor besides the higher requirements for process preparation accuracy. The short channel effects are effects that occur in the transistor in a case where the conducted channel length of the metal oxide semiconductor field effect transistor is reduced to the order of tens of nanometers or even a few nanometers. The short channel effects mainly include: the threshold voltage decreases with the channel length, drain-induced barrier lowering, carrier surface scattering, velocity saturation effect, and so on. The existence of the short channel effects makes the characteristic size of the semiconductor device cannot be further reduced. To reduce the short channel effects, currently, the industry has adopted special device structures, for example, a fin field-effect transistor (FinFET) and an all-envelop gate field-effect transistor are provided under the 14 nm node, a gate-all-around transistor (GAA) device is provided under the 5 nm node, to improve the impact of the short channel effects on the device.

[0051] Currently, the GAA device is in a more widely application, while the PN junction is still in the GAA device, that is, the problems such as doping diffusion remain and limit the size of the device. Moreover, as a surface channel device, the GAA device has problems such as surface mobility and the hot carrier effect. For example, the conventional GAA device has the following defects.

[0052] (1) Short channel effect and narrow channel effect affecting the threshold voltage

[0053] In the case where the channel length is reduced to a certain extent, the proportion of the depletion region of the source and the drain in the whole channel increases, the charges required to form the inversion layer on the silicon surface below the gate decrease, and the threshold voltage decreases. Meanwhile, the threshold voltage increases due to the charges in the widened part of the depletion region along the channel width. When the channel width decreases to the same order as the depletion region width, the threshold voltage decreases significantly, and the threshold voltage of the short channel device is very sensitive to the change of the channel length.

[0054] (2) Mobility field correlation effect and carrier velocity saturation effect

[0055] In a low field, the mobility is constant and the carrier velocity increases linearly with the electric field. In a high field, the mobility field decreases, and the carrier velocity saturates and is no longer related to the electric field. The conventional device has a surface inversion layer in an on state, the electron layer disposed on the interface of the device affected by the interface scattering. Drain saturation current and current characteristics of the device are determined by the interface mobility, and the mobility decreases affected by the surface scattering and Coulomb scattering in the semiconductor surface, and the surface carrier saturation velocity decreases. Meanwhile, the extremely strong electric field in the vertical interface direction of the gate will further reduce the carrier mobility.

[0056] (3) Degradation of subthreshold characteristics and the device cannot pinch off

[0057] The subthreshold region leakage makes the off-state characteristics of the MOSFET device worse and the static power consumption larger, resulting in logic state confusion in dynamic circuits and memory cells. The drain-induced barrier lowering (DIBL) effect caused by the short channel is a basic physical effect that determines the size limit of the short channel MOS device. The DIBL effect is in a case where a high voltage is applied to the drain, the source junction barrier lowers because the gate is short and the source is affected by the drain electric field. The drain depletion region extends and even connects to the source junction, making the device cannot pinch off. The drain voltage affects the off of the gate and affects the potential. In a case where the drain voltage increases, the drain voltage will not be affected after the normal turning off. In the case where the short channel effects exist, changing with the drain voltage, the higher the drain voltage, the higher the current.

[0058] (4) Gate dielectric layer tunneling and gate leakage of the device

[0059] The tunneling current is the current in microelectronics technology quantum tunneling effects of the carriers occur in a case where the semiconductor barrier or the thickness of the silicon dioxide thin film is as thin as the length of the de Broglie wave in the microelectronics. In a case where the size of the device scales down to the nanoscale, the tunneling current in the gate oxide layer by the tunneling effect cannot be ignored and becomes an important factor affecting the miniature device. In a case where the device is an inversion device, the carriers of the device exist at the interface of the device and the highest at the interface, and the tunneling current of the device is strong.

[0060] (5) 3D integrated and annealing process

[0061] The device process requires ion implantation and annealing, and annealing is contradictory to the low-temperature process. Temperature brings two problems, the first is diffusion, where the diffusion of the PN junction makes it impossible to miniature to a small size, and the second is that the high-temperature process cannot be adopted after the metal and the silicide process, damaging the silicide and metal structure.

[0062] (6) The process of the GAA is shown in Fig. 1, and the overall process is complex.

[0063] Therefore, a semiconductor device that can further break through the characteristic size is urgently needed.

[0064] To solve the above-described problems, a semiconductor structure and a semiconductor device are provided by the embodiment of the present disclosure. To make the objects, technical schemes, and advantages of the present disclosure clear, the present disclosure is described in further detail in conjunction with accompanying drawings and examples. It should be understood that the specific embodiments described herein are merely used to illustrate the present disclosure, and are not intended to limit the present disclosure.

[0065] The terms such as “first”, “second” and the like in the disclosure are used to distinguish

similar objects and are not necessarily used to describe a specific sequence or a precedence order. The “connected” and “linked” described in the present disclosure include direct connection and indirect connection (communication) unless otherwise specified. In the descriptions of the disclosure thereof, it is to be understood that orientation or position relationships indicated by terms “up”, “down”, “front”, “rear”, “left”, “right”, “vertical”, “horizontal”, “top”, “bottom”, “inside”, “outside”, “clockwise”, “counterclockwise”, and the like are orientation or position relationships shown in the drawings, are adopted not to indicate or imply that indicated devices or components must be in specific orientations or structured and operated in specific orientations but only to conveniently describe the disclosure and simplify descriptions, and thus should not be understood as limits to the disclosure.

[0066] In the present application, unless expressly stipulated and defined otherwise, the first feature is “on” or “under” the second feature may be that the first feature is in direct contact with the second feature, or that the first feature is in indirect contact with the second feature by means of an intermediate medium. Moreover, the first feature is “over”, “above” and “on”, the second feature may be that the first feature is directly above or obliquely above the second feature, or simply means that a level of the first feature is higher than that of the second feature. The first feature is “under”, “below” and “beneath”, the second feature may mean that the first feature is directly below or obliquely below the second feature, or it simply means that the level of the first feature is smaller than that of the second feature.

[0067] Please refer to Figs. 2 to 4, the embodiment of the present disclosure provides a semiconductor structure 10 at least comprising: a gate structure 30; a source region 300, and a drain region 400.

[0068] The source region 300 and the drain region 400 are disposed on two sides of the gate structure 30 respectively. Please refer to Figs. 2 and 3, Fig. 2 is a perspective structure view of the semiconductor structure 10 provided by the embodiment of the present disclosure. Fig. 3 is a simulation structure diagram of the semiconductor structure 10 provided by the embodiment of the present disclosure, including an x-direction along a planar extension and a y-direction along a vertical direction (a depth direction or a height direction). Fig. 4 is a sectional view of the semiconductor structure 10 along the yz direction in Fig. 3.

[0069] The gate structure 30 at least comprises: a channel region 100 and a gate region 200 disposed from inside to outside, where the channel region 100 is surrounded inside the inner cavity of the gate region 200, the channel region 100 is attached to the source region 300, the drain region 400, and the gate region 200, and the ion doping types of the drain region 400, the source region 300, and the channel region 100 are the same.

[0070] The gate region 200 can be a metal gate and the first ion doping type, the embodiment of the present disclosure is not specifically limited. The gate region 200 can comprise a top gate and

a bottom gate, as shown in Fig. 4, the top gate and the bottom gate are both disposed at the surface layer of the channel region 100, and the top gate and the bottom gate can be formed at one time to simplify the process. The source region 300 and the drain 400 can be high-doped regions to improve the movement performance of the conduction electron or hole. The first ion doping type is different from the second ion doping type. That is, the first ion doping type is N-type doping and the second ion doping type is P-type doping, or the first ion doping type is P-type doping and the second ion doping type is N-type doping.

[0071] In the first aspect, the drain region 400, source region 300, and the channel region 100 of the embodiment of the present disclosure are all doped with the same type of ions and are homojunction device structure, and no interface effect between the regions. By converting conventional interface conduction to body conduction, the drift velocity of the electron or the drift velocity of the hole is higher and the mobility of the carrier is higher, resulting in a higher drift velocity of the electron or a higher drift velocity of the hole, and further improves the working efficiency and the device reliability of the semiconductor structure 10. The body conduction is the conduction of electrons or holes along the interior of the device layers, differing from the interface conduction of the electric field formed at the interface or the inversion electron layer.

[0072] In the second aspect, the drain region 400, the source region 300, and the channel region 100 in the embodiment of the present disclosure are all doped with the same type of ions, the conventional interface conduction is converted into the body conduction, and the channel region 100 being controlled by the gate electrode directly.

[0073] With no voltage or 0 V voltage applied to the gate region 200, due to the energy band difference between the gate region 200 and the channel region 100 (the electron affinity of the Si device (the difference between the bottom of the conduction band to the vacuum energy level) is 4.05 eV), the channel region 100 of the device is self-depleted by the affecting of the gate region 200 to form a self-depleted non-inverted semiconductor structure 10. In the case where a voltage is applied to the gate region 200, the current flows from the high doping region of the drain region 400 through the channel region 100 to the source region 300, that is the channel region 100 is turned on. In the case where no voltage is applied to the gate region 200, the channel region 100 in the off state forms a normally-off device structure, consuming less energy than the conventional normally-on device.

[0074] In the third aspect, the semiconductor structure 10 provided by the embodiment of the present disclosure is body conduction, and the device has no PN junction structure. The threshold voltage reduction effect caused by the PN junction can be eliminated with no PN junction structure, that is, the characteristic size can be further reduced. Experiments have shown the channel length of the device can meet the requirement of less than 10 nm.

[0075] In the fourth aspect, the semiconductor structure 10 provided by the embodiment of the

present disclosure is body conduction, the conducting current away from the interface, and no problem of reduced interface mobility. The conducting current away from the interface further reduces tunneling current and gate leakage, and improves the reliability and stability of the device structure.

[0076] In the fifth aspect, the semiconductor structure 10 provided by the embodiment of the present disclosure is a non-inverted device, the electrons of the channel region 100 do not flow through the surface inversion layer, thus avoiding leakage from the gate of the device. At the nanoscale, the tunneling current caused by the tunneling effect is the main source of the gate leakage, the thickness of the gate dielectric of the device is limited, and the high-k dielectric has been developed. After adopting the high-k dielectric, the gate dielectric can be thickened without decreasing the control capability of the gate. The semiconductor structure 10 provided by the embodiment of the present disclosure can reduce tunneling current because the current is not on the surface inversion layer, and cannot adopt the high-k dielectric, providing a new technical direction.

[0077] Please refer to Figs. 2 and 4, in an alternative embodiment of the present disclosure, the gate structure region 30 further comprises: a dielectric layer 500, disposed between the gate region 200 and the channel region 100, and attached to the gate region 200, the channel region 100, the drain region 400, and the source region 300, where the gate region 200 is disposed inside different dielectric layer 500.

[0078] The dielectric layer 500 can be made of an insulating material such as silicon dioxide, and the gate region 200 is surrounded inside the dielectric layer 500 completely, that is, a thin dielectric is between the gate region 200 and the channel region 100, and similarly, a thin dielectric layer between the bottom gate and the channel. By the structure, an all-surrounded gate structure is formed. That is, the doping of the channel region 100 is circular surrounded by the dielectric layer 500, and only exposes the portions electrically connected to the source region 300 and the drain region 400.

[0079] Please refer to Figs. 2 and 4, in an alternative embodiment of the present disclosure, the gate structure region 30 further comprises a buffer isolation region 600, where: the buffer isolation region 600 is disposed between the channel region 100 and the dielectric layer 500, and attached to the dielectric layer 500, the channel region 100, the drain region 400, and the source region 300.

[0080] The gate region 200 and the channel region 100 are isolated by the buffer isolation region 600, and/or, the bottom gate region and the channel region 100 are isolated by the buffer isolation region 600. The buffer isolation region 600 can be a low doping region, that is, the ion doping concentration is less than the ion doping concentration of the drain region 400 and the ion doping concentration of the source region 300. By providing the buffer isolation region 600, the device does not form the surface inversion electron layer at the contact interface between the channel

region 100 and the gate region 200, avoiding the performance loss caused by the reduction of the surface mobility, effectively preventing the appearance of the electron tunneling effect, reducing the gate region current, preventing the interface scattering, and improving the reliability and stability of the device.

[0081] That is, the buffer isolation region 600 is disposed between each gate region 200 and channel region 100 to not form the surface inversion electron layer at the contact interface between the channel region 100 and the gate region 200, avoiding the performance loss caused by the reduction of the surface mobility, effectively preventing the appearance of the electron tunneling effect, reducing the gate region current, preventing the interface scattering, and improving the reliability and the stability of the device.

[0082] That is, the buffer isolation region 600 is of the same ion doping type as the channel region 100, the drain region 400 is of the same ion doping type as the source region 300, and can be grown and formed at the same time to reduce the complexity of the process, avoiding the conventional thermal processes such as the annealing, and improves the yield of the manufacturing of the device structure, as well as the reliability and stability of the performance of the finished device.

[0083] In an alternative embodiment of the present disclosure, the ion doping concentration of the buffer isolation region 600 is less than that of the drain region 400 and the source region 300; and/or, the ion doping concentration of the buffer isolation region 600 is one order of magnitude less than that of the channel region 100.

[0084] That is, the drain region 400 and the source region 300 are high-ion doped regions, the buffer isolation region 600 is a low-ion doped region, and an ion concentration difference is formed between the two to avoid the electron flow formed by the source region 300 and the drain region 400 scattering from the channel region 100 to the buffer isolation region 600, and further ensure the reliability and the stability of the device structure.

[0085] In an alternative embodiment of the present disclosure, the ion doping concentration of the buffer isolation region 600 is no more than $1 \times 10^{17} / \text{cm}^3$ as a low-doped region, the thickness of the buffer isolation region 600 is about 0.3 nm to 5 nm, and the buffer isolation region 600 is made of the Si material.

[0086] Please refer to Fig. 5, Fig. 5 is a data graph of the device structure when working, illustrating simulation results of the electron concentration of the vertical channel region 100 with a width of 1 nm of the channel region 100 and a thickness of 0.5 nm of the buffer isolation region 600 for example. The horizontal axis represents a position along the vertical direction of the channel in micrometers, where the 0 coordinate point is the center position of the channel in micrometers. The vertical axis represents the electron concentration in $/\text{cm}^3$. It can be seen that the electrons of the channel of the device are concentrated inside the channel region 100 in a conducted state, and the electron concentration in the buffer isolation region 600 of the device is reduced by

more than one order of magnitude, proving the device is in an internal conduction state.

[0087] In an alternative embodiment of the present disclosure, the ion doping concentration of the gate region 200 ranges from $1e16 /cm^3$ to $1e20 /cm^3$; and/or, the ion doping concentration of the channel region 100 ranges from $1e17 /cm^3$ to $5e19 /cm^3$; and/or, the ion doping concentration of the drain region 400 and the ion doping concentration of the source region 300 ranges from $1e18 /cm^3$ to $5e20 /cm^3$.

[0088] The device structure by the above concentration parameter range has a better self-depletion effect, better body conduction performance, and fewer other negative effects, further improving the stability and reliability of the device structure.

[0089] In an alternative embodiment of the present disclosure, the ion doping concentration of the drain region 400, the ion doping concentration of the source region 300, and the ion doping concentration of the channel region 100 are equal.

[0090] That is, the channel region 100, the drain region 400, and the source region 300 are in the same ion doping type and can be grown and formed at the same time to reduce the complexity of the process, avoiding conventional thermal processes such as the annealing, and improving the yield of the manufacturing of the device structure, as well as the reliability and stability of the performance of the finished device.

[0091] In an alternative embodiment of the present disclosure, the ion doping concentration of the drain region 400, the ion doping concentration of the source region 300, and the ion doping concentration of the channel region 100 are not less than $1e17 /cm^3$.

[0092] That is, the channel region 100, the drain region 400, and the source region 300 are made in the same type of materials, the required ions are injected into the initial materials and no additional ion doping is required during the manufacturing process. The channel region 100, the drain region 400 and the source region 300 can be grown and formed at the same time to reduce the complexity of the process, avoiding conventional thermal processes such as the annealing, and improving the yield of the manufacturing of the device structure, as well as the reliability and stability of the performance of the finished device.

[0093] In an alternative embodiment of the present disclosure, the ion doping concentration of the drain region 400, the source region 300, and the channel region 100 are made in one piece. That is, the channel region 100, the drain region 400, and the source region 300 are in the same ion doping type and can be grown and formed at the same time to reduce the complexity of the process, avoiding conventional thermal processes such as the annealing, and improving the yield of the manufacturing of the device structure, as well as the reliability and stability of the performance of the finished device. Moreover, by converting conventional interface conduction to body conduction, no interface effect between the regions at all, the electron drift velocity or the hole drift velocity is higher, and the surface mobility of the carrier is higher, further improving the

working efficiency of the semiconductor structure 10 and the device reliability.

[0094] In an alternative embodiment of the present disclosure, the semiconductor structure 10 is an N-type device and the gate region 200 is a metal having a metal working function ranging from 4.5 eV to 5.2 eV.

[0095] Please refer to Fig. 6, Fig. 6 is an energy band diagram and an electron distribution diagram of the buffer isolation region 600 and the channel region 100 of the case where the device is an N-type device in an off state and the metal of gate region 200 has a metal working function ranging from 4.5 eV to 5.2 eV. (a) of Fig. 6 is an energy band diagram, the horizontal axis represents a position along the vertical direction of the channel in a micrometer, where the 0 coordinate point is the center position of the channel and the vertical axis represents the electron concentration in $/\text{cm}^3$. (b) of Fig. 6 is an electron distribution diagram of the buffer isolation region 600, the horizontal axis represents a position along the vertical direction of the channel in micrometer, where the 0 coordinate point is the center position of the channel, and the vertical axis represents the electron concentration in $/\text{cm}^3$. As shown in Fig. 6, in a case where the metal working function of the gate region 200 ranges from 4.5 eV to 5.2 eV, the Fermi level of the semiconductor layer is located in the middle, the Fermi level distance of the conduction band and the valence band are both closed to 0.5 eV as shown in the diagrams in the silicon material, at the time electrons and holes are both very few, the device is completely shut down, and the performance of the device is excellent.

[0096] Please refer to Fig. 7, Fig. 7 is simulation result diagrams of the case where the device is an N-type device with a channel thickness of 7 nm and a total gate width of 1 μm . (a) of Fig. 7 is a transfer characteristic curve, the horizontal axis represents the gate voltage, and the vertical axis represents the drain current. (b) of Fig. 7 is a drain leakage I_gV_g graph, the horizontal axis represents gate voltage, and the vertical axis represents gate current. As shown in Fig. 7, in a case where the device structure is in the on-off state, the channel current variation is between 6 orders of magnitude, the gate leakage is controlled below 100 μA , and the performance of the device is excellent.

[0097] Please refer to Fig. 8, Fig. 8 is an I_dV_g curve graph for different V_d of the N-type device. As shown in Fig. 8, the difference in the current of the device for different drain voltages is small, and the drain-induced barrier lowering (DIBL) characteristic is better.

[0098] In an alternative embodiment of the present disclosure, the semiconductor structure 10 is a P-type device and the gate region 200 is a metal having a metal working function ranging from 4.0 eV to 4.5 eV.

[0099] Please refer to Fig. 9, Fig. 9 is an energy band diagram and a hole distribution diagram of the buffer isolation region 600 and the channel region 100 of the case where the device is a P-type device in an off state and the metal of gate region 200 has a metal working function ranging from

4.0 eV to 4.5 eV. (a) of Fig. 9 is an energy band diagram, the horizontal axis represents a position along the vertical direction of the channel in micrometer, where the 0 coordinate point is the center position of the channel and the vertical axis represents the electron concentration in $/\text{cm}^3$. (b) of Fig. 9 is a hole distribution diagram of the buffer isolation region 600, the horizontal axis represents a position along the vertical direction of the channel in micrometer, where the 0 coordinate point is the center position of the channel, and the vertical axis represents the hole concentration. As shown in Fig. 9, in a case where the metal working function of the gate region 200 ranges from 4.0 eV to 4.5 eV and in an off state, the Fermi level is located in the middle of the band gap, the holes are very few, the device is completely turned off, and the performance of the device is excellent.

[0100] Please refer to Fig. 10, Fig. 10 is simulation result diagrams of the case where the device is a P-type device with a channel thickness of 7 nm and a total gate width of 1 mm. (a) of Fig. 10 is a transfer characteristic curve, the horizontal axis represents the gate current, and the vertical axis represents the drain current. (b) of Fig. 10 is a drain leakage I_gV_g graph, the horizontal axis represents gate voltage, and the vertical axis represents gate current. As shown in Fig. 10, in a case where the device structure is in the on-off state, the channel current variation is between 5 orders of magnitude, the gate leakage is controlled below 100 μA , and the performance of the device is excellent.

[0101] Please refer to Fig. 11, Fig. 11 is an I_dV_g curve graph for different V_d of the P-type device. As shown in Fig. 11, the difference in the current of the device for different drain voltages is small, and the drain induced barrier lowering (DIBL) characteristic is better.

[0102] In an alternative embodiment of the present disclosure, the semiconductor structure 10 can be a FinFET device or a GAA device.

[0103] Please referring the beneficial effects of the semiconductor structure 10 as described above, the embodiment of the present disclosure provides a semiconductor device 20 with body conduction, non-inversion layer, small tunneling effect, small gate leakage, low power consumption, higher electron drift velocity or hole drift velocity, higher mobility efficiency of the carrier, small characteristic size and breakthrough the limiting of the device size.

[0104] Please refer to Fig. 12, the embodiment of the present disclosure provides a semiconductor structure 20, and the semiconductor structure 20 comprises:

[0105] any one of the semiconductor structures 10 as described above.

[0106] Please referring the beneficial effects of the semiconductor structure 10 as described above, the embodiment of the present disclosure provides a semiconductor structure 20 with body conduction, non-inversion layer, small tunneling effect, small gate leakage, low power consumption, higher electron drift velocity or hole drift velocity, higher mobility efficiency of the carrier, small characteristic size and breakthrough the limiting of the device size.

[0107] As shown in Fig. 12, in an alternative embodiment of the present disclosure, the number of the semiconductor structures 10 is a plurality; the conduction type of the plurality of the semiconductor structures 10 is not identical, and the plurality of semiconductor structures 10 is insulated from each other by insulating layers 22. It is to be explained that the plurality of semiconductor structure 10 can be stacked or arranged along any direction in the actual produce, Fig. 12 does not constitute a specific limitation of the semiconductor device 20 and the arrangement of the semiconductor structure 10.

[0108] That is, both N-type semiconductor device 20 and P-type semiconductor device 20 can be realized in the same device, and for example, a complementary FET can be made by 3D integration to form a logic unit realizing logic function. In the first aspect, the N-type semiconductor device 20 and the P-type semiconductor device are integrated in the same three-dimensional structure in the embodiment of the present disclosure, improving the integration level and reducing the area; In the second aspect, the delay caused by the connection wires can be reduced and the performance of the device can be improved. As shown in Fig. 12, the devices are divided into two types as example, the first conduction type device is between the bottom insulating layer 22 on the substrate layer 21 and the middle insulating layer 22, and the second conduction type device is on the middle insulating layer 22. The two types of devices are an NFET and a PFET in complementary, the number of the NFET and the PFET can be a plurality, and the metal layers of the NFET and the PFET have different metal working functions.

[0109] Please referring the beneficial effects of the semiconductor structure 10 as described above, the embodiment of the present disclosure provides a complementary-type FET device or GAA device with body conduction, non-inversion layer, small tunneling effect, small gate leakage, low power consumption, higher electron drift velocity or hole drift velocity, higher mobility efficiency of the carrier, small characteristic size and breakthrough the limiting of the device size.

[0110] In an alternative embodiment of the present disclosure, the semiconductor device 20 as described above comprises: a first semiconductor substrate 23 and a second semiconductor structure are stacked along the vertical direction on the surface of the substrate 21, the first semiconductor structure comprises a plurality of the first conduction type semiconductor structures, the second semiconductor structure comprises a plurality of the second conduction type semiconductor structures, and the first conduction type is different from the second conduction type. For example, the first conduction type is an N-type conduction and the second conduction type is a P-type conduction, or the first conduction type is a P-type conduction and the second conduction type is an N-type conduction.

[0111] As described above, the embodiment of the present disclosure provides a P-type and N-type complementary-type semiconductor device with body conduction, non-inversion layer, small tunneling effect, small gate leakage, low power consumption, higher electron drift velocity or hole

drift velocity, higher mobility efficiency of the carrier, small characteristic size and breakthrough the limiting of the device size.

[0112] In an alternative embodiment of the present disclosure, the semiconductor device 20 as described above further comprises: an insulating layer 22, disposed between the first semiconductor structure 23 and the second semiconductor structure 24, and through the gate region 200. The first semiconductor structure 23 and the second semiconductor structure 24 are isolated by the insulating layer 22, ensuring the relative independence of the first semiconductor structure 23 and the second semiconductor structure 24, avoiding mutual interference, and improving the stability and reliability of the device.

[0113] It is to be understood that, although the steps in the flowcharts are sequentially shown according to an indication of arrows, the steps are not necessarily sequentially performed according to a sequence indicated by the arrows. Unless otherwise explicitly stated in this specification, these steps are not necessarily performed in a strictly limited order, and the steps may be performed in other orders. Besides, at least some steps in the flowchart may include a plurality of sub-steps or a plurality of stages, the sub-steps or stages are not necessarily performed at the same moment and may be performed at different moments, the sub-steps or stages are not necessarily sequentially performed, and the sub-steps or stages and at least some of other steps or sub-steps or stages of other steps may be performed in turn or alternately.

[0114] The technical features of the embodiments described above may be combined in any way. For brevity of description, possible combinations of the technical features in the foregoing embodiments are not exhausted, which, however, are to be considered as falling within the scope of this specification as long as there is no contradiction in the combinations of these technical features.

[0115] The foregoing embodiments show only several implementations of the present disclosure and are described in detail, which, however, are not to be construed as a limitation to the patent scope of the present disclosure. It should be noted that a person of ordinary skill in the art may further make several variations and improvements without departing from the ideas of the present disclosure, and such variations and improvements fall within the protection scope of the present disclosure. Therefore, the protection scope of this patent application is subject to the protection scope of the appended claims.

CLAIMS

What is claimed is:

1. A semiconductor structure, comprising:
a gate structure region; and
a source region and a drain region, disposed on two sides of the gate structure respectively;
wherein the gate structure region comprises:
a channel region and a gate region disposed from inside to outside, wherein the channel region is surrounded inside an inner cavity of the gate region and attached to the source region, the drain region, and the gate region, and an ion doping type of the drain region, an ion doping type of the source region and an ion doping type of the channel region are same.
2. The semiconductor structure according to claim 1, wherein the gate structure region further comprises:
a dielectric layer, disposed between the gate region and the channel region and attached to the gate region, the channel region, the drain region, and the source region.
3. The semiconductor structure according to claim 2, wherein the gate structure region further comprises:
a buffer isolation region, disposed between the channel region and the dielectric layer, and attached to the dielectric layer, the channel region, the drain region, and the source region.
4. The semiconductor structure according to claim 3, wherein an ion doping concentration of the buffer isolation region is not more than $1 \times 10^{17} / \text{cm}^3$.
5. The semiconductor structure according to claim 3, wherein an ion doping concentration of the buffer isolation region is less than an ion doping concentration of the drain region and an ion doping concentration of the source region.
6. The semiconductor structure according to claim 3, wherein a thickness of the buffer isolation region ranges from 0.3 nm to 5 nm.
7. The semiconductor structure according to claim 1, wherein an ion doping concentration of the gate region ranges from $1 \times 10^{16} / \text{cm}^3$ to $1 \times 10^{20} / \text{cm}^3$.

8. The semiconductor structure according to claim 1, wherein an ion doping concentration of the drain region, an ion doping concentration of the source region, and an ion doping concentration of the channel region are equal.

9. The semiconductor structure according to claim 8, wherein the ion doping concentration of the drain region, the ion doping concentration of the source region, and the ion doping concentration of the channel region are not less than $1 \times 10^{17} / \text{cm}^3$.

10. The semiconductor structure according to claim 1, wherein the drain region, the source region, and the channel region are made integrally.

11. The semiconductor structure according to claim 1, wherein the semiconductor structure is an N-type device, and the gate region is a metal having a metal working function ranging from 4.5 eV to 5.2 eV.

12. The semiconductor structure according to claim 1, wherein the semiconductor structure is selected from at least one of a fin field-effect transistor (FinFET) device or a gate-all-around transistor (GAA) device.

13. The semiconductor structure according to claim 3, wherein an ion doping concentration of the buffer isolation region is one order of magnitude less than an ion doping concentration of the channel region.

14. The semiconductor structure according to claim 1, wherein an ion doping concentration of the channel region ranges from $1 \times 10^{17} / \text{cm}^3$ to $5 \times 10^{19} / \text{cm}^3$.

15. The semiconductor structure according to claim 1, wherein an ion doping concentration of the drain region and an ion doping concentration of the source region ranges from $1 \times 10^{18} / \text{cm}^3$ to $5 \times 10^{20} / \text{cm}^3$.

16. The semiconductor structure according to claim 1, wherein the semiconductor structure is a P-type device and the gate region is a metal having a metal working function ranging from 4.0 eV to 4.5 eV.

17. A semiconductor device, comprising:

a substrate layer; and

a first semiconductor substrate and a second semiconductor structure, stacked along a vertical direction on a surface of the substrate layer, wherein the first semiconductor structure comprises a plurality of semiconductor structures of a first conduction type, the second semiconductor structure comprises a plurality of semiconductor structures of a second conduction type;

wherein each of the plurality of semiconductor structure comprises:

a gate structure region; and

a source region and a drain region, disposed on two sides of the gate structure respectively;

wherein the gate structure region comprises:

a channel region and a gate region, disposed from inside to outside, wherein the channel region is surrounded inside an inner cavity of the gate region and attached to the source region, the drain region, and the gate region, and an ion doping type of the drain region, an ion doping type of the source region and an ion doping type of the channel region are same.

18. The semiconductor device according to claim 17, wherein conduction types of the plurality of the semiconductor structures are not identical.

19. The semiconductor device according to claim 17, wherein

the first conduction type is different from the second conduction type.

20. The semiconductor device according to claim 17, further comprising:

an insulating layer, disposed between the first semiconductor structure and the second semiconductor structure, and through the gate region of each of the plurality of the semiconductor structures.