Buried Metal Body Contact Structure and Method for Fabricating SOI MOSFET Devices

Field of the Invention

This invention is related, more generally, to semiconductor integrated circuit devices and to a method of forming such devices. More particularly, the present invention is directed to silicon-on-insulator (SOI) CMOS devices provided with a buried metal body contact for improving its performance and shrinking its size.

Background of the Invention

Silicon-on-insulator (SOI) has emerged as an alternative device technology to the conventional bulk technology prevalent in high performance VLSI (Very Large Scale Integrated) products . One of the main differences between the two technologies is how to connect the body (i.e., the area placed directly beneath the gate of the CMOS device, and more particularly, between the source and the drain) of a transistor. In a bulk technology, the body resides in the well or in the substrate. As a result, the body can easily be connected to a fixed potential without sacrificing area or performance. However, it is impractical to apply a body switching scheme typical of, for instance, DTMOS (dynamic threshold voltage MOS) FETs to a bulk technology device because the well to substrate junction is significant. Details of the DTMOS device are described in U.S. Patent No. 5,559,368, "Dynamic threshold voltage MOSFET having a gate to body connection for ultra-low voltage operation", wherein a dynamic threshold voltage IGFET such as a MOSFET is found to be operable at voltages of 0.6 volt or less. The threshold voltage of the transistor is reduced to 0 volt or less by interconnecting the gate contact and the device body in which the voltage controlled channel is located.

The Dynamic threshold MOSFET (DTMOS) was first described by F.

Assaderaghi in 1994, in an article entitled "Dynamic threshold voltage MOSFET (DTMOS) for ultra low voltage VLSI" published in the Electron Device Letters (USA), Vol.15, No.12, Dec. 1994, pp. 510-512. By connecting together the gate and the body, the device threshold voltage is lowered in the presence of a high gate voltage. This results in a much higher current drive than that found in a standard MOSFET operating at a low power supply voltage, while still maintaining a low leakage current at Vgs=0V.

A schematic diagram of the layout of a conventional SOI body contact device is shown in Fig. 1. Source 40, drain 30 and body contact 10 reside in an single SOI island 60. It is necessary to extend the gate to include a supplemental area 20 used to facilitate contact with the body underneath the gate 50. From the body contact to the middle of the device, the resistance is very high because of the low conductivity of the well. Additionally, the channel length is usually much shorter than its width and, therefore, the number of squares (i.e., width to length ratio) and the total resistance is very high. A DTMOS device can be formed by connecting the extended gate region 20 to the body contact 10 by way of an additional interconnect layer. The extended gate area 20 required for the body contact does not contribute to the current drive, but it increases significantly the total gate capacitance. All of this translates in a performance degradation (> 20% typically) and an increase in layout area. The drawbacks of these non-ideal conditions are so serious that the DTMOS technology becomes almost impractical for SOI technology.

In the SOI technology, it is difficult to contact the body, particularly, since it requires special layouts for contacting the body. These layouts typically increase the area taken by the device and reduce its performance by adding more capacitance. In view of the foregoing, it is customary to let all the transistors in the SOI VLSI technology have their body floating, leaving only a few transistors with their body contacted. A floating body, however, induces instability in many

circuits since the potential of the body fluctuates, making the circuit delay dependent on its past history. To assure proper functioning of the circuit, a transistor designer needs to be more conservative. By way of example, the threshold voltage of the devices needs to be higher to improve the noise margin. All the aforementioned factors involving a floating body affect the performance of SOI circuits. It is therefore beneficial to have a body contact that is deemed to be efficient without adding extra area and capacitance. This body contact can substantially improve the body switching, as it is the case in, e.g., DTMOS, currently used in SOI. For instance, DTMOS is the only technology that makes it possible for a CMOS circuit to operate with the power supply down to 0.2V and still achieve an acceptable performance. When operating at the same supply voltage, DTMOS offers a substantially smaller power consumption than that of a conventional CMOS circuit. In order for a DTMOS to work properly, the body resistance has to be sufficiently low to allow the body potential follow the switching input. The only course left to lower the resistance by orders of magnitude is to place metal directly underneath the body, as will be described in considerable detail hereinafter.

In an article entitled "0.25 μm W polycide dual gate and buried metal on diffusion layer (BMD) technology for DRAM embedded logic devices" published in the 1997 Symposium on VLSI Technology Digest of Technical Papers, pp. 23-24, there is described a logic process technology which is suitable for high speed, low voltage operation, logic and DRAM integration in one chip. To fabricate the embedded DRAM, a high thermal stability W polycide dual gate process is achieved by intentionally using a chemical oxide formation for large grain polysilicon growth. Lateral dopant diffusion and boron penetration through a 5nm thick gate oxide are prevented with being annealed at 1000°C for 10 sec and, then, at 850°C for 30 min. The buried metal process uses high energy implantation of metal such as Ti to a layer of metal silicide, i.e., $TiSi_2$, to lower the diffusion resistance. However, the process described does not provide a second

layer of interconnect and does not contact the MOSFET body. Furthermore, such a process is not compatible with SOI technology.

A similar approach is also described in U.S. Patent No. 5,236,872, "Method of manufacturing a semiconductor device having a semiconductor body with a buried silicide layer", wherein a semiconductor device in which a thin buried silicide layer is formed by implantation includes the step of first forming an amorphous layer by implantation, which layer is then converted into the buried silicide layer by a heat treatment. A thin buried silicide layer, about 10 nm thick, can be obtained in this manner, and the resulting structure is suitable, for example, for the manufacture of a metal-base transistor. As was the case in the previous reference, such a process is not compatible with SOI technology.

In another article entitled "Buried metallic layers with silicon direct bonding", published in the Proceedings of the Third International Symposium on Semiconductor Wafer Bonding: Physics and Applications (1995), pp. 553-560, there is described a method for manufacturing dielectrically isolated silicon substrates incorporating low resistivity buried metal silicide layers. Solid phase reaction of either sputtered W or Ti is employed to form the respective silicides. Stress and wafer warpage problems are avoided by bonding prior to the formation of the silicide. A tungsten layer bonding is achieved by first coating with polysilicon and by polishing before bonding. Annealing at 1000°C. strengthens the bond and forms WSi_2 with a resistivity of 30 Ohm/square. The WSi_2 layer is refractory, withstanding a 6 hours treatment at 1000°C without increase in resistivity. A low energy low dose phosphorous implant into the n-type active wafer ensures ohmic contact with the WSi_2. Buried $TiSi_2$ layers are achieved by bonding Ti layers to either silicon or silicon coated oxidized substrates. RTA (rapid thermal annealing) at 800°C for 10 seconds forms both the $TiSi_2$ and the bond. The $TiSi_2$ resistivity is 18 ohms/square. The bonded wafers show voids around the wafer periphery due to a non-uniform heating in

the RTA. The $TiSi_2$ layer is refractory but does interact with boron to degrade conductivity. A spacer of silicon is needed to separate the $TiSi_2$ from the oxidized handle wafers. The process described forms the metal underneath the silicon before any device processing. The metal patterned on one side of wafer is bonded to another wafer. The other wafer surface has to be silicon, but not oxide. No indication is, however, given of whether the process can be used to build an SOI transistor and contact the body.

In still another publication, entitled "SOI MOSFET with buried body strap by wafer bonding", published in the IEEE Transactions of Electron Devices, Vol. 45, No. 5, May 1998, pp.1084-91, there is described a device having a buried oxide in the SOI MOSFET which makes it possible to achieve a higher performance. It allows for various floating body effects, including the kink effect, drain current transients, and a history dependence on output characteristics. As previously mentioned, it is difficult to incorporate an effective contact to the body because of limitations imposed by the SOI structure. A candidate for maintaining device symmetry is embodied by the lateral body contact. However, high lateral body resistance makes the contact effective only in narrow width devices. The buried lateral body contact in SOI consists of a low resistance polysilicon strap running under the MOSFET body along the device width. MOSFETs having an effective channel length of 0.17 μm have been fabricated incorporating this buried body strap, showing improved breakdown characteristics. The process described forms only buried polysilicon but not the buried metal. The buried polysilicon is formed by bonding before device processing.

In yet another article entitled "Thin film quasi SOI power MOSFET fabricated by reversed silicon wafer direct bonding", published in the IEEE Transactions of Electron Devices, Vol. 45, No.1, Jan. 1998, pp.105-109, there is described a quasi SOI power MOSFET fabricated by reversed silicon wafer direct bonding. In this

power MOSFET, the buried oxide underneath the channel and source regions is removed, and the channel region is directly connected to the source body contact electrode to reduce the base resistance of the parasitic n-p-n bipolar transistor. The quasi SOI power MOSFET suppresses the parasitic bipolar action and shows an ON resistance which is lower than that of a conventional SOI power MOSFET. The chip level quasi SOI power MOSFET displays an ON resistance of 86 $m\Omega.mm^2$ and an ON state breakdown voltage of 30 V Although the process addresses SOI CMOS devices, no reference is made to buried metal.

In U.S. Patent No. 5,332,913, "Buried interconnect structure for semiconductor devices", there is described an improved density semiconductor device having a buried interconnect. The buried interconnect electrically connects electrical device regions on a semiconductor substrate such that other structures may directly overlay the buried interconnect without being electrically connected to the conductive portions of the interconnect. The interconnect consists of a buried conductor and conductive segments. The conductive segments are electrically joined to the buried conductor to form an electrical pathway. First, a buried conductor is formed over an oxidized portion of a first field oxide. A layer of selective poly-epitaxial silicon is then grown over the surface of the substrate. A non-conductive portion of selective poly-epitaxial silicon is then formed over the buried conductor by oxidizing at least some of the selective poly-epitaxial silicon layer. This non-conductive portion of the selective poly-epitaxial silicon allows other structures to be formed over the buried conductor which are not in direct electrical contact with the buried interconnect. Accordingly, buried metal is formed by selective poly-epitaxial silicon growth.

In U.S. Patent No. 5,702,957, "Method of making buried metallization structure" describes an IC structure providing conductive lines for routing within a semiconductor substrate immediately below the level of the active IC devices. These buried conductive lines are insulated from each other by dielectric regions formed as an insulating plane immediately below the active devices, resembling

a conventional silicon on insulator (SOI) structure. Within this plane, however, the buried conductive lines provide routes between various active device elements to form circuit interconnections such as intra-cell connections for a gate array. Thus, the buried conductive lines replace some of the routing from the metallization/dielectric layer stack on top of the active region. Herein, the buried metal is formed by high energy implantation of metal into the substrate before any device processing.

In U.S. Patent No. 5,306,667, "Process for forming a novel buried interconnect structure for semiconductor devices", an improved density semiconductor device having a buried interconnect is described. The buried interconnect incorporates an elevated source/drain structure formed by selective poly-epitaxial silicon growth and silicized source-drain-gate interconnect segments. First, a buried conductor is formed over an oxidized portion of a first field oxide. A layer of selective poly-epitaxial silicon is then grown over the surface of the substrate. Selected areas of the poly-epitaxial silicon layer are oxidized. A layer of refractory metal is deposited, annealed, and etched to complete the buried interconnect. Thus, the buried metal is formed by selective poly-epitaxial silicon growth.

In U.S. Patent No. 5,260,233, "Semiconductor device and wafer structure having a planar buried interconnect by wafer bonding", there is described a wafer structure suitable for the formation of semiconductor devices thereon and having a buried interconnect structure for interconnection of selected semiconductor devices according to a predetermined interconnection pattern and a method of making the same. The wafer structure consists of a primary substrate having a first thickness appropriate for the formation of the desired semiconductor devices. The primary substrate further includes: a) conductive interconnection pads of a second thickness formed on a bottom surface of the primary substrate according to the predetermined inter- connection pattern; b) first isolation pads of a third thickness formed on the bottom surface of the primary substrate between

the conductive interconnection pads; and c) interconnection pad caps of a fourth thickness formed upon the surface of the interconnection pads opposite from the primary substrate, wherein the interconnection pad caps are formed by a material suitable for wafer bonding, and further wherein the total thickness of the second thickness and the fourth thickness equals the third thickness. The structure further includes a secondary substrate having an oxide layer thereon bonded to the interconnection pad caps and the first isolation pads of the primary wafer. The buried metal is formed, herein, by bonding before device processing.

In U.S. Patent No. 4,977, 439, "Buried multilevel interconnect system", a method and apparatus for providing interconnections between levels on a semiconductor substrate of various types includes forming a plurality of trenches in the substrate, followed by forming conductive layers at the bottom of the trenches. The trenches are then filled with an oxide to provide a planar surface on the substrate. Various levels of trenches are provided with crossovers being formed by a bridging layer of a conductive material that is formed over an oxide layer in the lower level trenches. Vertical contacts are formed by etching an opening from the surface to the bottom of the trenches through the oxide layer and filling the opening with a metal plug. Herein, the buried metal is formed starting from the top surface. This method suffers the limitation of having the buried metal to be highly localized and further, it cannot be placed underneath the device.

In U.S. No. 4,778,775, "Buried interconnect for silicon on insulator structure", an improved processing for forming an interconnect in a process where a recrystallized polysilicon layer is formed over an insulative layer. Recrystallization takes place through a plurality of seed windows formed in the insulating layer. A doped region is formed in the substrate prior to deposition of the polysilicon layer. The polysilicon layer is in contact with at least a portion of the doped region through an opening in the insulating layer. Recrystallization takes place through this opening, and the doped region is electrically connected to a source or drain region

of a semiconductor device formed in the recrystallized layer. The buried metal or doped silicon is formed before any device processing, and the SOI material is formed by selective epitaxy growth through the seed windows .

Objects of the Invention

Accordingly, it is an object of the invention to improve the performance and density as well as reducing the size of an SOI MOSFET or of a DTMOS device by incorporating within the structure a buried metal body contact.

It is another object to provide additional layers of interconnections underneath the active region of the device.

It is yet another object to eliminate floating the body in devices manufactured using the SOI technology.

It is a further object to make a three-dimensional integrated circuit by placing metal directly underneath the active region.

It is a more particular object to fabricate a dense and high speed lateral bipolar device having a buried body contact.

Summary of the Invention.

In one aspect of the present invention, there is provided a structure and a process to form metal interconnect directly underneath the MOSFET device manufactured in a conventional SOI CMOS process. One or more layers of interconnection contact the silicon insulator from underneath the device through the buried oxide. In this manner, the bottom of source or drain diffusion area as well as the MOSFET body region can be contacted . Further, it provides a

connection having an extremely low resistance to the bottom of MOSFET body region.

An advantage of this configuration resides in eliminating the floating body effect -- a significant source of concern in the SOI technology. Furthermore, the body contact makes it possible to achieve a substantial power saving that lowers the standby power by applying a negative body bias. Even more significant, a DTMOS. device may be formed by attaching the gate to the body. In such a DTMOS, device, the threshold voltage is reduced during the turn-on phase, improving the current drive.

The present invention fully exploits the advantages of DTMOS technology. Beside providing body contact for SOI devices, this method also allows multi-layer of metal underneath he device, which translates in an improved density and performance.

In another aspect of the invention, there is provided an SOI MOS device having a source, a drain and a gate, the SOI MOS device including: a body region positioned between and separating the source and the drain; and a buried metal via placed directly under the body region and aligned with the gate, the buried metal contacting the body region without touching either the source or the drain.

In still another aspect of the invention, there is provided a dynamic threshold MOS device having a source, a drain and a gate, the dynamic threshold MOS device including: a body region positioned between the source and the drain; and a buried metal via placed directly under the body region and aligned with the gate, the buried metal via contacting the body region without touching the source or the drain, the buried metal extending alongside the gate and contacting the gate.

Brief Description of the Drawings

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

Fig. 1 shows a schematic top view of the layout of a prior art SOI device with body contact;

Fig. 2a is a schematic diagram of a top view of the layout of a buried metal SOI DTMOS device, in accordance with the present invention;

Fig. 2b is a schematic diagram of a top view of the layout of a SOI device with buried metal body contact, in accordance with the present invention;

Fig. 3 is a cross-sectional side view of the starting SOI CMOS wafer, specifically showing the bulk Si substrate; the buried oxide (BOX) and the body of the SOI MOSFET;

Fig. 4 illustrates the structure shown in Fig. 3 with a handling substrate attached to it;

Fig. 5 illustrates the structure of Fig. 4 with the bulk Si removed;

Fig. 6 shows a via opened in the BOX layer;

Fig. 7 shows the aforementioned via now filled with via fill;

Fig. 8 shows several layers interconnection layer positioned on top of the BOX layer, making contact with the MOS device terminals; and

Fig. 9 illustrates the layout of a SOI lateral bipolar with buried metal base contact, similar to the SOI device with buried metal body contact described in Fig. 2b.

Detailed Description of the Invention

A generic process to place metal directly underneath the active device of an SOI wafer will first be described to be followed by a description of the process that provides body contact to the SOI MOSFET. Finally, in order to form a DTMOS, a description will follow to show how the gate is connected to the body.

Generic Buried Metal Body Contact Process

Referring to Fig. 2a, there is shown a schematic diagram of a top view of an SOI DTMOS device having the gate attached to a buried metal contact, in accordance with the present invention. For the sake of clarity, the buried metal pattern is shown wider than the gate pattern, although the buried metal can be wider or narrower depending on the process selected. The buried metal recticle is aligned to the gate pattern.

Drain 30 and source 40 previously depicted in prior art Fig. 1 remain unchanged. The extended gate region 20 (Fig. 1) is replaced by a gate terminated in a shrunken configuration. Both, the source and the drain are placed on top of a first SOI island 60. The gate to body connection is provided by the through gate oxide contact 70. In the through gate oxide contact, the gate oxide is removed to provide contact between the gate to a second SOI island which contacts the buried metal 80. As shown in the drawing, no additional area is required for the gate-to-body connection, as compared to a conventional MOSFET layout, thereby precluding the presence of undesired additional gate capacitance.

Shown in Fig. 2b is a top view of a schematic depicting a body contact MOS device, according with a second embodiment of the present invention. Unlike Fig. 2a, wherein the gate and the body contact are merged, in Fig. 2b, a separate gate contact 50 and body contact 10 are provided, allowing for an independent control of the body voltage. Note that the structure shown in Fig. 2b

does not require an extended gate region 20, thereby eliminating the additional added capacitance that is introduced by the extended gate. Clearly, the device shown in Fig, 2b occupies a significantly smaller area than the prior art device shown in Fig. 1.

Referring now to Fig. 3, a cross-section of an SOI CMOS device in accordance with the present invention is illustrated, specifically showing the bulk Si substrate 100, the buried oxide (BOX) 110, and the body of the SOI MOSFET 130. Also shown are the through gate oxide contact 70 joining gate 50 to the second silicon island 60. This schematic represents a cross-section viewed from lines B-B'. When viewed from lines A-A', contacts (e.g., 120) are shown linking the source and drain to other circuits, devices, etc. (not shown).

Referring to Fig. 4, there is shown a handling wafer 170 attached to the topside of the wafer of Fig. 3. This handler is preferably made of silicon or glass, having a thickness adequate for mechanical handling (e.g., for an 8 inch wafer. the thickness is in the order of 0.5mm^2). The handler has preferably the same shape as the wafer and has the edge aligned with the wafer edge. The glueing material may need to withstand temperature up to 300°C because of the later buried metallization process. The handling substrate can be bulk, SOI or even glass material. It serves only as a mechanical support.

The bulk silicon of the original wafer is etched back by a chemical and/or mechanical grinding process until the buried oxide (BOX) is exposed (see Fig. 5). Such etch back process is similar to the one developed for bond-and-etch-back SOI process except that now the chemical etch, usually KOH, a Potassium-hydroxide solution, can easily stop at the buried oxide. This results in a perfectly flat and clean oxide surface. This surface is essential for the high resolution lithography to be discussed further hereinafter. The chemical etching has to be the last etching step because the mechanical grinding does not stop on oxide.

Referring to Fig. 6, a standard lithography process opens a via for etching.

The via is aligned to the front side pattern of the original wafer. Since the buried oxide typically measures 100-300 nm, it is transparent. Thus, most of the structure in the original wafer such as STI (shallow trench isolation) and gate pattern can be easily visualized for alignment. The via mask is mirrored for proper alignment. The oxide in the opening area is then removed using any etching technique, such as RIE. The etching should stop right at the oxide-silicon interface. Further over-etching is allowed provided that the etching does not reach the source, drain and gate region.

Referring to Fig. 7, the via opening is then filled by suitable plug material, preferably metal, e.g., tungsten. If the opening is sufficiently wide, metal (aluminum or copper) can be formed by a single damascene process. In order to insure good contact to the MOS body region 130 , the inner surface providing the interface with the via 190 needs to be either metal or silicon with proper doping.

Referring to Fig. 8, multilayer of metal 140 (preferably, Cu or Al) is formed on top of the BOX 110 by conventional metal deposition and etching. These metal layers provide interconnection between the buried metal via.

Referring now to Fig. 9, there is shown a top view of the SOI lateral bipolar device in accordance to another aspect of the present invention. This structure is similar to the body contact MOS device shown in Fig. 2b. The body area becomes now the base of the bipolar device, the emitter and collectors are, respectively, the source and drain of the MOS device. The gate is preferably left floating to save space. Alternatively, the gate can be connected to a fixed voltage with penalty of increased layout area.

Several advantages are evident from the description of the aforementioned structure:

Body boosting

Rather than connecting the body to gate of the same transistor, the body can be connected to the node of other devices. Depending on the output loading condition, the body voltage is boosted to increase the current drive when needed

High performance lateral bipolar device

With the efficient body contact, the device can be operated as a bipolar transistor. Because of the low base resistance and base-to-collector capacitance, this bipolar transistor is characterized by its high speed. Since bipolar transistor is a better device for analog application than CMOS, this invention enables the full integration of high performance analog and digital circuit. Its impact on, e.g., wireless communication, is substantial.

General Body Contact

DTMOS is only one example showing the benefit of having a reduced area and a low resistance body contact in the SOI technology. Besides, the new body contact structure can be beneficial in the following ways:

A) Elimination of the floating body effect

By fixing the body bias and/or connecting the body to the source, all the disadvantage of floating body are eliminated. It further improves circuit stability as well as performance.

B) Power saving

The standby power can be lowered by applying a negative body bias to an NFET device and a positive body bias to a PFET device. This technique cannot be extended to a conventional SOI technology because of the area penalty caused by adding the body contact. With this invention, the aforementioned technique can be used without any problems. It is even more efficient than bulk

technology in term of area because contacting the body at the bottom may be established independently of the connection to transistors located above.

The foregoing description of exemplary embodiments has been presented for the purposes of illustrating and describing the main points of the concept of the invention. The present invention is not limited, however, to those embodiments. Rather, various changes and modifications may be made in the details within the scope and range of equivalents of claims and without departing from the spirit of the invention.

CLAIMS

1. A silicon-on-insulator (SOI) MOS device having a source, a drain and a gate, the SOI MOS device comprising:

a body region positioned between and separating said source and said drain; and

a buried metal via placed directly under said body region and aligned with said gate, said buried metal contacting said body region without contacting said source or said drain.

2. The SOI MOS device as in claim 1, wherein said buried metal is co-planar with a buried oxide layer.

3. The SOI MOS device as in claim 1, wherein an interconnect placed below said buried metal connects the buried metal to other circuits.

4. A dynamic threshold MOS device having a source, a drain and a gate, the dynamic threshold MOS device comprising:

a body region positioned between said source and said drain; and

a buried metal via placed directly under said body region and aligned with said gate, said buried metal via contacting said body region without touching said source or said drain, said buried metal extending alongside said gate and contacting said gate.

5. The dynamic threshold MOS device as in claim 4, wherein said buried metal

via contacts said gate through an SOI island, said SOI island being insulated from said source and said drain, said SOI island further contacting said gate.

6. The dynamic threshold MOS device as in claim 5, wherein said SOI island has a resistance at least one order of magnitude lower than said resistance of said body region.

7. The dynamic threshold MOS device as in claim 4, wherein said buried metal via contacts said gate through a metal filled via.

8. A method a forming an SOI MOS device having a buried metal body contact. the method comprising the steps of:

providing an SOI substrate, said SOI substrate having a silicon thin-film on an buried oxide layer, said buried oxide layer being placed on a bulk silicon substrate;

forming a plurality of SOI islands electrically segregated from each other by insulating material;

depositing a conformal layer of insulation covering said SOI islands;

forming a gate on top of at least one of said insulated SOI islands;.

forming a source and a drain in said at least one of said SOI islands having said gate, leaving a body region separating said source from said drain;

forming interconnections to said drain, source and gate and linking said interconnections to elements forming a circuit;

filling areas between said interconnections with insulating material;

planarizing the top surface of said insulating material;

attaching a handling substrate to said planarized surface;

removing said bulk silicon substrate, exposing said buried oxide layer;

opening at least one window in said buried oxide layer, said window being aligned with said body region without overlap with said source and drain; and

forming a buried via by filling said window with metal.

9. The method as in claim 8, further comprising the steps of adding additional interconnect layers under said buried vias.

10. A method of forming an SOI dynamic threshold MOS device having a buried metal body contact, the method comprising the steps of:

providing an SOI substrate, said SOI substrate having a silicon thin-film on an buried oxide layer, said buried oxide layer being placed on a bulk silicon substrate;

forming a plurality of SOI islands electrically segregated from each other by insulating material;

depositing a conformal layer of insulation covering said SOI islands;

forming a gate on top of at least one of said insulated SOI islands and extending said gate beyond said SOI island;

having said extended gate contact a second one of said SOI islands;

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forming a source and a drain in said at least one of said SOI islands having said gate, leaving a body region separating said source from said drain;

forming interconnections to said drain, source and gate and linking said interconnections to elements forming a circuit;

filling areas between said interconnections with insulating material;

planarizing the top surface of said area filled with insulating material;

attaching a handling substrate to said planarized surface;

removing said bulk silicon substrate, exposing said buried oxide layer;

opening at least one window in said buried oxide layer, said window being aligned with said body region without overlap with said source and drain, said window extending said SOI island and contacting said gate through said second SOI island; and

forming a buried via by filling said window with metal.

11. The method as in claim 10, further comprising the steps of adding additional interconnect layers under said buried vias.