

## Description

### Title: Manufacturing of a POI Structure with a Highly Uniform Piezoelectric Layer

The present invention relates to the manufacturing process of Piezo on Insulator, POI, structures, in particular, POI structures usable for the manufacturing of microelectronic, micromechanical and photonic devices.

In the field of microelectronics, micromechanics and photonics POI structures are of increasing importance due to superior sensibility and information propagation properties, for example. For example, sensors as surface acoustic wave (SAW) sensors, or bulk acoustic wave (BAW) sensors utilizing the piezoelectric effect to transduce an electrical signal into a mechanical / acoustic wave offer particularly advantageous options due to a wide variety of measurable ambient parameters including temperature, pressure, strain and torque, for example.

A typical POI structure comprises a layer of piezoelectric material, in particular, a single-crystal material, such as, for example, lithium niobate ( $\text{LiNbO}_3$ ) or lithium tantalate ( $\text{LiTaO}_3$ ), on a support substrate, for example, made of silicon. Various processes of forming a thin layer of piezoelectric material on the support substrate are known in the art. Application of the Smart Cut™ technology has been proven particularly advantageous. According to this technology (see, for example, WO 2020/200986 A1), a piezoelectric substrate formed on a support substrate is implanted by light species to form a weakened region in the piezoelectric substrate and afterwards the piezoelectric substrate is bonded to a target substrate. By fracture at the weakened region the thin layer of piezoelectric material can be obtained on the support substrate. The transferred layer of piezoelectric material is subject to an anneal process and, subsequently, a polishing process, particular, by chemical mechanical polishing, CMP, in an attempt to improve the crystalline quality and achieve the desired thickness uniformity of a mono-domain layer of piezoelectric material with substantially all dipole moments being aligned parallel to each other in a given direction.

However, despite recent engineering progress, there is a risk that the achieved thickness uniformity of the transferred layer of piezoelectric material is not high enough to comply with the demands of actual applications.

- 5 Therefore, it is an object of the present invention to provide a technique of manufacturing a POI structure (based on the Smart Cut™ technology) with a high thickness uniformity of the layer of piezoelectric material.

The present invention addresses this object by providing a method of manufacturing a  
10 Piezoelectric on Insulator, POI, structure, comprising

providing a donor substrate comprising a piezoelectric substrate, wherein the piezoelectric substrate comprises or consists of one of lithium tantalate ( $\text{LiTaO}_3$ ) and lithium niobate ( $\text{LiNbO}_3$ );

15 transferring a piezoelectric layer from the piezoelectric substrate to a target substrate (for example, a silicon substrate); and

polishing the piezoelectric layer transferred to the target substrate with a chemical mechanical polishing, CMP, slurry, wherein the CMP slurry consists of an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon in the range of  
20 4 to 18.

The polishing step may be preceded by an annealing step in order to increase crystalline quality and consolidate the bonding between the piezoelectric layer and the target  
25 substrate. The amorphous silicon used for the CMP slurry may comprise or consist of precipitated amorphous silicon particles with diameters in the range of 40 to 60 nm.

It is known in the art to polish the transferred piezoelectric layer in order to remove a top  
30 multi-domain layer comprising a plurality of regions exhibiting different polarities and increase the surface quality (reduce roughness) and thickness uniformity. In the art, however, a CMP slurry consisting of an aqueous suspension of amorphous silicon with a much higher weight percent of the amorphous silicon, namely, in the range of 25 to 35,

is employed for the process of polishing the transferred piezoelectric layer. The inventors of the present invention found out that surprisingly polishing the transferred piezoelectric layer with a significantly lower concentration of amorphous silicon in the CMP slurry results in better polishing results in terms of thickness uniformity of the finally obtained mono-domain piezoelectric layer.

Other parameters of the entire manufacturing process may be chosen as it is done conventionally and known to the skilled person (see, however, description below). Depending on the actual choice of the piezoelectric material and values of the other parameters a weight percent of the amorphous silicon in the range of 4 to 13, in particular, 5 to 7, may be advantageous with respect to the resulting thickness uniformity of the finally obtained transferred piezoelectric layer.

According to an embodiment, the step of providing the donor substrate (pseudodonor, PSD) comprises bonding a block of piezoelectric material to a support (manipulator) substrate via a bonding layer, grinding and polishing the block of piezoelectric material to obtain the piezoelectric substrate and implanting a species (for example, hydrogen) into the piezoelectric substrate to obtain a weakened layer in the piezoelectric substrate. Thereby, a suitable donor substrate for providing a high quality piezoelectric layer above the weakened layer can reliably be manufactured. The bonding of the block of piezoelectric material to the support substrate may be mediated by a dielectric bonding layer, for example, a photo (UV) polymer layer or a layer made of or comprising silicon oxide and/or silicon nitride.

The step of transferring the piezoelectric layer to the target substrate may comprise bonding the donor substrate to the target substrate (at the side of the piezoelectric substrate) and fracturing the piezoelectric substrate at the weakened layer in an anneal process. Thereby, the piezoelectric layer can be reliably transferred to the target substrate without too heavy defects. Further post-processing (annealing and polishing) is, however, still needed as described above. It is noted that naturally occurring silicon oxide may be present between the transferred piezoelectric layer and the target substrate. Further, a dielectric assembly layer may be formed on or over a surface of the target

substrate before transfer of the piezoelectric layer to that surface. This dielectric assembly layer may be made of or comprise silicon oxide and/or silicon nitride or a stack of layers composed of these materials. Moreover, depending on the actual application a charge trapping layer may be formed on or over a surface of the target substrate before  
5 transfer of the piezoelectric layer to that surface. The charge trapping layer may be made of or comprise polycrystalline silicon.

For the polishing process, the target substrate with the transferred piezoelectric layer is positioned on a rotatable head and contacted with a rotatable polishing pad. According  
10 to particular embodiments, the head is rotated at 80 to 120 rounds per minute (rpm) and the polishing pad is rotated in the same direction as the head at a different speed as compared to the head in the range of 90 to 130 rpm. These parameter ranges may prove advantageous in terms of the thickness uniformity of the resulting polished piezo-  
electric layer.

15 According to another embodiment, the wafer pressure applied to the target substrate to press it against the polishing pad is not larger than 20.68 kPa (3 psi) or lower than 18.96 kPa (2.75 psi), for example, in the range of 17.24 kPa (2.5 psi) to 20.68 kPa (3 psi). For example, the ratio of the wafer pressure to the ring pressure used to hold the target sub-  
20 strate in place in a ring retainer during the polishing process is in the range of 1:2 to 5:3. These parameter ranges may prove advantageous in terms of the thickness uniformity of the resulting polished piezoelectric layer, in particular, in combination with the above cited parameter ranges.

25 According to another embodiment, the flow rate of the CMP slurry is lower than 250 ml/minute or 200 ml/minute or 150 ml/minute or in the range of 150 ml/minute to 250 ml/minute. These parameter ranges may prove advantageous in terms of the thickness uniformity of the resulting polished piezoelectric layer, in particular, in combination with the above cited parameter ranges.

30 Further, it is provided a POI structure comprising a piezoelectric layer formed on or over a target substrate and obtainable by the method according to one of the above-de-

scribed examples, wherein the piezoelectric layer exhibits a thickness uniformity (thickness range across the diameter of the layer) of less than 50 nm, in particular, less than 20 nm. Furthermore, it is provided a microelectronic, micromechanical or photonic device or micro-electro-mechanical system (MEMS) comprising such a POI structure.

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Additional features and advantages of the present invention will be described with reference to the drawings. In the description, reference is made to the accompanying Figures that are meant to illustrate preferred embodiments of the invention. It is understood that such embodiments do not represent the full scope of the invention.

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[Fig. 1] illustrates steps of a method of manufacturing a POI structure according to an embodiment of the present invention.

[Fig. 2] illustrates the technical effect of obtaining a highly uniform piezoelectric layer resulting from a method of manufacturing a POI structure according to an embodiment of the present invention.

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Herein, it is provided a method of manufacturing a POI structure comprising a target substrate on which a piezoelectric layer with high thickness uniformity is formed. The high thickness uniformity results from a polishing step performed with a relatively highly diluted aqueous suspension of amorphous silicon. The method employs the Smart Cut™ technology.

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Fig. 1 illustrates steps of a method of manufacturing a POI structure according to an embodiment of the present invention. The method is similar to a method described in WO 2020/200986 A1 but differs from the latter one by the inventive process of polishing the transferred piezoelectric layer.

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As shown in step i) of Fig. 1 a donor substrate 1 is provided that comprises a piezoelectric substrate 1a formed on a support (manipulator) substrate 1b. The piezoelectric substrate 1a is made of lithium tantalate ( $\text{LiTaO}_3$ ) or lithium niobate ( $\text{LiNbO}_3$ ). The support substrate 1b may be made of a material (or a plurality of materials) with a coefficient of thermal expansion close to that exhibited by a target substrate 7, i.e., the thermal expansion coefficient of the support substrate 1b differs from the one of the target sub-

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strate 7 by less than the difference of the thermal expansion coefficient of the piezoelectric substrate 1a and that of the target substrate 7. The support substrate 1b and the target substrate 7 may have identical thermal expansion coefficients and both substrates may, for example, consist of or comprise silicon. Moreover, both substrates may have similar thicknesses.

In order to obtain the donor substrate 1, a massive block of piezoelectric material may first be attached to the support substrate 1b, for example, using a molecular adhesion bonding technique. The bonding may be mediated by a dielectric bonding (adhesion) layer (not shown in Fig. 1), for example, a photo (UV) polymer layer or a layer made of or comprising silicon oxide and/or silicon nitride. The bonding process may include the application of a low temperature heat treatment (for example, at a temperature between 50 and 300°C, typically 100°C) making it possible to sufficiently reinforce the bonding energy to allow the following thinning step. Subsequently, the piezoelectric substrate 1a is formed by thinning, for example, by grinding and/or mechanical-chemical polishing.

The thinning step is carried out in such a way that the piezoelectric substrate 1a has a sufficiently low thickness such that the stresses generated during heat treatment applied in a later processing stage are reduced. On the other hand, the thickness has to be sufficiently high in order to provide the piezoelectric layer 3 that is to be transferred to the target substrate 7 or to provide for a plurality of such layers that are to be transferred one after the other in multiple transfer steps (after respective regeneration of the donor substrate 1) to respective target substrates. The thickness of the piezoelectric substrate 1a can be, for example, between 5 and 400 µm, for example, 20 µm or 100 µm.

Hydrogen (maybe supplemented by helium) is implanted ii) in the piezoelectric substrate 1a through the exposed surface 4 to generate a weakened layer 2 which marks the separation of the piezoelectric layer 3 from the remainder part 5 of the donor substrate 1. The nature and dose of the implanted species and the implantation energy can be chosen according to the thickness of the piezoelectric layer 3 that is to be transferred to the target substrate 7 and the physicochemical properties of the piezoelectric substrate 1a. For example, for a lithium tantalate substrate a dose of hydrogen ions between  $10^{16}$  and  $5 \cdot 10^{17}$  at/cm<sup>2</sup> with an energy between 30 keV and 300 keV may be implanted to delimit the piezoelectric layer 3 with a thickness of 200 nm to 2000 nm, for example.

According to the method illustrated in Fig. 2 the implantation step ii) is followed by the step of attaching iii) the donor substrate 1 to the support substrate 7 at the side of the piezoelectric substrate 1a by molecular adhesion and/or electrostatic bonding. A dielectric assembly layer 7b may be provided between the piezoelectric substrate 1a of the donor substrate 1 and the target substrate 7. The dielectric assembly layer 7b may comprise an oxide and may be made of or comprise silicon oxide and/or silicon nitride or a stack of layers composed of these materials. Further, a charge trapping layer, for example, made of or comprising polycrystalline silicon, may be formed on or over the target substrate 7 in order to enhance the electrical resistivity of the same if it is desired by an actual application.

The piezoelectric layer 3 is then detached from the remainder part 5 of the donor substrate 1 to obtain iv) a POI structure 9 comprising the target substrate 7, the dielectric assembly layer 7b (if provided) and the piezoelectric layer 3. Detachment at the weakened layer 2 is facilitated by heat treatment in a temperature range of around 100°C to 600° to allow the transfer of the piezoelectric layer 3 to the target substrate 7. Alternatively or additionally detachment at the weakened layer 2 can be facilitated by the application of a blade or a jet of gaseous or liquid fluid or any other mechanical force applied to the weakened layer 2.

Post-processing of the transferred piezoelectric layer 3 is necessary to obtain a transferred piezoelectric layer 3 having satisfactory mono-domain crystalline and surface quality (reduced roughness) and thickness uniformity as demanded by actual applications. The post-processing comprises a heat treatment v) of the piezoelectric layer 3, for example, at about 500°C in a neutral atmosphere or an atmosphere comprising oxygen. This heat treatment makes it possible to cure crystalline defects present in the piezoelectric layer and consolidates the bonding between the piezoelectric layer 3 and the target substrate 7. However, the heat treatment causes diffusion of hydrogen contained in the piezoelectric layer 3, particularly in its upper portion (of thickness of about 50 nm or less, for example) and, thereby, generation of a plurality of ferroelectric domains giving the upper portion a multi-domain character. In fact, the hydrogen implanted in the piezoelectric substrate 1a during the step of defining the piezoelectric layer 3 above the

weakened layer 2 is distributed in this substrate according to a profile presenting a concentration peak at the level of the weakening plane 2. After fracture at the weakened layer 2 the piezoelectric layer 3 transferred to the target substrate 7, thus, has a significant concentration of hydrogen and heat treatment leads to the generation of multi-domains, i.e., a plurality of regions exhibiting different polarities. Performance of devices which are intended to be formed on/in the piezoelectric layer 3 would be heavily affected by such multi-domains.

In order to remove the upper multi-domains and increase surface quality and thickness uniformity of the transferred piezoelectric layer 3 the post-processing comprises polishing of the exposed surface of the piezoelectric layer 3 (see step vi) in Fig. 1). For example, 100 to 300 nm of the upper part of the piezoelectric layer 3 may be removed by the polishing process to reach a pre-determined target thickness, for example, of about 600 nm.

According to the invention, the piezoelectric layer 3 is polished by CMP using a relatively highly diluted CMP slurry. Conventionally, an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon of 25 to 35 is used for the post-processing CMP step following thermal anneal of the transferred piezoelectric layer. According to the invention, an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon in the range of only 4 to 18, particularly, in the range of 4 to 13, more particularly, in the range of 5 to 7, is used as a CMP slurry. Other parameters of the overall manufacturing process may be chosen conventionally as it is known to the skilled person. A mono-domain piezoelectric layer in that substantially all dipole moments are aligned parallel to each other in a given direction can, thereby, be formed over the target substrate 7 providing both the required thickness uniformity and surface and crystalline qualities.

For the polishing process, the target substrate 7 with the transferred piezoelectric layer 3 is positioned on a rotatable head and contacted with a rotatable polishing pad. It may be preferred to use a "single zone" head with one single holding ring retainer rather than a "multizone" head that has several ring retainers with variable pressures applied to. For

example, during the polishing process, the head is rotated at 80 to 120 rounds per minute (rpm) and the polishing pad is rotated in the same direction as the head at a different speed as compared to the head in the range of 90 to 130 rpm. For example, the head may be rotated at 75 rpm and the polishing pad may be rotated at 100 rpm. The speed of a reconditioning brush may be chosen similar to the one of the head or the polishing pad.

The wafer pressure applied to the target substrate to press it against the polishing pad may be chosen not to be larger than 20.68 kPa (3 psi) or lower than 18.96 kPa (2.75 psi), for example, in the range of 17.24 kPa (2.5 psi) to 20.68 kPa (3 psi). For example, the ratio of the wafer pressure to the ring pressure used to hold the target substrate in place in a ring retainer during the polishing process is in the range of 1:2 to 5:3. The flow rate of the CMP slurry may be chosen to be lower than 250 ml/minute or 200 ml/minute or 150 ml/minute or may be chosen to be in the range of 150 ml/minute to 250 ml/minute.

The CMP slurry used according to the invention may be prepared by diluting a commercially available CMP slurry. For example, Klebosol 30HB50 may be diluted with water to obtain a CMP slurry with a weight percent of the amorphous silicon in the range of 4 to 18, particularly, in the range of 4 to 13, more particularly, in the range of 5 to 7. Klebosol 30HB50 has amorphous silicon with 25 to 35 weight percent and an average diameter of the precipitated amorphous silicon particles of 50 nm. Assuming 35 weight percent of amorphous silicon a dilution by adding 1 part water to 1 part of Klebosol 30HB50 (dilution of 1:1) results in a CMP slurry having 17.5 weight percent of amorphous silicon. A 1:4 dilution of Klebosol 30HB50 having 25 weight percent of amorphous silicon results in a CMP slurry having 5 weight percent of amorphous silicon and a 1:4 dilution of Klebosol 30HB50 having 35 weight percent of amorphous silicon results in a CMP slurry having 7 weight percent of amorphous silicon.

Fig. 2 illustrates exemplary results for the obtained thickness uniformity (thickness range) of the piezoelectric layer of the POI structure after CMP of the piezoelectric layer made of lithium tantalate with a CMP slurry obtained by diluting Klebosol 30HB50 with dilutions 1:1 to 1:6. The abscissa shows the diameter of the piezoelectric layer in mm

and the ordinate shows the thickness of the piezoelectric (LTO) layer in nm. Thickness profiles are shown for dilutions of the Klebosol 30HB50 with water of 1:1, 1:2, 1:3, 1:3.5, 1:4, 1:5 and 1:6. Other polishing parameters have been chosen in the above-described ranges.

- 5 It can be seen that for dilutions 1:5 and 1:6 edge removal is drastically increased resulting in a thickness range of the piezoelectric layer of 147.844 nm and 180.313 nm, respectively. However, for the other dilutions at least quite satisfying results could be achieved. The observed thickness range across the diameter of the layer for the 1:1 dilution is 61.879 nm. Excellent results can be achieved for the other dilutions shown. The
- 10 observed thickness range across the diameter of the layer for the 1:2 dilution is 36.82 nm, the observed thickness range across the diameter of the layer for the 1:3 dilution is 24.573 nm, the observed thickness range across the diameter of the layer for the 1:3.5 dilution is 23.186 nm, and the observed thickness range across the diameter of the layer for the 1:4 dilution is 21.849 nm.

**Claims**

1. A method of manufacturing a Piezoelectric on Insulator, POI, structure (9), comprising  
5 providing a donor substrate (1) comprising a piezoelectric substrate (1a), wherein the piezoelectric substrate (1) comprises or consists of one of lithium tantalate and lithium niobate;  
10 transferring a piezoelectric layer (3) from the piezoelectric substrate to a target substrate (7); and  
15 polishing the piezoelectric layer (3) transferred to the target substrate (7) with a chemical mechanical polishing, CMP, slurry, wherein the CMP slurry consists of an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon in the range of 4 to 18.
2. The method according to claim 1, wherein the CMP slurry consists of an aqueous suspension of amorphous silicon with a weight percent of the amorphous silicon  
20 in the range of 4 to 13, in particular, 5 to 7.
3. The method according to claim 1 or 2, wherein the amorphous silicon comprises or consists of precipitated amorphous silicon particles with diameters in the range of 40 to 60 nm.  
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4. The method according to one of the preceding claims, wherein the step of providing the donor substrate (1) comprises bonding a block of piezoelectric material to a support substrate (1b) via a bonding layer, grinding and polishing the block of piezoelectric material to obtain the piezoelectric substrate (1a) and implanting a  
30 species into the piezoelectric substrate (1a) to obtain a weakened layer (2) in the piezoelectric substrate (1a).

5. The method according to claim 4, wherein the step of transferring the piezoelectric layer (3) to the target substrate (7) comprises bonding the donor substrate (1) to the target substrate (7) and fracturing the piezoelectric substrate (1a) at the weakened layer (2).
- 5 6. The method according to one of the preceding claims, further comprising performing an anneal treatment of the piezoelectric layer (3) transferred to the target substrate (7) before the polishing of the piezoelectric layer (3).
- 10 7. The method according to one of the preceding claims, wherein the polishing comprises rotating the target substrate at 80 to 120 rounds per minute and a polishing pad in the same direction as the head and in contact with the piezoelectric layer (3) at a different speed as compared to the head at 90 to 130 rounds per minute.
- 15 8. The method according to one of the preceding claims, wherein the polishing comprises applying a wafer pressure to the target substrate (7) to press it against a polishing pad of not more than 20.68 kPa or less than 18.96 kPa, in particular, in the range of 17.24 kPa to 20.68 kPa.
- 20 9. The method according to one of the preceding claims, wherein the polishing comprises applying the CMP slurry to a polishing pad at a flow rate lower than 250 ml/minute or 200 ml/minute or 150 ml/minute or in the range of 150 ml/minute to 250 ml/minute.
- 25 10. Piezoelectric on Insulator, POI, structure (9), comprising a piezoelectric layer (3) formed on or over a target substrate (7) and obtainable by the method according to one of the preceding claims, wherein the piezoelectric layer (3) exhibits a thickness uniformity of less than 50 nm, in particular, less than 20 nm.
- 30 11. Microelectronic, micromechanical or photonic device or micro-electro-mechanical system comprising the POI structure (9) according to claim 10.