CLAIMS

1. A semiconductor device assembly, comprising:

a silicon core comprising:

a first side opposing a second side, wherein the silicon core has a via through the silicon core from the first side to the second side;

an oxide layer on the first side, the second side, and within the via; and

one or more conductive interconnections through the via and having a surface exposed at the first side and the second side;

an insulating layer over the oxide layer on the first side, the second side, and within the via;

a first redistribution layer on the first side;

a silicon stiffener frame over the insulating layer and the first redistribution layer on the first side, an outer surface of the stiffener frame disposed substantially along a perimeter of the semiconductor device assembly; and

a first semiconductor die disposed within a cavity of the silicon core and embedded within the insulating layer,

wherein 6 or more surfaces of the first semiconductor die are in contact with the insulating layer;

wherein the silicon core has a thickness less than or equal to 1 mm; and

wherein the stiffener frame has a thickness greater than or equal to 500 μm.

2. The semiconductor device assembly of claim 1, wherein the silicon stiffener frame is formed of substantially the same material as the silicon core.

3. The semiconductor device assembly of claim 1, wherein the silicon stiffener frame has a coefficient of thermal expansion (CTE) substantially matching a CTE of the silicon core.

4. The semiconductor device assembly of claim 1, wherein the silicon stiffener frame has an opening formed therein.

5. The semiconductor device assembly of claim 4, wherein the semiconductor device assembly further comprises a second semiconductor die disposed within the opening of the silicon stiffener frame.

6. The semiconductor device assembly of claim 5, wherein the second semiconductor die is electrically coupled to one or more contacts of the redistribution layer by flip-chip attachment.

7. The semiconductor device assembly of claim 5, wherein the silicon stiffener frame has a coefficient of thermal expansion (CTE) substantially matching a CTE of the silicon core and a CTE of the second semiconductor die.

8. The semiconductor device assembly of claim 5, further comprising a third semiconductor die electrically coupled to one or more electrical contacts on the second side of the semiconductor device assembly by a ball grid array (BGA).

9. The semiconductor device assembly of claim 1, wherein the silicon stiffener frame has a metal layer formed over one or more surfaces thereof.

10. The semiconductor device assembly of claim 9, wherein the metal layer comprises nickel.

11. A semiconductor device assembly, comprising:

a silicon core comprising:

a first side opposing a second side, wherein the silicon core has a via extending through the silicon core from the first side to the second side;

an oxide layer on the first side, the second side, and within the via; and

one or more conductive interconnections through the via and having a surface exposed at the first side and the second side;

an insulating layer over the oxide layer on the first side, the second side, and within the via;

a first redistribution layer on the first side;

a silicon stiffener frame contacting the oxide layer on the first side of the silicon core, an outer surface of the stiffener frame disposed substantially along a perimeter of the silicon core; and

a semiconductor die disposed within a cavity of the silicon core and embedded within the insulating layer,

wherein 6 or more surfaces of the semiconductor die are in contact with the insulating layer;

wherein the silicon core has a thickness less than or equal to 1 mm; and

wherein the stiffener frame has a thickness greater than or equal to 500 μm.