

FIG. 1

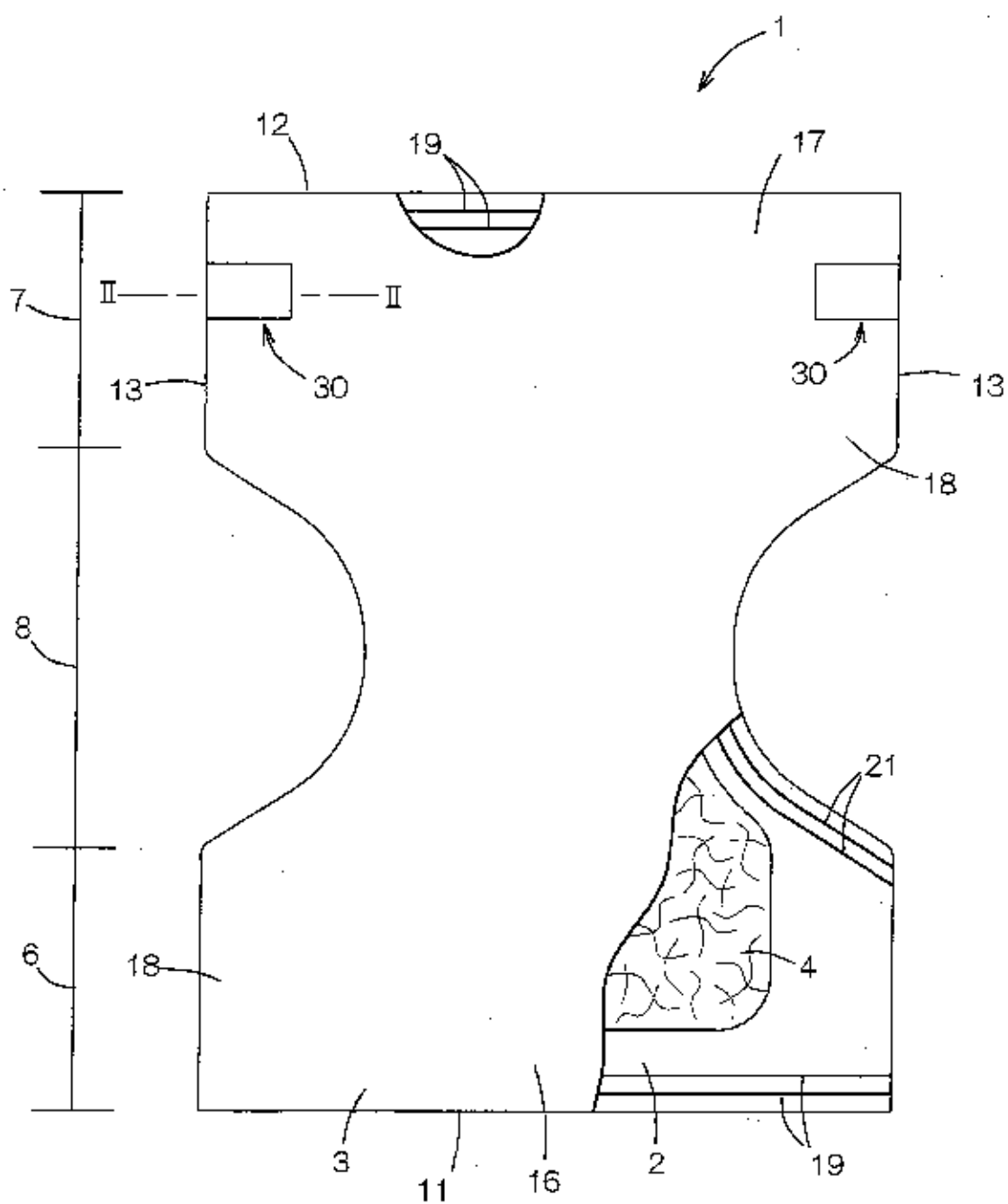


FIG.2

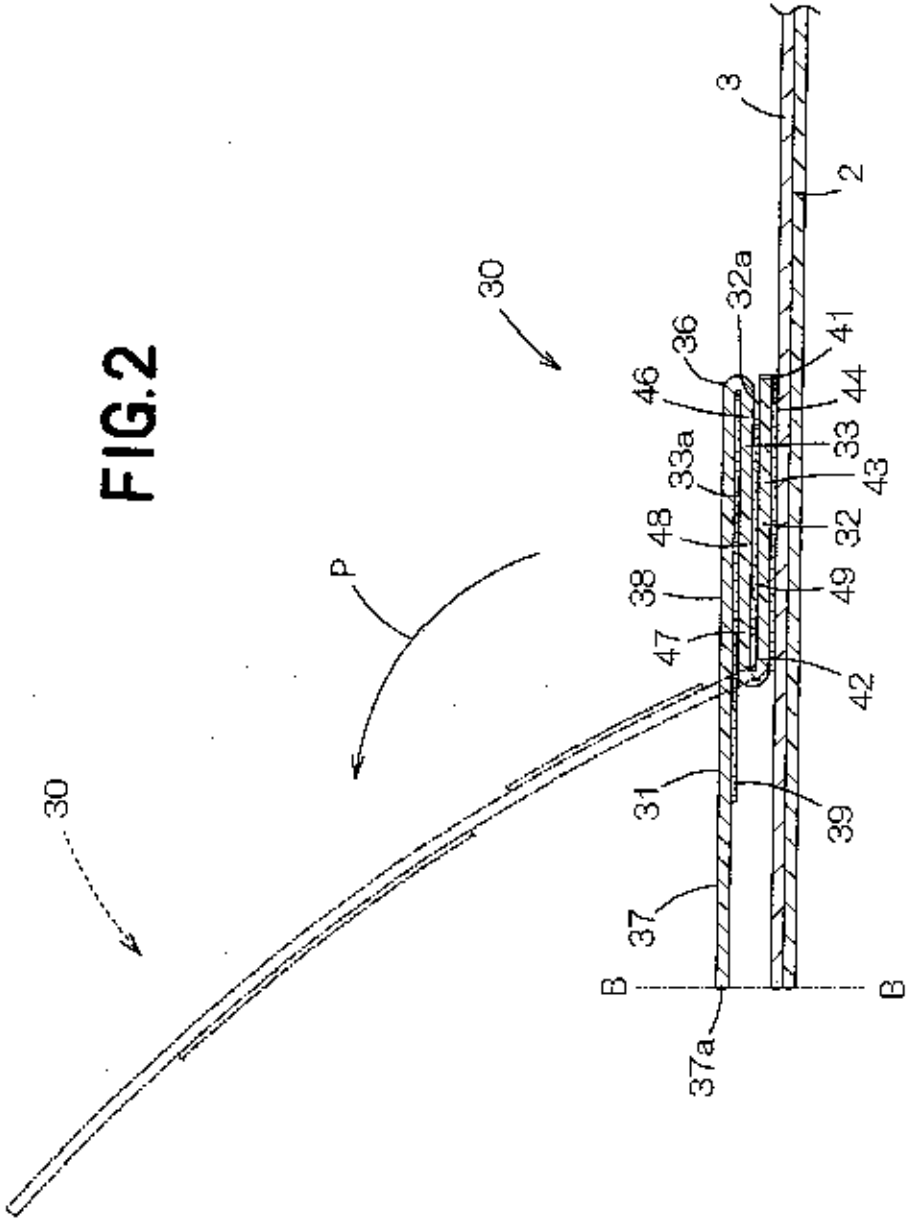


FIG.3A

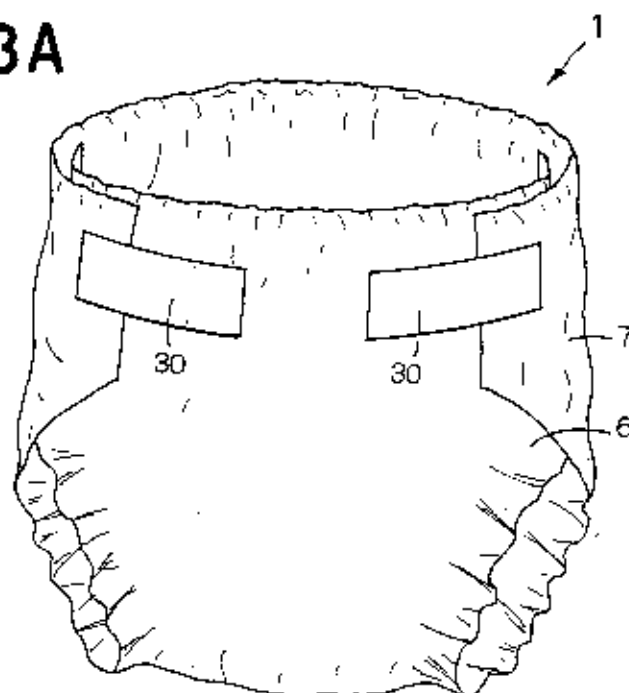


FIG.3B

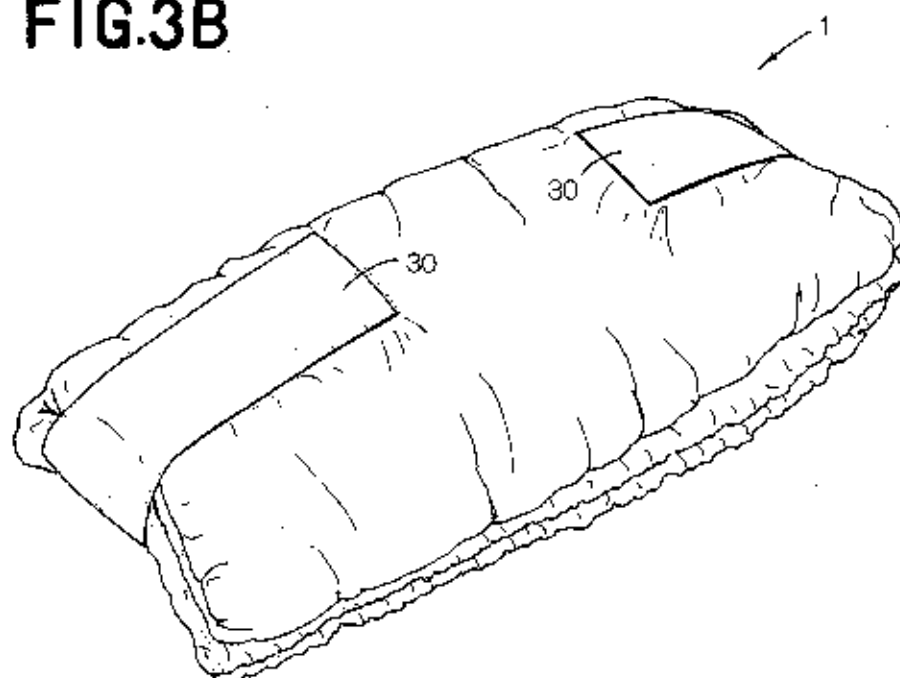
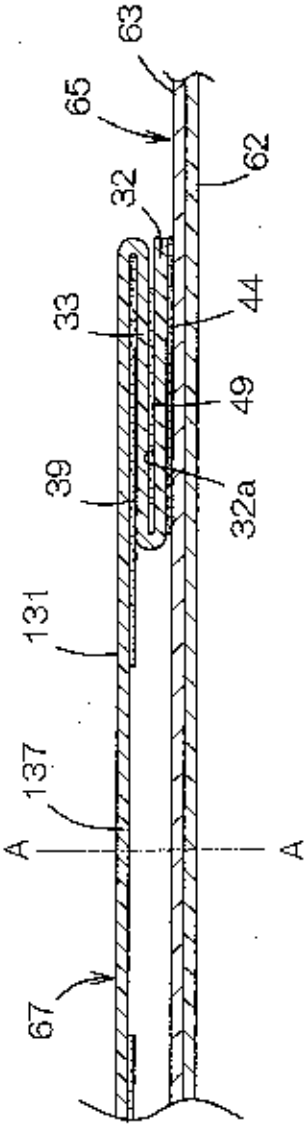
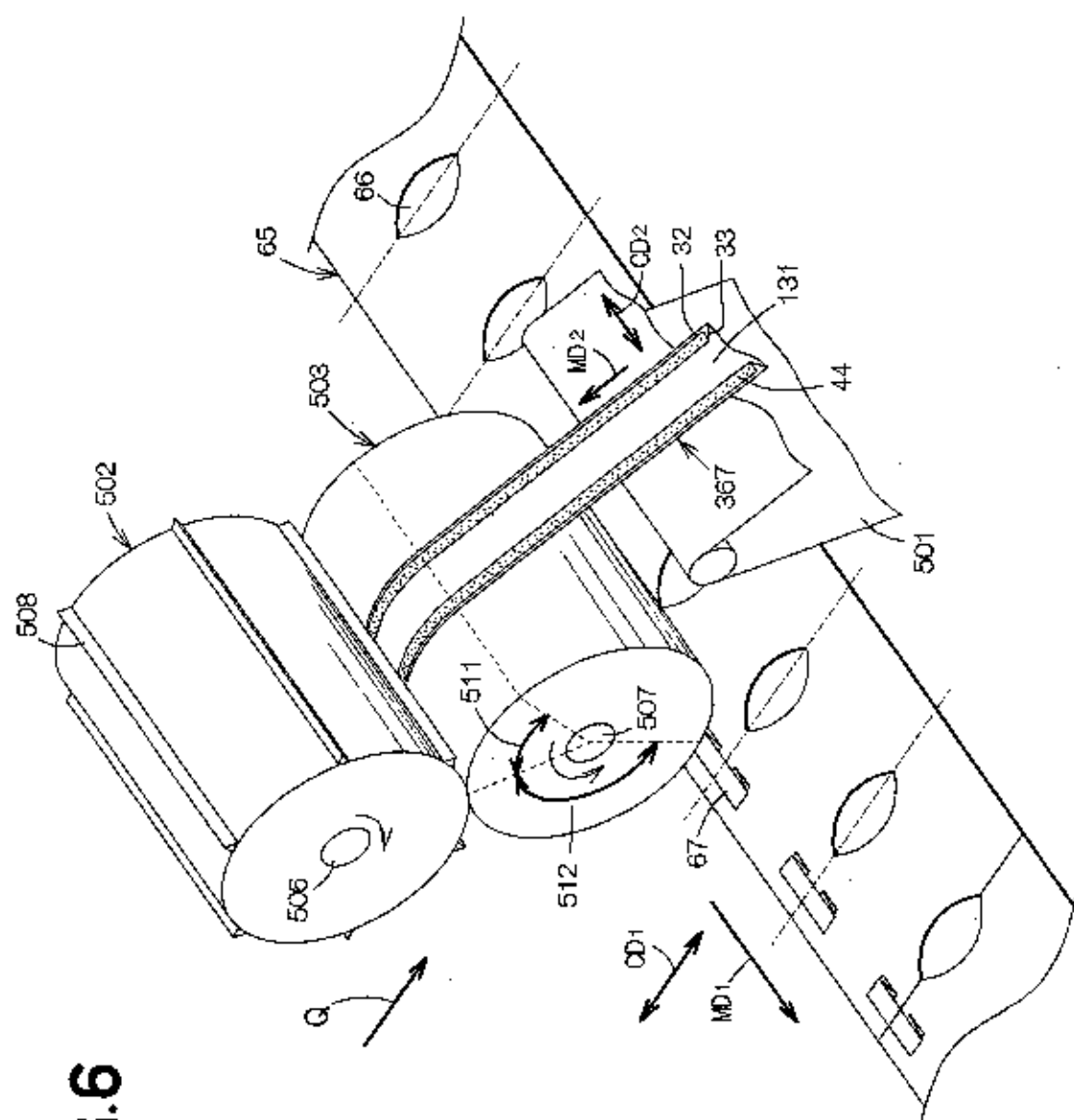


FIG. 4

FIG. 4 is a schematic diagram of a semiconductor device 1 in three cross-sectional views (1), (2), and (3) along a line A-A. The device includes a substrate 63, a gate stack 67, and a channel region 86. In view (2), a source/drain region 4 is shown with a textured pattern. Dimensions CD1 and MD1 are indicated for the gate stack, and CD2 and MD2 for the channel region. Arrows (a), (b), and (c) indicate different cross-sectional directions.

FIG.5





9.9.13

FIG. 7

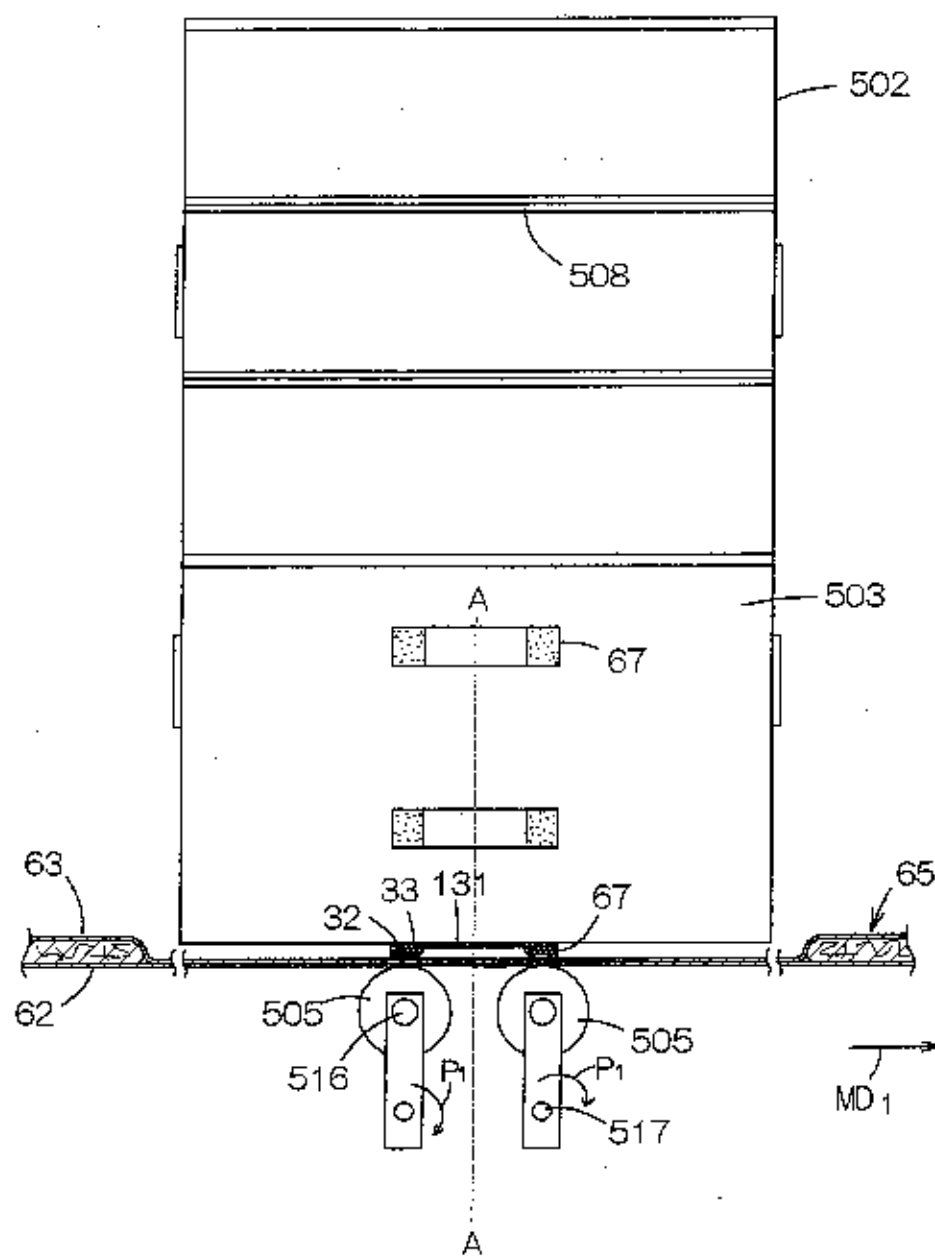


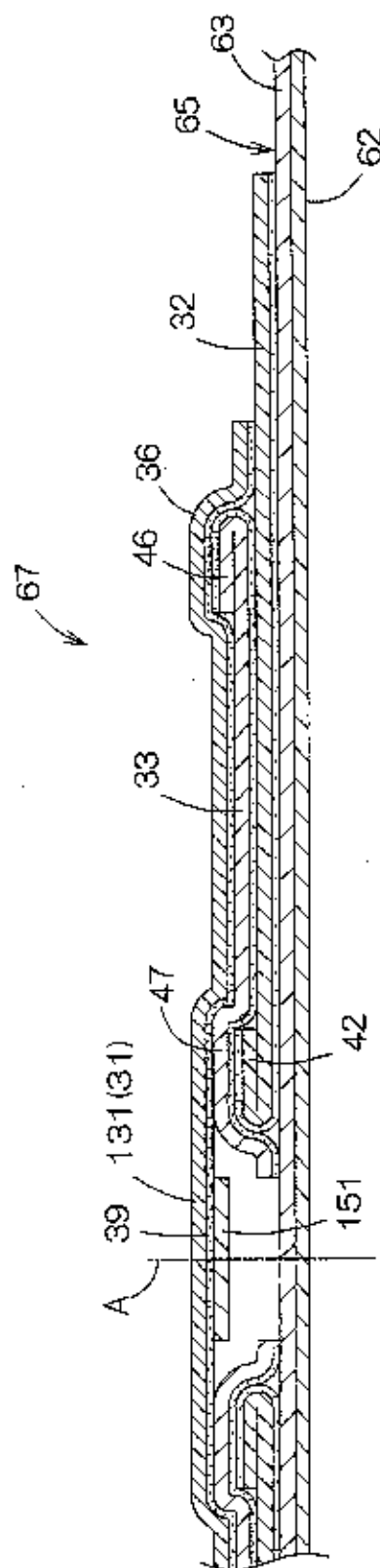
Fig. 9

FIG.10

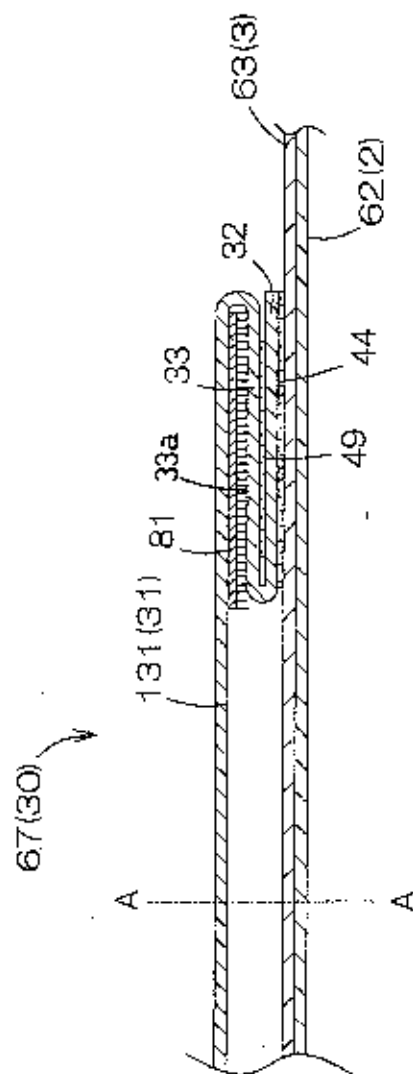


FIG.11

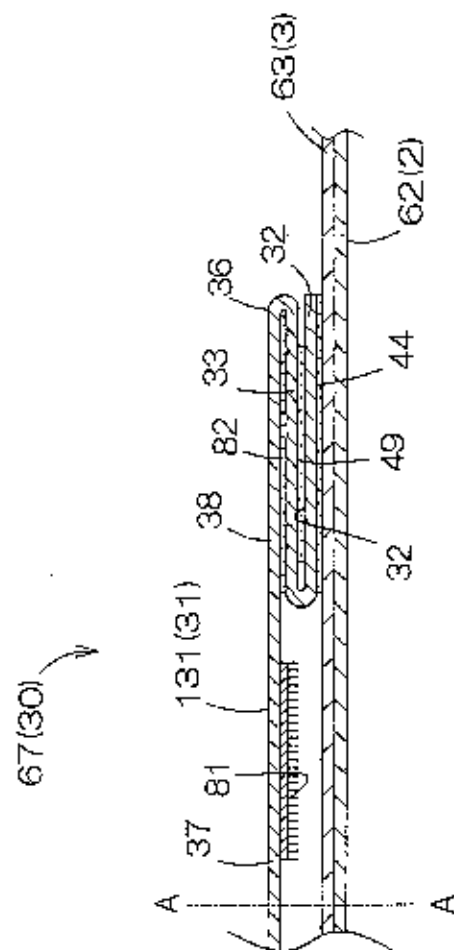


FIG.12

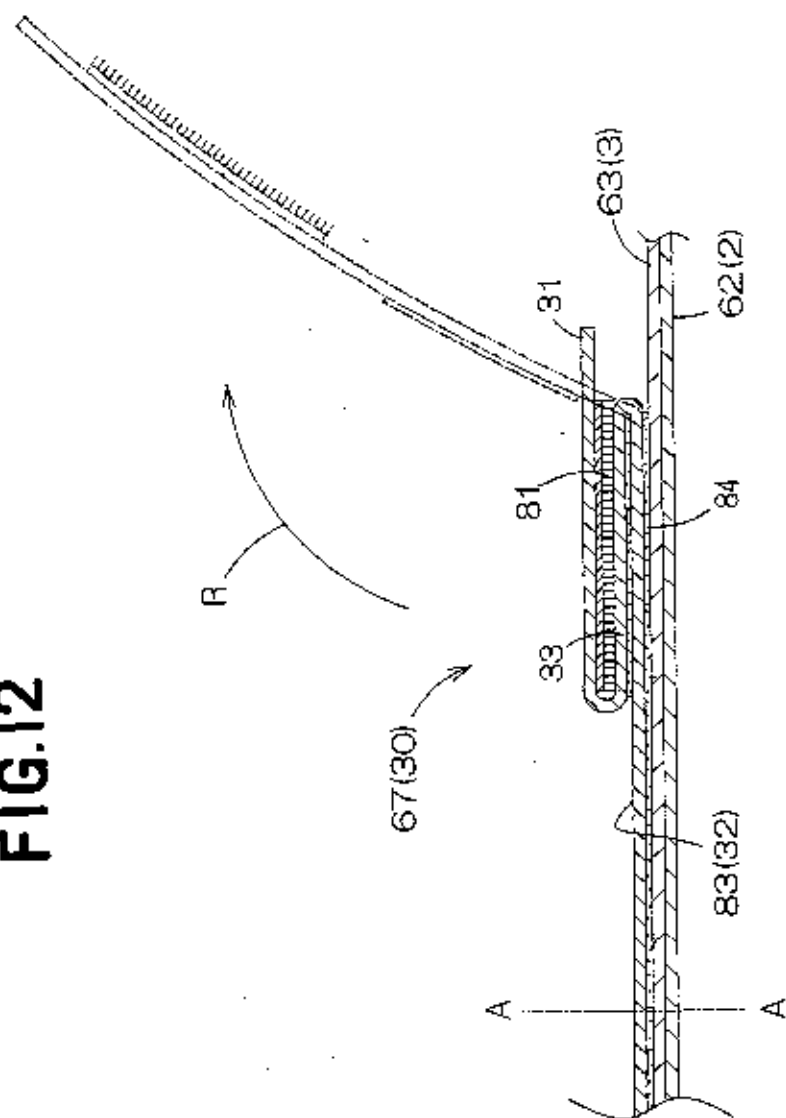


FIG.13

