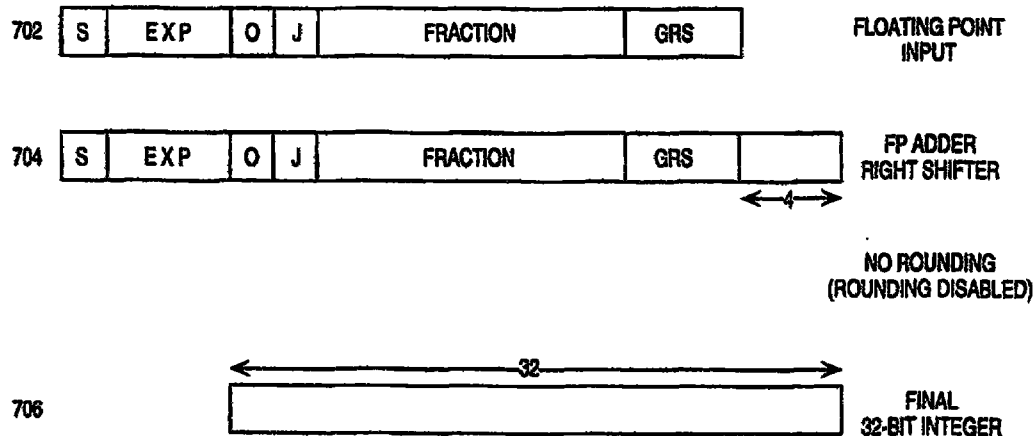




## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| (21) International Application Number: <b>PCT/US99/09156</b><br>(22) International Filing Date: <b>27 April 1999 (27.04.99)</b><br>(30) Priority Data:<br>09/071,466                      30 April 1998 (30.04.98)                      US<br>(71) Applicant (for all designated States except US): <b>INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).</b><br>(72) Inventors; and<br>(75) Inventors/Applicants (for US only): <b>ABDALLAH, Mohamad, A. [-/US]; 1009 Folsom Ranch Drive #203, Folsom, CA 95630 (US). MODALI, Prasad [IN/US]; 3115 Stonehurst Court, El Dorado Hills, CA 95762 (US).</b><br>(74) Agents: <b>TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor &amp; Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).</b> |  | (81) Designated States: <b>AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</b><br><br>Published<br><i>With international search report.</i> |                                                                 |

(54) Title: METHOD AND APPARATUS FOR FLOATING POINT OPERATIONS AND FORMAT CONVERSION OPERATIONS



## (57) Abstract

A floating point arithmetic apparatus for converting numbers between an integer format (706) and a floating point format (702), wherein a conversion operation requires a greater data path width than a conversion operation. The apparatus comprises right shift circuitry (704) that receives a number in the floating point format, wherein the right shift circuitry includes additional register positions to accommodate a shift beyond a data path width required by an arithmetic operation.