TEST CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the priority of the Chinese patent application No. 202110160891.7 filed with the China National Intellectual Property Administration (CNIPA) on February 5, 2021, entitled "TEST CIRCUIT", which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present application relates to, but is not limited to a test circuit.

BACKGROUND

[0003] Generally, in order to improve the reliability of memory chips (integrated circuits), memory chips need to undergo a series of tests before they leave the factory, these tests are for the functions and timings of the memory chips, and for finding out if the voltages generated by the voltage generating module in the memory chip are accurate, and so on, in addition, for performing voltage or resistance adjustments by testing some of the circuits in the memory chip.

[0004] The above tests all require sending the corresponding test mode signal to the circuit module in the memory chip to trigger the circuit module for testing. However, the number of circuit modules in the memory chip is large, and the test mode signals of different circuit modules are different. How to transmit test mode signals to different circuit modules accurately is a problem that needs to be solved urgently.

SUMMARY

[0005] A first aspect ~~An embodiment~~ of the present application provides a test circuit, including:

an input terminal, a processing circuit and an output terminal;

the input terminal being configured to receive an input signal, the input signal including a test command to instruct to test a target circuit module and an address of the target circuit module;

the processing circuit being configured to determine a test mode signal according to the test command and the address of the target circuit module, the test mode signal carrying a test type, the test mode signal being configured to trigger the target circuit module to perform a test corresponding to the test type;

the output terminal being configured to send the test mode signal to the target circuit module according to the address of the target circuit module.

[0006] A second aspect ~~Another embodiment~~ of the present application provides a memory, including a control circuit, at least one circuit module, and the test circuit according to the first aspect or any one of the possible implementations of the first aspect;

the control circuit being configured to send the input signal to the test circuit; and

the test circuit being configured to receive the input signal, and send the test mode signal to one of the at least one circuit module according to the input signal.

BRIEF DESCRIPTION OF DRAWINGS

[0007] In order to more clearly explain the technical solutions in the present application or the prior art, the following will briefly introduce the drawings that need to be used in the description of the embodiments or the prior art. Obviously, the drawings in the following description are some embodiments of the present application. For those of ordinary skill in the art, other drawings can be obtained based on these

drawings without creative labor.

[0008] FIG. 1 is a schematic diagram of an application scenario of a test circuit provided by an embodiment of the present application;

[0009] FIG. 2 is a schematic structural diagram of a test circuit provided by an embodiment of the present application;

[0010] FIG. 3 is a schematic structural diagram of a test circuit provided by an embodiment of the present application;

[0011] FIG. 4 is a schematic structural diagram of a test circuit provided by an embodiment of the present application;

[0012] FIG. 5 is a schematic structural diagram of a test circuit provided by an embodiment of the present application;

[0013] FIG. 6 is a schematic structural diagram of a test decoding circuit provided by an embodiment of the present application;

[0014] FIG. 7 is a schematic diagram of the internal structure of a 3-8 decoder;

[0015] FIG. 8 is a schematic structural diagram of a control logic circuit provided by an embodiment of the present application;

[0016] FIG. 9 is a schematic structural diagram of a self-test circuit provided by an embodiment of the present application;

[0017] FIG. 10 is a schematic structural diagram of a first test sub-circuit provided by an embodiment of the present application;

[0018] FIG. 11 is a timing sequence diagram of input and output signals of each unit in the test circuit shown in FIG. ~~4~~5; and

[0019] FIG. 12 is a schematic structural diagram of a memory provided by an embodiment of the present application.

DESCRIPTION OF EMBODIMENTS

[0020] In order to make the purpose, technical solutions and advantages of the present application clearer, the technical solutions in the present application will be described clearly and completely in conjunction with the accompanying drawings in

the present application. Obviously, the described embodiments are part of the embodiments of the present application, not all of the embodiments. Based on the embodiments in the present application, all other embodiments obtained by those of ordinary skill in the art without creative work shall fall within the protection scope of the present application.

[0021] The test circuit provided by the embodiment of the present application can be applied to a memory chip or an integrated circuit. It should be understood that the memory chip is a miniaturized integrated circuit, and the test circuit provided by the embodiment of the present application can also be applied to a non-miniaturized integrated circuit. The test circuit provided by the embodiment of the present application can be applied to a memory chip or an integrated circuit including at least one circuit module.

[0022] FIG. 1 is a schematic diagram of an application scenario of a test circuit provided by an embodiment of the present application. As shown in FIG. 1, the application scenario of the test circuit provided by an embodiment of the present application involves a memory chip 1. The memory chip 1 includes a control circuit 11, at least one circuit module 12 and a test circuit 13. It should be understood that there may be multiple circuit modules 12 in the memory chip 1, and different circuit modules 12 are responsible for different functions. When performing a series of tests on the memory chip 1 before leaving the factory, it is necessary to send a corresponding test mode signal to a circuit module 12 in the memory chip 1, to trigger the circuit module 12 to perform a corresponding functional test. However, the number of circuit modules 12 in the memory chip 1 is large, and the test mode signals of different circuit modules 12 are different. How to accurately transmit the test mode signals to different circuit modules is a problem.

[0023] To solve this problem, the present application provides a test circuit 13, the test circuit 13 receives an input signal sent by the control circuit 11. The input signal includes a test command to instruct to test a target circuit module and an address of the target circuit module. The test circuit 13 sends the test mode signal to the corresponding

target circuit module according to the input signal, thereby triggering the target circuit module to perform the corresponding functional test, thereby realizing the accurate transmission of the test mode signals to different circuit modules. It should be noted that the application scenario shown in FIG. 1 is only an example, and does not constitute a limitation on the application scenario of the test circuit of the present application.

[0024] The structure of the test circuit of the present application will be described below in conjunction with embodiments, and the structure of the test circuit of the present application is not limited to any of the following structures.

[0025] FIG. 2 is a schematic structural diagram of a test circuit provided by an embodiment of the present application. As shown in FIG. 2, the test circuit of this embodiment may include: an input terminal, a processing circuit 2 and an output terminal, where the input terminal is configured to receive an input signal, the input signal includes a test command to instruct to test a target circuit module and the address of the target circuit module.

[0026] The processing circuit 2 is configured to determine a test mode signal according to the test command and the address of the target circuit module, the test mode signal carries a test type, and the test mode signal is used to trigger the target circuit module to perform a test corresponding to the test type.

[0027] Where, the test type can be, for example, a function test, a timing test, or a voltage test of the memory chip, and the voltage test can test whether the voltage generated by the voltage generating module is accurate.

[0028] The output terminal is configured to send the test mode signal to the target circuit module according to the address of the target circuit module.

[0029] The test circuit provided in this embodiment includes an input terminal, a processing circuit and an output terminal. The input terminal receives an input signal including a test command to instruct to test a target circuit module and an address of the target circuit module. The processing circuit determines the test mode signal according to the test command and the address of the target circuit module, the determined test mode signal is used to trigger the target circuit module to perform a test

corresponding to the test type, and the output terminal sends the test mode signal to the target circuit module according to the address of the target circuit module. Therefore, the test circuit can accurately transmit the test mode signals to different circuit modules, and the circuit module can be triggered to perform a test corresponding to the test type carried by the test mode signal.

[0030] The structure of the processing circuit 2 shown in FIG. 2 will be described below with reference to FIGS. 3 to 5.

[0031] In an implementation, FIG. 3 shows a schematic structural diagram of a test circuit provided by an embodiment of the present application. As shown in FIG. 3, in the test circuit of this embodiment, the processing circuit 2 may include: a first address latch 21, a command logic circuit 22, and a second address latch 23, where the first address latch 21 is configured to receive the first internal address and output the first internal delay address. It should be understood that the first internal delay address is generated by the first internal address delayed by a preset time. The command logic circuit 22 is configured to receive a test command and a second internal address, and output a test mode command. The second address latch 23 is configured to receive the third internal address and the test mode command, and output the third internal delay address.

[0032] In an implementation, FIG. 4 is a schematic structural diagram of a test circuit provided by an embodiment of the present application. As shown in FIG. 4, the test circuit of this embodiment is based on the test circuit shown in FIG. 3, and further, may also include: a control logic circuit 24, a test decoding circuit 25, and a slave latch 26, where the control logic circuit 24 is configured to receive the first internal delay address and the test mode command, and output the test mode enable active signal and the test mode enable slave signal.

[0033] The test decoding circuit 25 is configured to receive the first internal delay address and the third internal delay address, and output a decoding signal.

[0034] The slave latch 26 is configured to receive the third internal address and the test mode enable slave signal, and output the slave address.

[0035] As an implementation, FIG. 5 is a schematic structural diagram of a test circuit provided by an embodiment of the present application. As shown in FIG. 5, the test circuit of this embodiment is based on the test circuit shown in FIG. 4, and further, may also include: a self-test circuit 27, the self-test circuit 27 is configured to receive the test mode enable active signal, the slave address, and the decode signal, and output the test mode signal to the target circuit module.

[0036] In some embodiments, the command logic circuit 22 is configured to generate a test mode command according to the test command when the value of the second internal address is a preset value. For example, the preset value is 1, that is, the command logic circuit 22 is configured to generate a test mode command according to the test command when the value of the second internal address is 1.

[0037] In some embodiments, the control logic circuit 24 is configured to: when the value of the first internal delay address is the first value, perform a logical operation on the first value with the test mode command to generate the test mode enable active signal; and when the value of the first internal delay address is the second value, perform a logic operation on the second value with the test mode command to generate the test mode enable slave signal. For example, when the first value is “00/01/10”, the control logic circuit 24 is configured to perform an AND operation on a value of inverting “00/01/10” with the test mode command to generate a test mode enable active signal. When the second value is “11”, the control logic circuit 24 is configured to perform an AND operation on the “11” with the test mode command to generate the test mode enable slave signal.

[0038] In an implementation, the test decoding circuit 25 may include multiple decoders. Preferably, the decoder may include a 3-8 decoder or a 4-16 decoder. The 3-8 decoder is taken as an example to show a structure of the test decoding circuit.

[0039] FIG. 6 is a schematic structural diagram of a test decoding circuit provided by an embodiment of the present application. As shown in FIG. 6, the test decoding circuit of this embodiment includes three 3-8 decoders: the first 3-8 decoder, the second 3-8 decoder, and the third 3-8 decoder. The three 3-8 decoders are used to receive the

first internal delay address and the third internal delay address. Correspondingly, the decoding signal includes a first decoding signal, a second decoding signal, and a third decoding signal. If the first internal address is 2 bits (RAT<1:0>) and the third internal address is 7 bits (RAD<6:0>), correspondingly, the first 3-8 decoder receives the first address: 3 bits (RAD<2:0>), and outputs the first decoding signal; the second 3-8 decoder receives the second address: 3 bits (RAD<5:3>), and outputs the second decoding signal; the third 3-8 decoder receives the third address: 3 bits (RAT<1:0> and RAD<6>), and outputs the third decoding signal.

[0040] FIG. 7 is a schematic diagram of the internal structure of a 3-8 decoder. As shown in FIG. 7, a 3-8 decoder includes 3 input ports (A, B and C) and 8 output ports (Y0-Y7) on the right. Each input port is connected to two inverters.

[0041] The structure of the control logic circuit will be described in detail below in conjunction with FIG. 8.

[0042] As an implementation, FIG. 8 is a schematic structural diagram of a control logic circuit provided by an embodiment of the present application. As shown in FIG. 8, the control logic circuit of this embodiment may include the first NAND gate 241, the first inverter 242, the second NAND gate 243, the second inverter 244, the third NAND gate 245, and the third inverter 246, where the output terminal of the first NAND gate 241 is connected to the input terminal of the first inverter 242, the output terminal of the second NAND gate 243 is connected to the input terminal of the second inverter 244, and the output terminal of the third NAND gate 245 is connected to the input terminal of the third inverter 246.

[0043] The first NAND gate 241 is configured to receive the first internal delay address and output the first signal. The first inverter 242 is configured to receive the first signal and output the second signal.

[0044] The second NAND gate 243 is configured to receive the first signal and the test mode command, and output the third signal. The second inverter 244 is configured to receive the third signal and output the test mode enable active signal. The third NAND gate 245 is configured to receive the second signal and the test mode command,

and output the fourth signal. The third inverter 246 is configured to receive the fourth signal and output the test mode enable slave signal.

[0045] The structure of the self-test circuit will be described in detail below in conjunction with FIG. 9.

[0046] As an implementation, FIG. 9 is a schematic structural diagram of a self-test circuit provided by an embodiment of the present application. As shown in FIG. 9, the self-test circuit of this embodiment may include a first test sub-circuit. Where, the first test sub-circuit includes a first logic control sub-circuit 271 and a first latch group 272. The first logic control sub-circuit 271 is connected to the first latch group 272. Each latch of the first latch group 272 corresponds to one test mode signal. It should be understood that the self-test circuit may include a plurality of first test sub-circuits.

[0047] As an implementation, the input terminal of the first logic control sub-circuit 271 is connected to the output terminal of the control logic circuit 24, the output terminal of the test decoding circuit 25, and the output terminal of the slave latch 26.

[0048] The first logic control sub-circuit 271 is configured to perform a logic operation according to the test mode enable active signal and the decoding signal, generate a clock signal, and output the clock signal to the first latch group 272.

[0049] The first latch group 272 is configured to receive the slave address and the clock signal, generate a test mode signal according to the slave address and the clock signal, and output the test mode signal to the target circuit module.

[0050] As an implementation, FIG. 10 is a schematic structural diagram of a first test sub-circuit provided by an embodiment of the present application. As shown in FIG. 10, the first test sub-circuit in this embodiment includes a first logic control sub-circuit 271 and the first latch group 272, where the first logic control sub-circuit 271 includes a first P-type transistor P1, a first N-type transistor N1, a second N-type transistor N2, a third N-type transistor N3, and a fourth N-type transistor N4.

[0051] The control terminal of the first P-type transistor P1 is connected to the output terminal of the control logic circuit 24, the first terminal of the first P-type transistor P1 is connected to the power supply terminal, and the second terminal of the

first P-type transistor P1 is connected to the input terminal of the first latch group and the first terminal of the first N-type transistor N1.

[0052] The control terminal of the first N-type transistor N1, the control terminal of the second N-type transistor N2, and the control terminal of the third N-type transistor N3 are all connected to the output terminal of the test decoding circuit 25. In some embodiments, the control terminal of the first N-type transistor N1 receives the first decoding signal, the control terminal of the second N-type transistor N2 receives the second decoding signal, and the control terminal of the third N-type transistor N3 receives the third decoding signal.

[0053] The second terminal of the first N-type transistor N1 is connected to the first terminal of the second N-type transistor N2, the second terminal of the second N-type transistor N2 is connected to the first terminal of the third N-type transistor N3, and the second terminal of the third N-type transistor N3 is connected to the first terminal of the fourth N-type transistor N4.

[0054] The control terminal of the fourth N-type transistor N4 is connected to the output terminal of the control logic circuit, the first terminal of the fourth N-type transistor N4 is connected to the second terminal of the third N-type transistor N3, and the second terminal of the fourth N-type transistor N4 is connected to the ground terminal.

[0055] In the above embodiment, preferably, the first internal address can be 2 bits (A<1:0>), the second internal address can be 1 bit (A<7>), and the third internal address can be 7 bits (A<7:0>).

[0056] FIG. 11 is a timing sequence diagram of input and output signals of each unit in the test circuit shown in FIG. 5. As shown in FIG. 11, a schematic diagram of the sequential relationship among the input and output signals of each unit in the test circuit shown in FIG. 5 on the time axis is shown. First, referring to FIGS. 5 and 11, after the test circuit in the embodiment of the present application receives the test circuit enable signal, the test circuit starts to work, and the first address latch 21 receives the first internal address (A<1: 0>), first receive the first internal address whose value is

“11”, and the first address latch 21 output the first internal delay address (RAT<1:0>) whose value is “11”. The command logic circuit 22 receives the test command and the second internal address (A<7>), and outputs the test mode command. The second address latch 23 receives the third internal address (A<7:0>) and the test mode command, and outputs the third internal delay address (RAD<7:0>) as shown in FIG. 11.

[0057] Next, the control logic circuit 24 performs an AND operation on the first internal delay address (RAT<1:0>) whose value is “11” with the test mode command to generate the test mode enable slave signal shown in FIG. 11, and outputs the test mode enable slave signal to the slave latch 26.

[0058] Next, the slave latch 26 receives the third internal delay address (RAD<7:0>) and the test mode enable slave signal, and outputs the slave address as shown in FIG. 11.

[0059] Next, the first address latch 21 receives the first internal address whose value is “00/01/10”, and the first address latch 21 outputs the first internal delay address (RAT<1:0>) whose value is “00/01/10”. The control logic circuit 24 performs an AND operation on a value of inverting the first internal delay address (RAT<1:0>) whose value is “00/01/10” with the test mode command to generate the test mode enable active signal, and outputs the test mode enable active signal to the self-test circuit 27.

[0060] Next, the test decoding circuit 25 receives the first internal delay address (RAT<1:0>) and the third internal delay address (RAD<7:0>), and outputs the decoding signal as shown in FIG. 11.

[0061] Finally, the self-test circuit 27 receives the test mode enable active signal, the slave address and the decoding signal, and performs a logical operation according to the test mode enable active signal and the decoding signal to generate the clock signal shown in FIG. 11, and generates the test mode signal shown in FIG. 11 according to the slave address and the clock signal, and finally outputs the test mode signal to the target circuit module.

[0062] The embodiment of the present application further provides a memory. FIG.

12 is a schematic structural diagram of a memory provided by an embodiment of the present application. As shown in FIG. 12, the memory of this embodiment may include a control circuit 31, at least one circuit module 32, and the test circuit 33 in any one of the foregoing embodiments.

[0063] Where, the control circuit 31 is configured to send an input signal to the test circuit 33.

[0064] The test circuit 33 is configured to receive an input signal and send a test mode signal to one of the at least one circuit module 32 according to the input signal.

[0065] In the memory provided by the present application, the test circuit in the memory can accurately transmit the test mode signals to different circuit modules, and then can trigger the circuit module to perform a test corresponding to the test type carried by the test mode signal.

[0066] Finally, it should be noted that the above embodiments are only used to illustrate the technical solution of the present application, but not to limit it; although the present application has been described in detail with reference to the foregoing embodiments, those of ordinary skill in the art should understand that the technical solutions described in the foregoing embodiments can still be modified, some or all of the technical features can be equivalently replaced; and these modifications or replacements do not make the essence of the corresponding technical solutions deviate from the scope of the technical solutions of the embodiments of the present application.

CLAIMS

1. A test circuit, comprising:

an input terminal, a processing circuit and an output terminal;

the input terminal being configured to receive an input signal, the input signal comprising a test command to instruct to test a target circuit module and an address of the target circuit module;

the processing circuit being configured to determine a test mode signal according to the test command and the address of the target circuit module, the test mode signal carrying a test type, the test mode signal being used to trigger the target circuit module to perform a test corresponding to the test type; and

the output terminal being configured to send the test mode signal to the target circuit module according to the address of the target circuit module.

2. The test circuit according to claim 1, wherein the processing circuit comprises:

a first address latch, a command logic circuit and a second address latch;

the first address latch being configured to receive a first internal address, and output a first internal delay address;

the command logic circuit being configured to receive the test command and a second internal address, and output a test mode command; and

the second address latch being configured to receive a third internal address and the test mode command, and output a third internal delay address.

3. The test circuit according to claim 2, wherein the processing circuit further comprises:

a control logic circuit, a test decoding circuit and a slave latch;

the control logic circuit being configured to receive the first internal delay address and the test mode command, and output a test mode enable active signal and a test mode enable slave signal;

the test decoding circuit being configured to receive the first internal delay address and the third internal delay address, and output a decoding signal; and

the slave latch being configured to receive the third internal address and the test mode enable slave signal, and output a slave address.

4. The test circuit according to claim 3, wherein the processing circuit further comprises:

a self-test circuit, being configured to receive the test mode enable active signal, the slave address and the decoding signal, and output the test mode signal to the target circuit module.

5. The test circuit according to claim 4, wherein the command logic circuit is configured to:

generate the test mode command according to the test command when a value of the second internal address is a preset value.

6. The test circuit according to claim 4 or 5, wherein the control logic circuit is configured to:

when a value of the first internal delay address is a first value, perform a logical operation on the first value with the test mode command to generate the test mode enable active signal; and

when the value of the first internal delay address is a second value, perform a logic operation on the second value with the test mode command to generate the test mode enable slave signal.

7. The test circuit according to any one of claims 4 to 6, wherein the test decoding circuit comprises a plurality of decoders.

8. The test circuit according to claim 7, wherein the decoder comprises a 3-8 decoder.

9. The test circuit according to any one of claims 4 to 8, wherein the control logic circuit comprises a first NAND gate, a first inverter, a second NAND gate, a second inverter, a third NAND gate, and a third inverter;

an output terminal of the first NAND gate is connected to an input terminal of the first inverter, an output terminal of the second NAND gate is connected to an input terminal of the second inverter, and an output terminal of the third NAND gate is

connected to an input terminal of the third inverter;

the first NAND gate is configured to receive the first internal delay address, and output a first signal;

the first inverter is configured to receive the first signal, and output a second signal;

the second NAND gate is configured to receive the first signal and the test mode command, and output a third signal;

the second inverter is configured to receive the third signal, and output the test mode enable active signal;

the third NAND gate is configured to receive the second signal and the test mode command, and output a fourth signal; and

the third inverter is configured to receive the fourth signal, and output the test mode enable slave signal.

10. The test circuit according to any one of claims 4 to 9, wherein the self-test circuit comprises a first test sub-circuit, the first test sub-circuit comprises a first logic control sub-circuit and a first latch group, the first logic control sub-circuit is connected to the first latch group, and each of the latches in the first latch group corresponds to one test mode signal.

11. The test circuit according to claim 10, wherein an input terminal of the first logic control sub-circuit is connected to an output terminal of the control logic circuit, an output terminal of the test decoding circuit and an output terminal of the slave latch; and

the first logic control sub-circuit is configured to perform a logic operation according to the test mode enable active signal and the decoding signal, to generate a clock signal and output the clock signal to the first latch group.

12. The test circuit according to claim 11, wherein the first latch group is configured to receive the slave address and the clock signal, determine the test mode signal according to the slave address and the clock signal, and output the test mode signal to the target circuit module.

13. The test circuit according to any one of claims 10 to 12, wherein the first logic

control sub-circuit comprises a first P-type transistor, a first N-type transistor, a second N-type transistor, a third N-type transistor, and a fourth N-type transistor;

a control terminal of the first P-type transistor is connected to an output terminal of the control logic circuit, a first terminal of the first P-type transistor is connected to a power supply terminal, and a second terminal of the first P-type transistor is connected to an input terminal of the first latch group and a first terminal of the first N-type transistor;

a control terminal of the first N-type transistor, a control terminal of the second N-type transistor, and a control terminal of the third N-type transistor are all connected to an output terminal of the test decoding circuit;

a second terminal of the first N-type transistor is connected to a first terminal of the second N-type transistor, a second terminal of the second N-type transistor is connected to a first terminal of the third N-type transistor, and a second terminal of the third N-type transistor is connected to a first terminal of the fourth N-type transistor;

a control terminal of the fourth N-type transistor is connected to the output terminal of the control logic circuit, the first terminal of the fourth N-type transistor is connected to the second terminal of the third N-type transistor, and a second terminal of the fourth N-type transistor is connected to a ground terminal.

14. The test circuit according to any one of claims 4 to 13, wherein the first internal address is 2 bits, the second internal address is 1 bit, and the third internal address is 7 bits.

15. A memory, comprising a control circuit, at least one circuit module, and the test circuit according to any one of claims 1 to 14;

the control circuit being configured to send the input signal to the test circuit; and

the test circuit being configured to receive the input signal, and send the test mode signal to one of the at least one circuit module according to the input signal.