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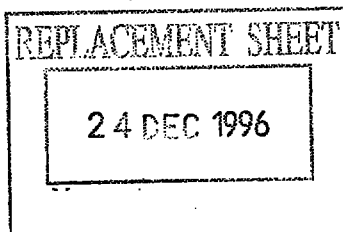
PRODUCT SUMMING CIRCUITRY

ABSTRACT

In processors, in particular digital signal processors, it often happens that products of a chain of pairs of data words must be summed, for example for correlation or convolution operations, in which each data word of each pair may only have one of both values +1 or -1. According to the invention, one data word of each pair is supplied to a summing/subtracting arrangement, instead of being supplied to a multiplier for forming a product, and determines whether the summing/subtracting arrangement carries out a summing or a subtracting operation. One input of the summing/subtracting unit receives the other data words of the pairs of data words and the other input is connected to the output of the accumulator register. A costly multiplier arrangement can thus be dispensed with, or when it is anyway available, it is not used, so that the processor dissipates less power.

FIGURE 1

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REPLACED



This Sheet Has Been Replaced

