

## READING CIRCUIT FOR A RESISTIVE MEMORY CELL

### ABSTRACT

5 A reading circuit for a resistive memory cell is provided, the circuit including a current source, a precharge switch, a comparator circuit including a first input node (*in*-node), and a second *in*-node, the precharge switch configured to couple the current source to the first *in*-node to apply a precharge voltage during a first reading time period, and to decouple the current source during a second reading time period, the comparator circuit  
10 configured to operate during a third reading time period, a memory cell access switch to enable a current flow at least partially during the second and the third reading time periods through a memory cell, the comparator circuit configured to compare a voltage at the first *in*-node with a reference voltage at the second *in*-node and to determine a programming state of the memory cell based on the voltage at the first *in*-node during the  
15 third reading time period.

Figure 3