

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the digital data processing art and more particularly to a new method and apparatus for encoding binary digital data which is particularly suitable to be used in digital data communication systems and digital data storage and retrieval systems.

2. Description of the Prior Art

Data storage capacity of digital data storage and retrieval systems has been gradually increasing, and some improved methods for encoding binary digital data have contributed to the increase of storage data capacity to a large extent. Generally, the method for encoding binary data is required to have the following features:

- (i) large value of T_{min} ;
- (ii) small value of T_{max} ; and
- (iii) DC free,

where T_{min} and T_{max} represent respectively the minimum and maximum distances between encoded signal transitions. The feature (i) means that high frequency spectra of the encoded digital signals is reduced. With this feature, the upper limit of transmission band can be lowered, or storage capacity of the data storage system can be increased. The feature (ii) means that self clocking is possible. With this feature timing shift between the clock and signals is reduced, so that storage capacity of the data storage system can be increased. As a method which is excellent in the features (i) and (ii), so-called "3PM" method is already known as disclosed in U.S. Patent 4,323,931. This method separates input binary data into successive data words each containing 3 data bits and converts each data word to a channel word containing 6 data bits. The 3PM method has such excellent features of $T_{min} = 1.5T$ and $T_{max} = 6T$, but does not have the feature (ii).

In the case of retrieving data from a magnetic storage medium by means of a ring head in which differential signals can be detected, it is possible to detect peak levels of the retrieved signals, so that it is not necessary to be DC free. However, when the retrieved signals contain a large amount of high frequency noises, the differential signals may preferably be integrated prior to being wave-shaped. In this case, a DC free encoding method is desirable. Also, in the case of using a thin-film head showing the magnetoresistance effect in which the differential signals are not retrieved, a DC free encoding method is desired. Moreover, in optical data storage and retrieval systems which require accurate tracking on data tracks, encoded digital signals will be added as noises to the tracking control signal if the encoding method is not DC free.

As a method having all of the above feature (i), (ii) and (iii), so-called "EFM" method is already known which is applied to the "compact disk" (trademark of Philips Corp. and Sony Corp.). This method is discussed together with a number of other methods in an article by Toshi T. Doi in the Journal of the Audio Engineering Society, vol 31, no. 4, April 1983 pages 224-238 entitled "Channel Codings for Digital Audio Recordings". This method realizes a very small value of digital sum variation (DSV, hereafter), where DSV is generally defined as a value obtained by summing data bits of encoded binary data assuming bit '1' as +1 and bit '0' as -1. The EFM method separates input binary data into data words each containing 8 data bits, converts each data word to a channel word containing 14 data bits, inserts 3 merging bits between two channel words, and converts the obtained data to NRZI code data. The merging bits are selected, by referring to the previous DSV and the following channel word, so as to reduce total DSV, thereby to make the encoded data to be DC free. The merging bit selection also takes account of the maximum allowed number of consecutive '0' bits and appropriate merging bits are added which ensure that this maximum number is not exceeded. In this method, however, a complicated decoding circuit must be provided for decoding the 14-bit channel words. If the number of data bits of the channel word would be reduced for simplifying the decoding circuit, then data storage capacity would decrease due to the overhead of the 3 merging bits.

The present invention provides an apparatus for encoding binary data comprising:

converting means adapted to convert a sequence of binary data words each containing N data bits, where N is an integer larger than 1, to a sequence of respective corresponding binary channel words each containing M data bits, where M is an integer larger than N, each channel word having at least one merging

bit at a boundary of the channel word, the value of which may be set to ensure that the sequence of channel words complies with given run-length rules and has minimal digital sum variation;

output means adapted to output said sequence of channel words;

NRZI modulating means arranged to modulate said sequence of channel words into NRZI coded channel codes,

characterized in that:

a predetermined number of said channel words have at least one selective bit, in addition to and separated from said at least one merging bit, which may be either '1' or '0'; and

the apparatus comprises:

means adapted to set the value of the at least one selective bit if present in a channel word to ensure that the sequence of channel words complies with given run-length rules;

means for establishing, for each channel word, whether the value of the at least one merging bit and/or the at least one selective bit if present therein may be changed without contravening the given run-length rules;

means for temporarily storing a signal indicating a channel word in which the value of a bit may be so changed;

means for delaying the output of a first channel word in which the value of a bit may be so changed for a delay period, that period being the time until the next channel word in which the value of a bit may be so changed appears or until a predetermined number of subsequent consecutive channel words in which the

value of no bits may be so changed appear; and

means adapted to set the at least one merging bit and/or the at least one selective bit in the first channel word at the end of the delay period, prior to the output of the first channel word, to have the value which results in a lower absolute value of digital sum variation (DSV) of the channel codes at the end of the delay period, or a lower maximum absolute value of DSV of the channel codes during the delay period.

An advantage of the present invention is that it provides an apparatus for encoding binary data using a method for encoding binary data which has features of DC free and large minimum distance between encoded signal transitions and does not require a complicated decoding circuit.

The conversion may preferably be performed according to the following rules:

(i) two or more '0' bits exist between two '1' bits in the channel word if the channel word contain two or more '1' bits;

(ii) most significant bit or least significant bit of each channel word is made normally '0' as a merging bit, and when bits adjacent to said merging bit at both sides thereof are both '1' the adjacent bits are both made '0' and the merging bit is made '1'; and

(iii) the merging bit is made '0' or '1' so that the absolute value of DSV reduces when a bit preceeding by three bits to the merging bit is '1' and the merging bit is followed by two continuous '0' bits or when two continuous bits just before the merging bit are both '0' and a bit three bits after the merging bit is '1'.

Or, the conversion may preferably be performed according to the following rules:

(i) two or more '0' bits exist between two '1' bits in the channel word if the channel word contains two or more '1' bits;

(ii) most significant bit or least significant bit of each channel word is made normally '0' as a merging bit, and when bits adjacent to the merging bit at both sides thereof are both '1' the adjacent bits are both made '0' and the merging bit is made '1';

(iii) the merging bit is made '0' or '1' so that the absolute value of DSV reduces when a bit preceeding by three bit to the merging bit is '1' and two bits following the merging bit are both '0' or when two bits just before the merging bit are both '0' and a bit three bits after the merging bit is '1'; and

(iv) the specific data word is converted to one of two channel words which differ from each other only in one specific data bit so that the absolute value of DSV reduces.

With the above configuration, even if the number of operations for suppressing DSV is small, DSV can be effectively suppressed because DVS is looked ahead far enough. Accordingly, the DC free feature can be obtained without largely sacrificing the above features (i) and (ii). If the requirement to suppress DC is not so severe, either of the above features (iii) or (iv) may be omitted. Also, the above features (i), (ii) and (iii) can be obtained even if the number of bits of the channel word is small and a conversion rule which requires an easy inverse-conversion is used.

The above and other objects, features and advantages of the present invention will become apparent from the following description taken in connection with the accompanying drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

- Fig. 1 is a block diagram of an embodiment according to the invention;
 Fig. 2 is a conversion table for a 4/8 converter used in the Fig. 1 embodiment;
 Fig. 3 is a block diagram of another embodiment according to the invention;
 Fig. 4 is a logic circuit diagram of an embodiment of a circuit for performing conversion according to the conversion table in Fig. 2;
 Fig. 5 is a logic circuit diagram of an embodiment of a circuit for performing inverse-conversion according to the conversion table in Fig. 2;
 Fig. 6 is another conversion table for a 4/8 converter used in the Fig. 1 or Fig. 2 embodiment;
 Fig. 7 is a temporary inverse-conversion table for a temporary inverse-conversion performed as a first step prior to the inverse-conversion according to the conversion table in Fig. 6;
 Fig. 8 is a logic circuit diagram of an embodiment of a circuit for performing inverse-conversion according to the conversion table in Fig. 6;
 Fig. 9 is a conversion table for a 2/4 converter used in place of the 4/8 converter in the Fig. 1 or Fig. 3 embodiment;
 Fig. 10 is a circuit diagram showing an embodiment of first and second DSV counters used in the Fig. 1 embodiment;
 Fig. 11 is a timing chart showing the operation of the circuit in Fig. 10;
 Fig. 12 is a circuit diagram showing an embodiment of a comparator used in the Fig. 1 embodiment;
 Figs. 13-15 are block diagrams showing other embodiments of converting means used in the Fig. 1 or Fig. 3 embodiment; and
 Fig. 16 is a circuit diagram showing an example of a violation checking circuit used in this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1, a 4/8 converter 1 converts a data word containing 4 input data bits to a channel word containing 8 data bits according to the following conversion rules:

- rule 1: Convert a 4-bit data word to a 8-bit channel word.
 rule 2: If a data word contains a plurality of '1' bits, more than one '0' bits exist between the '1' bits.
 rule 3: Either of the most and least significant bits of each channel word is made '0' as a merging bit.

There exist 19 kinds of channel words which satisfy all of the above three rules. There exist many conversion tables on which the 19 kinds of channel words correspond to 16 kinds of data words. One preferred example of such conversion tables is shown in Fig. 2. Each data word consists of 4 data bits - a_3 , a_2 , a_1 and a_0 - in the order from the most significant bit (MSB) to the least significant bit (LSB), and each channel word consists of 8 data bits - b_7 , b_6 , b_5 , b_4 , b_3 , b_2 , b_1 and b_0 - in the order from the MSB to the LSB. In this conversion table, each of three kinds of data words 0000, 0001 and 1100 corresponds to two kinds of channel words. We call these three kinds of data words "extraordinary data words" and the other data words "ordinary data words". Each extraordinary data word correspond to two kinds of channel words: one in which bit b_4 indicated by * is '0' and the other in which bit b_4 indicated by * is '1'. We call this bit b_4 "extraordinary bit". Bit b_0 is a merging bit for connecting channel words.

The 4/8 converter 1, when converts the extraordinary data word, temporarily make the extraordinary bit b_4 '0' and sets an extraordinary flag. A violation checking circuit 2 converts each channel word to a serial data starting from bit b_0 and tests whether the number of continuous '0' bits between two '1' bits is between 2 and 11. Since the conversion table in Fig. 2 is made such that at least two '0' bits exist between two '1' bits in each channel word, the case in which the number of '0' bits between two '1' bits becomes one or zero occurs only when the bits adjacent to the merging bit b_0 at both sides thereof are both '1'. In this particular case, the violation checking circuit 2 makes the merging bit b_0 '1' and both of the bits adjacent to the merging bit b_0 at both side thereof '0', so that the number of '0' bits between two '1' bits is always more than one. Since the merging bit b_0 is always zero except the above particular case, inverse-conversion of encoded data during decoding can be performed in such a manner that when the merging bit b_0 is '0' the encoded data is inverse-converted according to the conversion table, and when the merging bit b_0 is '1' the merging bit b_0 is changed to '0' and the both of the bits adjacent to the merging bit b_0 at both sides thereof are changed to '1'.

Further, according to the conversion table in Fig. 2, when all of the extraordinary bits in the extraordinary data words are '1' the number of continuous '0' bits between two '1' bits is less than 12 regardless of the connection of channel words. Accordingly, the violence checking circuit 2 will make the extraordinary bit '1' when detects 12 or more number of continuous '0' bits between two '1' bits.

By performing violation check as described above, features of $T_{\min} = 1.5T$ and $T_{\max} = 6T$ can be obtained. The violation checking circuit 2 outputs from an output terminal 2a first the lower 4 bits and then the upper 4 bits of each channel word separately each 4-bit data in the serial order from the LSB to the MSB. When the upper 4 bits b_4 , b_5 , b_6 and b_7 are outputted the extraordinary flag is set with respect to the channel word, and if the extraordinary bit b_4 is '0' an arbitrary flag 2c is set and outputted from an output terminal 2c. The arbitrary flag indicates that the channel word is selectable on bit b_0 or bit b_4 . When the lower 4 bits b_0 , b_1 , b_2 and b_3 are outputted the arbitrary flag 2c is set when bit b_5 of the preceding channel word is '1' and bits b_1 and b_2 following the merging bit b_0 are both '0' or when bits b_6 and b_7 of the preceding channel word are both '0' and bit b_3 following the merging bit b_0 is '1'. In these cases, it will never occur that both of bits b_7 and b_1 at both sides of the merging bit b_0 are '1' and that even if the merging bit b_0 is made '1' the number of '0' bits between two '1' bits will never become less than two. Accordingly, the above cases can be discriminated from the case the merging bit b_0 was made '1' by the violation check.

As described above, bit b_0 or b_4 of the channel word outputted from the output terminal 2a is not fixed but is made temporary '0' as a pending bit when the arbitrary flag 2c is set. From an output terminal 2b of the violation checking circuit 2 is outputted a temporary channel code of NRZI code following the pending bit. A first DSV counter 3 counts DSV including the temporary channel code, and a second DSV counter 4 counts DSV including an inverted temporary channel code which is obtained by inverting the temporary channel code with an inverter 19. A comparator 12 compares the absolute values of DSV obtained by the first and second DSV counters 3 and 4.

A shift register 5 converts each of the serial upper 4 bits and lower 4 bits of the channel word outputted from the output terminal 2a of the violation checking circuit 2 to a parallel 4-bit data (half word, hereafter). A controller 6 controls a data selector 7 to apply the half word outputted from the shift register 5 to a data input port of a channel word storage memory 8, and at the same time controls an address selector 9 to apply a write address outputted from a write address counter 10 to an address input port of the channel word storage memory 8, so that the half word is written into the channel word storage memory 8. The write address counter 10 is incremented when the above writing operation is completed. When the arbitrary flag 2c is set the output address of the write address counter 10 is stored into a pointer register 11 before the write address counter 10 is incremented. The above operation is repeated thereby to store half words into the channel word storage memory 8.

Among the half words stored in the channel word storage memory 8 the half word stored in the address indicated by the address stored in the pointer register 11 is a temporary half word in which the extraordinary bit b_4 or the merging bit b_0 is '0'. The extraordinary bit b_4 or the merging bit b_0 may be made '1'. The value of bit b_4 or bit b_0 will be determined later in the following manner.

When the arbitrary flag 2c is set again by the violation checking circuit 2 the controller 6 refers to the comparison result of the comparator 12. If the absolute value of DSV outputted from the second DSV counter 4 is smaller than that outputted from the first DSV counter 3, the controller 6 controls the data selector 7 and the address selector 9 to write '1' into bit b_0 or bit b_4 of the half word stored in the channel word storage memory 8 in the address indicated by the address data stored in the pointer register 11. Oppositely, if the absolute value of DSV outputted from the first DSV counter 3 is smaller than that from the second DSV counter 4, bit b_0 or bit b_4 of the half word stored in the channel word storage memory 8 in the address indicated by the address data stored in the pointer register 11 remains unchanged or is written with '0' again. In this manner the value of the temporary half word is established. At this time, the controller 6 loads the DSV having smaller absolute value from one of the first and second DSV counters to the other.

When a predetermined number of half words are stored into the channel word storage memory 8 the controller 6 controls the data selector 7 and the address selector 9 to read out from the memory 8 the half word stored in the address indicated by the address data outputted from a read address counter 13. The read-out half words are each converted to a serial data by a shift register 14. A NRZI modulator 15 modulates each of the serial half words outputted from the shift register 14 into a NRZI code data as a finally obtained channel code.

When a temporary half word has been written into the channel word storage memory 8 and no other temporary half word has been written after that, or the arbitrary flag 2c has not been set, until the predetermined number of half words is written into the memory 8, the temporary half word would be read out as it is without DSV control. In order to eliminate this problem the controller 6 changes the temporary half word in the memory 8 to a half word having an established content in accordance with the comparison result of the comparator 12 at this moment before the half word is read out from the memory 8.

Timing signals such as bit clocks and word clocks necessary for the elements configuring the above embodiment are produced from a master clock signal by a timing generator 16. In the above embodiment,

4/8 converter 1, violation checking circuit 2, first and second DSV counters 3 and 4, shift register 5, controller 6, data selector 7, channel word storage memory 8, address selector 9, write and read address counters 10 and 13, pointer register 11, comparator 12 and timing generator 16 constitute a converting means 17; and shift register 14 and NRZI modulator 15 constitute a NRZI modulating means 18.

In the above embodiment each channel word is divided into two half words and the half words are stored into the channel word storage memory 8. However, each channel word may be stored as it is into the memory 8 without being divided. In this case, the address where a temporary channel word is stored may be stored in the pointer register 11 and an information showing a pending bit should be stored in a memory. Further, instead of storing the channel words into the channel word storage memory, the data "words may be stored in a data word storage memory. Furthermore, the first and second DSV counters 3 and 4 may be substituted by a single DSV counter for counting DSV of channel words and an accumulator for accumulating the output values of the DSV counter. Another embodiment modified in this way is shown in Fig. 3.

Referring to Fig. 3, a controller 24 controls the data selector 7 and the address selector 9 to write data words into a data word storage memory 20 according to the addresses outputted from the write address counter 10. If the data word to be written into the memory 20 is an extraordinary data word the 4/8 converter 1 sets an extraordinary flag. The violation checking circuit 2 refers to the extraordinary flag and performs violation check. That is, if the extraordinary bit or the merging bit is selectable so as to reduce DSV, the violation checking circuit 2 sets the arbitrary flag and outputs it from the output terminal 2c. If both of the extraordinary bit and the merging bit are selectable, either one of them may be selected by fixing the other to be '0' or '1'. This is advantageous in that it is not necessary to provide two kinds of arbitrary flags corresponding to the extraordinary and merging bits.

When the arbitrary flag is set an accumulator 22 stores the value of DSV at this moment and a DSV counter 21 is cleared. At the same time, the address in which the data word corresponding to the arbitrary flag is written is stored in the pointer register 11. The violation checking circuit 2 outputs from the output terminal 2a a temporary channel word containing the selectable bit which is made temporary '0'. After that, the DSV counter 21 counts DSV of the channel words outputted from the violation checking circuit 2. A comparator 23 compares the sign of the DSV count output from the DSV counter 21 with the sign of the DSV stored in the accumulator 22.

Under this condition, when an extraordinary data word, which cannot be converted in real time, is inputted again the arbitrary flag is set again. When the arbitrary flag is set again a controller 24, referring to the comparison result of the comparator 23, will make '1' the extra-bit contained in the data word stored in the address in the data word storage memory 20 indicated by the address stored in the pointer register 11 when the signs of the DSV are equal to each other, and will make '0' the same extra-bit when the signs are different from each other. Further, the controller 24 controls the accumulator 22 to subtract the output value of the DSV counter 21 from the value stored in the accumulator 22 when the comparator 23 shows the signs of the both values are equal to each other, and to add the output value of the DSV counter 21 to the value stored in the accumulator 22 when the comparator 23 shows the signs of the both values are different from each other. Then, the DSV counter 21 is cleared and the above operation will be repeated.

The controller 24 controls the data selector 7 and the address selector 9 to read out the data words stored in the data word storage memory 20 with a delay time necessary for the temporary channel word to be established. The read-out data words are converted to channel words by a secondary 4/8 converter 25. Each channel word outputted from the secondary 4/8 converter 25 is subjected to violation check at a secondary violation checking circuit 26. The secondary 4/8 converter 25, when converting an extraordinary data word, makes the value of the extraordinary bit to be the same as the value of the extra-bit. The channel words subjected to violation check are then applied to the NRZI modulating means 18 where they are modulated to be NRZI coded channel codes. In the above way the absolute value of DSV of the channel codes are controlled to be small, in this embodiment, controller 24, data and address selectors 7 and 9, secondary 4/8 converter 25 and secondary violation checking circuit 26 constitute a read-out means.

The conversion table in Fig. 2 used for the conversion at the 4/8 converter 1 in the above two embodiments will further be described in more detail. This conversion table is made such that the conversion and inverse-conversion between the data words and the channel words are easy. That is, except the data word 0111, there exist fixed relations between the upper two bits (a_3, a_2) of the data words and the upper three bits (b_7, b_6, b_5) of the channel words and between the lower two bits (a_1, a_0) of the data words and the lower three bits (b_2, b_1, b_0) of the channel words, as follows:

	data words				channel words		
5	$\left(\begin{array}{cc} a_3 & a_2 \\ a_1 & a_0 \end{array} \right.$	$\longleftrightarrow$	$\begin{array}{ccc} b_7 & b_6 & b_5 \\ b_2 & b_1 & b_0 \end{array}$	$\left. \right)$			
	0 0	$\longleftrightarrow$	0 0 0				
10	0 1	$\longleftrightarrow$	0 0 1				
	1 0	$\longleftrightarrow$	0 1 0				
15	1 1	$\longleftrightarrow$	1 0 0				

This simple relation between the data words and the channel words is advantageous in that the conversion and inverse-conversion between the words can be achieved by a simple logical circuit configuration.

Fig. 4 shows an example of the 4/8 converter for converting the 4-bit data words to the 8-bit channel words according to the conversion table in Fig. 2. In the configuration of Fig. 4 bit b_0 is always '0'. The value of bit b_0 is determined later by the violation checking circuit so as to properly connect channel words. Fig. 5 shows an example of a 8/4 converter for inversely converting the 8-bit channel words to the 4-bit data words according to the conversion table in Fig. 2 in a decoding system.

In addition to the above advantage the conversion table in Fig. 2 provides a large T_{min} ($T_{min} = 1.5T$) and DC free feature.

Another 4/8 conversion table is shown in Fig. 6 in which with respect to each of three data words 0000, 0001 and 1000 are selectable two channel words: one in which bit b_4 indicated by * is '0'; and the other in which bit b_4 indicated by * is '1'. Data words corresponding to channel words having same bit pattern for bits b_5 , b_6 and b_7 are so defined to have hamming distances of one or zero from a specified 4-bit value. This makes the inverse-conversion easy. The inverse-conversion is performed in such a way that temporary data words are produced corresponding to the four kinds of values of sign word consisting of bits b_7 , b_6 and b_5 as shown in Fig. 7, and bits a_2 , a_1 and a_0 of the temporary data words are respectively inverted when $b_7 = '1'$, $b_6 = '1'$ and $b_5 = '1'$ thereby to obtain the data words according to the conversion table in Fig. 6. Here, data word 0011 is an exception. The above conversion can be easily performed by using a ROM table. Fig. 8 shows an example of the circuit for performing the inverse-conversion.

The present invention can be effectively applied to any N/M conversion (N is an integer larger than 1 and M is an integer larger than N) for converting data words each containing N data bits to channel words each containing M data bits.

Fig. 9 shows an example of 2/4 conversion table, in which each data word consists of two data bits a_1 and a_0 ($a_1 = \text{MSB}$, $a_0 = \text{LSB}$), and each channel word consists of four data bits bits b_3 , b_2 , b_1 and b_0 ($b_3 = \text{MSB}$, $b_0 = \text{LSB}$). In this conversion table, at least one '0' bit always exists between two '1' bits in every channel word and LSB b_0 of every channel word is '0'. This means that in a channel code produced by time-serially connecting the channel words there always exists at least one '0' bit between two '1' bits. Accordingly, the NRZI coded channel code has the feature of $T_{min} = T$.

Further, since there are five kinds of channel words and four kinds of data words, data word 00, for example, may be made to correspond to two kinds of channel words in which bit b_1 indicated by * is respectively '0' and '1' as shown in Fig. 9 thereby enabling the control to reduce the absolute value of DSV. Furthermore, if the channel words are outputted in the order from LSB to produce the time-serial channel code and if bit b_3 of a preceeding channel word and bit b_1 of the following channel word are both '0', then the bit b_0 therebetween may be either '0' or '1'. In this case, the absolute value of DSV can be reduced by controlling the value of bit b_0 . An apparatus for encoding binary data according to this 2/4 conversion can be easily configured similarly to the embodiments in Figs. 1 and 3.

Now, the first and second DSV counters 3 and 4 will be described in more detail with reference to Figs. 10 and 11. Fig. 10 shows an example of the circuit configurations of the first and second DSV counter 3 and 4, and Fig. 11 shows signal waveforms at portions A to G in Fig. 10. A temporary channel code A outputted from the output terminal 2b of the violation checking circuit 2 is latched by a D-flip-flop (DFF, hereafter) 31a operated by a channel bit clock B synchronized with the bit cell of the temporary channel code A. When an

output C of DFF 31a has the same state as that of the input A an output D of an EX-OR gate 33a becomes '0' thereby to enable an up/down counter 34a. If the states of the output C and the input A of DFF 31a are both '1', an output E of a NAND gate 32a becomes '1' thereby to make the up/down counter 34a operate as an up counter. Otherwise the up/down counter 34a operates as a down counter. Under the above control the up/down counter 34a counts a clock F which occurs with respect to every two bits of the channel code, so that a count value G changes as shown in Fig. 11. Since the up/down counter 34a operates at every two bits of the channel code, the operating speed of the up/down counter 34a can be reduced to half the repetition frequency of the channel code. DFF 31a, NAND gate 32a, EX-OR gate 33a and up/down counter 34a constitute the first DSV counter 3. Similarly, the second DSV counter 4 is constituted by a DFF 31b, a NAND gate 32b, an EX-OR gate 33b and an up/down counter 34b, and operates similarly to the first DSV counter 3. However, the second DSV counter 4 is inputted with the channel code A through the inverter 19. Accordingly, the count value of the first DSV counter 3 is the value of DSV when the extraordinary bit, or selectable bit, (b_4) of the temporary channel word is temporarily made '0', and the count value of the second DSV counter 4 is the value of DSV when the above extraordinary bit is temporarily made '1'. When the value of the above extraordinary bit is determined according the comparison result of the absolute values of DSV of the first and second DSV counters, the controller 6 loads the smaller one of the absolute values of DSV to the DSV counter outputting the larger one. The second DSV counter 4 may be so configured that the up/down counter 34b is enabled when the output D of the EX-OR gate 33a is '0' and the up/down selection of the up/down counter 34b is determined by a signal obtained by inverting the output E of the NAND gate 32a. By this configuration, DFF 31b, NAND gate 32b and EX-OR gate 33b can be removed.

The comparator 12 can be comprised by two complementing circuits 40a, 40b for respectively producing the absolute values of DSV from the values of DSV obtained by the first and second DSV counters 3 and 4, and a magnitude comparator 41 for comparing the absolute values of DSV as shown in Fig. 12. Since each of the first and second DSV counters has the up/down counter, negative value is expressed as 2's complement. Accordingly, each complementing circuit may produce 2's complement. However, each complementing circuit may be configured to produce 1's complement as shown in Fig. 12. In this case, if the two inputs have the same value, the positive DSV may be selected because the absolute value of the negative DSV decreases by one when converted to its 1's complement.

The operation of the comparator 12 shown in Fig. 12 will now be described. The complementing circuit 40a produces 1's complement of the count value of the first DSV counter if the count value is a negative value. The complementing circuit 40b produces 1's complement of the count value of the second DSV counter if the count value is a negative value. The magnitude comparator 41 compares the output values of the complementing circuits 40a and 40b. The magnitude comparator 41 has two output terminals 41a and 41b. If the output value of the complementing circuit 40b is larger than that of the complementing circuit 40a, only the output terminal 41b becomes '1', and if the output values of the complementing circuits 40a and 40b are equal to each other, only the output terminal 41a becomes '1'. A circuit composed of a NAND gate 42 and NOR gate 43 outputs a signal of '1' or '0' according a combination of the signals at the output terminals 41a and 41b and the sign bit (MSB) of the count value of the first DSV counter 3. The output of this circuit becomes '0' when the absolute value of the count value of the first DSV counter 3 is smaller than that of the second DSV counter 4, and otherwise becomes '1'. In other words, the output of the comparator 12 shows which one of the absolute values of DSV produced by the first and second DSV counters 3 and 4 is smaller or larger than the other.

In the above described embodiments, the final value of the temporary channel word is determined so that the value of DSV at that moment decreases. However, the final value of the temporary channel word may be determined so that the peak value of DSV by that moment decreases, and an example configured in such manner is shown in Fig. 13. Referring to Fig. 13, a comparator 51a, which has the same configuration as the comparator 12, compares the absolute value of the count value of the first DSV counter 3 with the absolute value of a value stored in a maximum DSV register 50a. If the absolute value of the count value of the first DSV counter 3 is larger than the absolute value of the value stored in the maximum DSV register 50a, the comparator 51a allows the maximum DSV register 50a replace the stored value by the count value of the first DSV counter 3 at that moment. Accordingly, the value stored in the maximum DSV register 50a is the value of DSV having maximum absolute value by that moment. A maximum DSV register 50b and a comparator 51b operate in the same way to store the maximum value of DSV of the second DSV counter 4 in the maximum DSV register 50b. The comparator 12 compares the absolute value of the values stored in the maximum DSV registers 50a and 50b. According to this comparison result the controller 6 controls to establish the value for the temporary channel word, or to convert the data word which remains unconverted to an established channel word, and then maximum DSV registers 50a and 50b

are cleared. This method is effective to further improve the DC component suppressing ability.

As described in the foregoing description, DC component can be suppressed by using the extraordinary data words. However, if the ordinary data words continuously appear for a long time, the above described control will not be caused, which means that DC component cannot be suppressed. This problem can be solved by inserting an extraordinary data word periodically into the data word train. This method can be realized by, for example, a circuit as shown in Fig. 14.

Referring to Fig. 14, a SYNC word generator 60 synchronized with the word clock from the timing generator 16 outputs a data request. An external device (not shown) outputs a binary data word in response to the data request. The binary data word is supplied to a data selector 61 which usually transfers the binary data word to the 4/8 converter 1. The SYNC word generator, when received a predetermined number of word clocks, outputs a specific SYNC word and controls the data selector 61 to transfer this SYNC word to the 4/8 converter 1. After that the SYNC word generator restarts counting the number of word clocks from 0. By repeating the above operation the data inputted to the 4/8 converter 1 periodically include the SYNC words. The SYNC word is selected to be an extraordinary data word. Accordingly, the above described control to reduce DSV can be periodically done to assure the DC free feature.

This effect can be obtained also by a circuit configuration as shown in Fig. 15. Referring to Fig. 15, SYNC marks are contained periodically in the input binary data. A random data generator 70 synchronized with the SYNC marks generates a periodically circulating pseudo-random data sequence. The input binary data are scrambled with the pseudo-random data sequence by an EX-OR gate 71. The scrambled binary data will later be scrambled with the same pseudo-random data sequence by an EX-OR gate to be recovered as the original binary data. The pseudo-random data generator may be realized by, for example, configuring a feedback loop comprised by shift registers and EX-OR gates to obtain maximum length sequence.

Fig. 16 shows an example of the violation checking circuit 2. Each channel word outputted from the 4/8 converter 1 is transferred through latches 80 and 81 to a shift register 82 in synchronization with the word clock. The extraordinary flag is transferred through D-flip-flops 88 and 89 to a D-flip-flop 90. However, if a channel word containing the extraordinary bit is latched by the latch 81 and more than eleven continuous '0' bits are detected by a Tmax checking circuit 87, the transfer of the extraordinary flag corresponding to the channel word is inhibited. In this case, the extraordinary bit is made '1' by means of an OR gate 91 when the channel word is loaded to the shift register 82. A Tmin checking circuit 83 tests bit b_1 of the channel word latched by the latch 80 and bit b_7 of the channel word latched by the latch 81, and, when these bits are both '1', makes these bits '0' by means of AND gates 85 and 86 and also makes '1' bit b_0 of the channel word latched by the latch 80 by means of an OR gate 84. If bit b_0 of the channel word loaded to the shift register 82 is selectable to be '0' or '1' so as to control DSV as described before, a merging bit checking circuit 93 output a signal '1' which is then latched by a D-flip-flop 95. A data selector 94 selects the output signal of the D-flip-flop 95 when data bits b_0 , b_1 , b_2 and b_3 are outputted in serial from the shift register 82, and selects the output signal of the D-flip-flop 90 when data bits b_4 , b_5 , b_6 and b_7 are outputted in serial from the shift register 82. The signal selected by the data selector 94 is the arbitrary flag 2c.

Claims

1. An apparatus for encoding binary data, comprising:

converting means adapted to convert a sequence of binary data words each containing N data bits, where N is an integer larger than 1, to a sequence of respective corresponding binary channel words each containing M data bits, where M is an integer larger than N, each channel word having at least one merging bit at a boundary of the channel word, the value of which may be set to ensure that the sequence of channel words complies with given run-length rules and has minimal digital sum variation;

output means adapted to output said sequence of channel words;

NRZI modulating means (18) arranged to modulate said sequence of channel words into NRZI coded channel codes,

characterized in that:

a predetermined number of said channel words have at least one selective bit (b_4), in addition to and separated from said at least one merging bit (b_0), which selective bit may be either '1' or '0'; and

the apparatus comprises:

means adapted to set the value of the at least one selective bit if present in a channel word to ensure that the sequence of channel words complies with given run-length rules;

means (2) for establishing, for each channel word, whether the value of the at least one merging bit



are cleared. This method is effective to further improve the DC component suppressing ability.

As described in the foregoing description, DC component can be suppressed by using the extraordinary data words. However, if the ordinary data words continuously appear for a long time, the above described control will not be caused, which means that DC component cannot be suppressed. This problem can be solved by inserting an extraordinary data word periodically into the data word train. This method can be realized by, for example, a circuit as shown in Fig. 14.

Referring to Fig. 14, a SYNC word generator 60 synchronized with the word clock from the timing generator 16 outputs a data request. An external device (not shown) outputs a binary data word in response to the data request. The binary data word is supplied to a data selector 61 which usually transfers the binary data word to the 4/8 converter 1. The SYNC word generator, when received a predetermined number of word clocks, outputs a specific SYNC word and controls the data selector 61 to transfer this SYNC word to the 4/8 converter 1. After that the SYNC word generator restarts counting the number of word clocks from 0. By repeating the above operation the data inputted to the 4/8 converter 1 periodically include the SYNC words. The SYNC word is selected to be an extraordinary data word. Accordingly, the above described control to reduce DSV can be periodically done to assure the DC free feature.

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Claims

1. An apparatus for encoding binary data, comprising:

converting means adapted to convert a sequence of binary data words each containing N data bits, where N is an integer larger than 1, to a sequence of respective corresponding binary channel words each containing M data bits, where M is an integer larger than N, each channel word having at least one merging bit at a boundary of the channel word, the value of which may be set to ensure that the sequence of channel words complies with given run-length rules and has minimal digital sum variation;

output means adapted to output said sequence of channel words;

NRZI modulating means (18) arranged to modulate said sequence of channel words into NRZI coded channel codes,

characterized in that:

a predetermined number of said channel words have at least one selective bit (b_4), in addition to and separated from said at least one merging bit (b_0), which selective bit may be either '1' or '0'; and

the apparatus comprises:

means adapted to set the value of the at least one selective bit if present in a channel word to ensure that the sequence of channel words complies with given run-length rules;

means (2) for establishing, for each channel word, whether the value of the at least one merging bit



and/or the at least one selective bit if present therein may be changed without contravening the given run-length rules;

means (11) for temporarily storing a signal (2c) indicating a channel word in which the value of a bit may be so changed;

means for delaying the output of a first channel word in which the value of a bit may be so changed for a delay period, that period being the time until the next channel word in which the value of a bit may be so changed appears or until a predetermined number of subsequent consecutive channel words in which the value of no bits may be so changed appear; and

means (6, 9) adapted to set the at least one merging bit and/or the at least one selective bit in the first channel word at the end of the delay period, prior to the output of the first channel word, to have the value which results in a lower absolute value of digital sum variation (DSV) of the channel codes at the end of the delay period, or a lower maximum absolute value of DSV of the channel codes during the delay period.

2. An apparatus according to claim 1, wherein each of said predetermined number of channel words has a single selective bit.
3. An apparatus according to claim 1 or 2, wherein each of said channel words has a single merging bit.
4. An apparatus according to claim 1, wherein said converting means (17) includes: pseudo-random data generating means (70) for generating pseudo-random data which circulates in synchronization with input data words; and scrambling means (71) for scrambling said input data words with said pseudo-random data, and wherein said converting means (17) converts output data of said scrambling means to said channel words.
5. An apparatus according to claim 1 or 2, wherein said converting means (17) performs conversion according to the following rules:
 - (i) two or more '0' bits exist between two '1' bits in a channel word if said channel word contains two or more '1' bits;
 - (ii) the most significant bit or the least significant bit of each channel word is made initially '0' as a merging bit, and when both bits adjacent to said merging bit are '1' both said adjacent bits are made '0' and said merging bit is made '1'; and
 - (iii) said merging bit is made '0' or '1' so that the absolute value of DSV reduces when a bit preceding said merging bit by three bits is '1' and said merging bit is followed by two consecutive '0' bits or when two consecutive bits immediately preceding said merging bit are both '0' and the bit three bits after said merging bit is '1'.
6. An apparatus according to claim 1, wherein said converting means (17) includes: a converter (1) for converting said data words to initial channel words; a channel word storage memory (8) for storing said initial channel words; a pointer register (11) for storing an address in which an initial channel word in which it has been established that a bit may be so changed is stored in said memory; and means (6, 7, 9, 10, 13) for writing a final channel word into said address stored in said pointer register at the end of said delay period.
7. An apparatus according to claim 1, wherein said converting means (17) includes: a data word storage memory (20) for storing said data words and their extra-bits; read-out means (25, 26) for converting said data words stored in said memory to said channel words with reference to said extra-bits; a pointer register (11) for storing an address in which a data word, the channel word for which has a bit which may be so changed, and its extra-bit are stored in said memory; and means (7, 9, 24) for setting said extra-bit of said data word stored in said memory in said address stored in said pointer register so that said extra-bit indicates the established channel word corresponding to said data word.
8. A method for encoding binary data, comprising the steps of:

converting a sequence of binary data words each containing N data bits, where N is an integer larger than 1, to a sequence of respective corresponding binary channel words each containing M data bits, where M is an integer larger than N, each channel word having at least one merging bit at a boundary of the channel word, the value of which may be set to ensure that the sequence of channel words complies with given run-length rules and has minimal digital sum variation;



- outputting said sequence of channel words;
modulating said sequence of channel words into NRZI coded channel codes,
characterized in that:
- a predetermined number of said channel words have at least one selective bit (b4), in addition to and separated from said at least one merging bit (b0), which selective bit may be either '1' or '0';
 - said method comprises:
 - setting the value of the at least one selective bit if present in a channel word to ensure that the sequence of channel words complies with given run-length rules;
 - establishing for each channel word, whether the value of the at least one merging bit and/or the at least one selective bit if present therein may be changed without contravening the given run-length rules;
 - temporarily storing a signal (2c) indicating a channel word in which the value of a bit may be so changed;
 - wherein the output of a first channel word in which the value of a bit may be so changed is delayed for a delay period, that period being the time until the next channel word in which the value of a bit may be so changed appears or until a predetermined number of subsequent consecutive channel words in which the value of no bit may be so changed appear; and
 - wherein the at least one merging bit and/or the at least one selective bit in the first channel word is set at the end of the delay period, prior to the output of the first channel word, to have the value which results in a lower absolute value of digital sum variation (DSV) of the channel codes at the end of the delay period, or a lower maximum absolute value of DSV of the channel codes during the delay period.
9. A method according to claim 8, wherein each of said predetermined number of channel words has a single selective bit.
10. A method according to claim 8 or 9, wherein each of said channel words has a single merging bit.
11. A method according to claim 8 or 9, wherein the conversion of said data words to said channel words is performed according to the following rules:
- (i) two or more '0' bits exists between two '1' bits in a channel word if said channel word contains two or more '1' bits;
 - (ii) the most significant bit or the least significant bit of each channel word is made initially '0' as a merging bit, and when both bits adjacent to said merging bit are '1' both said adjacent bits are made '0' and said merging bit is made '1'; and
 - (iii) said merging bit is made '0' or '1' so that the absolute value of DSV reduces when a bit preceding said merging bit by three bits is '1' and said merging bit is followed by two consecutive '0' bits or when two consecutive bits immediately preceding said merging bit are both '0' and the bit three bits after said merging bit is '1'.

40 Patentansprüche

1. Vorrichtung zur Binärcodierung von Daten, enthalten:
- eine Wandlereinrichtung zum Umwandeln einer Folge von binären Datenwörtern, die jeweils N Datenbits enthalten, wobei N eine ganze Zahl größer 1 ist, in einer Folge jeweils entsprechender binärer Kanalwörter, die jeweils M Datenbits enthalten, wobei M eine ganze Zahl größer N ist, jedes Kanalwort wenigstens ein Bindebit an einem Ende des Kanalworts hat, dessen Wert so eingestellt sein kann, daß sichergestellt ist, daß die Folge von Kanalwörtern mit gegebenen Lauflängenregeln verträglich ist und eine minimale Digitalsummenschwankung aufweist;
 - eine Ausgabereinrichtung zum Ausgeben der Folge von Kanalwörtern;
 - eine NRZI-Modulationseinrichtung (18) zum Modulieren der Folge von Kanalwörtern in NRZI-codierte Kanalwörter,
- dadurch gekennzeichnet, daß:
- eine vorbestimmte Anzahl der Kanalwörter wenigstens ein selektives Bit (b4) aufweist, das zusätzlich zu und getrennt von dem wenigstens einen Bindebit (b0) vorhanden ist und das entweder "1" oder "0" sein kann;
 - die Vorrichtung enthält:
 - eine Einrichtung zum Setzen des Wertes des wenigstens einen selektiven Bits, wenn es in einem Kanalwort vorhanden ist, um sicherzustellen, daß die Folge von Kanalwörtern zu gegebenen Lauflängen-



genregeln paßt;

eine Einrichtung (2) zum Ermitteln für jedes Kanalwort, ob der Wert des wenigstens einen Bindebits und/oder des wenigstens einen selektiven Bits, sofern es darin enthalten ist, geändert werden kann, ohne mit den gegebenen Lauflängenregeln zu kollidieren;

eine Einrichtung (11) zum vorübergehenden Speichern eines Signals (2c), das ein Kanalwort bezeichnet, in dem der Wert eines Bits so geändert werden kann;

eine Einrichtung zum Verzögern der Ausgabe von wenigstens einem Kanalwort, in dem der Wert eines Bits so verändert werden kann, um eine Verzögerungsperiode, wobei diese die Zeit bis zum Auftreten des nächsten Kanalworts ist, in dem der Wert eines Bits so verändert werden kann, oder bis zum Auftreten einer vorbestimmten Anzahl nachfolgender aufeinanderfolgender Kanalwörter, in denen Wert keines Bits so geändert werden kann;

eine Einrichtung (6,9) zum Einstellen des wenigstens einen Bindebits und/oder des wenigstens selektiven Bits in dem ersten Kanalwort am Ende der Verzögerungsperiode vor der Ausgabe des ersten Kanalworts auf den Wert, der zu einem niedrigeren Absolutwert der Digitalsummenschwankung (DSV) der Kanalcodes am Ende der Verzögerungsperiode führt oder zu einem niedrigeren maximalen Absolutwert der DSV der Kanalcodes während der Verzögerungsperiode führt.

2. Vorrichtung nach Anspruch 1, bei der jedes der vorbestimmten Anzahl von Kanalwörtern ein einzelnes selektives Bit hat.

3. Vorrichtung nach Anspruch 1 oder 2, bei der jedes der Kanalwörter ein einzelnes Bindebit hat.

4. Vorrichtung nach Anspruch 3, bei der die Umwandlungseinrichtung (17) enthält: eine Pseudo-Zufallsdatenerzeugungseinrichtung (70) zum Erzeugen von Pseudo-Zufallsdaten, die synchron zu den eingegebenen Datenwörtern umlaufen; und eine Vermischungseinrichtung (71) zum Vermischen der eingegebenen Datenwörter mit den Pseudo-Zufallsdaten, und wobei die Umwandlungseinrichtung (17) die ausgegebenen Daten der Vermischungseinrichtung in die Kanalwörter umwandelt.

5. Vorrichtung nach Anspruch 1 oder 2, bei der die Umwandlungseinrichtung in (17) die Umwandlung nach den folgenden Regeln ausführt:

(i) zwei oder mehr "0"-Bits sind zwischen zwei "1"-Bits in einem Kanalwort vorhanden, wenn das Kanalwort zwei oder mehr "1"-Bits enthält;

(ii) das höchstwertige Bit oder das niedrigstwertige Bit eines jeden Kanalworts wird anfänglich "0" als Bindebit gemacht, und wenn beide Bits benachbart dem Bindebit gleich "1" sind, dann werden diese beiden benachbarten Bits zu "0" gemacht und das Bindebit wird zu "1" gemacht; und

(iii) das Bindebit wird zu "0" oder "1" gemacht, so daß der Absolutwert der DSV abnimmt, wenn ein dem Bindebit um drei Bits vorausgehendes Bit gleich "1" ist und dem Bindebit zwei aufeinanderfolgende "0"-Bits nachfolgen oder wenn zwei aufeinanderfolgende Bits, die dem Bindebit unmittelbar vorausgehen, beide "0" sind und das drei Bits hinter dem Bindebit liegende Bit gleich "1" ist.

6. Vorrichtung nach Anspruch 1, bei der die Umwandlungseinrichtung (17) enthält: einen Wandler (1) zum Umwandeln der Datenwörter in anfängliche Kanalwörter; einen Kanalwortspeicher (8) zum Speichern der anfänglichen Kanalwörter; ein Zeigerregister (11) zum Speichern einer Adresse, an der ein anfängliches Kanalwort, in dem eingerichtet worden ist, daß ein Bit so geändert werden kann, in dem Speicher gespeichert ist; und eine Einrichtung (6, 7, 9, 10, 13) zum Einschreiben eines endgültigen Kanalworts an der Adresse, die in dem Zeigerregister gespeichert ist, am Ende der Verzögerungszeit.

7. Vorrichtung nach Anspruch 1, bei der die Umwandlungseinrichtung (17) enthält: einen Datenwortspeicher (20) zum Speichern der Datenwörter und ihrer Extrabits; eine Ausleseeinrichtung (25, 26) zum Umwandeln der in dem Speicher gespeicherten Datenwörter in Kanalwörter mit Bezug auf die Extrabits; ein Zeigerregister (11) zum Speichern einer Adresse, an der ein Datenwort, dessen Kanalwort ein Bit hat, das so geändert sein kann, und sein Extrabit in dem Speicher gespeichert sind; und eine Einrichtung (7, 9, 24) zum Setzen des Extrabits des Datenworts, das in dem Speicher gespeichert ist, auf die Adresse, die in dem Zeigerregister gespeichert ist, so daß das Extrabit das eingerichtete Kanalwort angibt, das dem Datenwort entspricht.

8. Verfahren zum Binärcodieren von Daten, umfassend die Schritte:
Umwandeln einer Folge von Binärdatenwörtern, die jeweils N Datenbits enthalten, wobei N eine ganze



Zahl größer 1 ist, in eine Folge jeweils entsprechender binärer Kanalwörter, die jeweils M Datenbits enthalten, wobei M eine ganze Zahl größer N ist, wobei jedes Kanalwort wenigstens ein Bindebit an einem Ende des Kanalworts aufweist, dessen Wert so gesetzt werden kann, daß sichergestellt ist, daß die Folge von Kanalwörtern zu gegebenen Auflängenregeln paßt und eine minimale Digitalsummenschwankung aufweist;

Ausgeben der Folge von Kanalwörtern;

Modulieren der Folge von Kanalwörtern in NRZI-codierte Kanalcodes,

dadurch gekennzeichnet, daß:

eine vorbestimmte Anzahl der Kanalwörter wenigstens ein selektives Bit (b4) zusätzlich zu und getrennt von dem wenigstens einen Bindebit (b0) aufweist, welches selektive Bit entweder "1" oder "0" sein kann;

wobei das Verfahren umfaßt:

Einstellen des Wertes des wenigstens einen selektiven Bits, wenn es in einem Kanalwort vorhanden ist, um sicherzustellen, daß die Folge von Kanalwörtern zu gegebenen Auflängenregeln paßt;

Einrichten für jedes Kanalwort, ob der Wert von dem wenigstens einen Bindebit und/oder des wenigstens einen selektiven Bits, sofern es darin vorhanden ist, geändert werden kann, ohne mit den gegebenen Auflängenregeln zu kollidieren;

Zwischenspeichern eines Signals (2c), das ein Kanalwort bezeichnet, in dem der Wert eines Bits so geändert werden kann;

wobei die Ausgabe eines ersten Kanalworts, bei dem der Wert eines Bits so geändert sein kann, um eine Verzögerungsperiode verzögert wird, wobei diese Periode die Zeit bis zum Auftreten des nächsten Kanalworts ist, bei dem der Wert eines Bits so geändert sein kann, oder bis zum Auftreten einer vorbestimmten Anzahl von nachfolgenden zusammenhängenden Kanalwörtern ist, in denen der Wert keines Bits so geändert sein kann; und

wobei das wenigstens eine Bindebit und/oder das wenigstens eine selektive Bit in dem ersten Kanalwort am Ende der Verzögerungsperiode vor der Ausgabe des ersten Kanalworts so eingestellt wird, daß es den Wert hat, der zu einem niedrigeren Absolutwert der Digitalsummenschwankung (DSV) der Kanalcodes am Ende der Verzögerungsperiode oder zu einem niedrigeren maximalen Absolutwert der DSV der Kanalcodes während der Verzögerungsperiode führt.

9. Verfahren nach Anspruch 8, bei dem jedes der vorbestimmten Anzahl Kanalwörter ein einziges selektives Bit hat.

10. Verfahren nach Anspruch 8 oder 9, bei dem jedes der Kanalwörter ein einziges Bindebit hat.

11. Verfahren nach Anspruch 8 oder 9, bei der die Umwandlung der Datenwörter in die Kanalwörter gemäß den folgenden Regeln ausgeführt wird:

(i) zwei oder mehr "0"-Bits sind zwischen zwei "1"-Bits in einem Kanalwort vorhanden, wenn das Kanalwort zwei oder mehr "1"-Bits enthält;

(ii) das höchstwertige Bit oder das niedrigstwertige Bit eines jeden Kanalworts wird anfänglich zu "0" als ein Bindebit gemacht, und wenn beide Bits benachbart dem Bindebit gleich "1" sind, werden beide benachbarten Bits zu "0" gemacht und das Bindebit wird zu "1" gemacht, und

(iii) das Bindebit wird zu "0" oder "1" gemacht, so daß der Absolutwert der DSV abnimmt, wenn ein dem Bindebit um drei Bits vorausgehendes Bit "1" ist und dem Bindebit zwei aufeinanderfolgende "0"-Bits folgen oder wenn zwei dem Bindebit unmittelbar vorausgehende Bits beide "0" sind und das drei Bits hinter dem Bindebit liegende Bit gleich "1" ist.

Revendications

1. Dispositif pour coder des données binaires, comprenant:

un moyen convertisseur agencé pour convertir une suite de mots de données binaires contenant chacun N bits de données, où N est un entier supérieur à 1, en une suite de mots de canal binaires correspondants respectifs contenant chacun M bits de données, où M est un entier supérieur à N, chaque mot de canal comportant au moins un bit de fusion à une limite du mot de canal dont la valeur peut être établie pour garantir que la suite de mots de canal est en accord avec des règles de longueur de passage données et comporte une variation de somme numérique minimale;

un moyen de sortie agencé pour sortir ladite suite de mots de canal;

un moyen modulateur en codage NRZI (18) agencé pour moduler ladite suite de mots de canal en



codes de canal en codage NRZI,

caractérisé en ce que :

un nombre prédéterminé desdits mots de canal comportent au moins un bit sélectif (b4), en plus et séparé dudit bit de fusion (b0) au moins, ce bit sélectif pouvant être à '1' ou à '0'; et

le dispositif comprend:

un moyen agencé pour établir la valeur dudit bit sélectif au moins s'il est présent dans un mot de canal afin de garantir que la suite de mots de canal est en accord avec des règles de longueur de passage données;

un moyen (2) pour établir, pour chaque mot de canal, si la valeur du bit de fusion au moins et/ou du bit sélectif au moins s'il y est présent peut être changée sans contrevenir aux règles de longueur de passage données;

un moyen (11) pour mémoriser temporairement un signal (2c) indiquant un mot de canal dans lequel la valeur d'un bit peut être ainsi changée;

un moyen pour retarder la sortie d'un premier mot de canal dans lequel la valeur d'un bit peut être ainsi changée pendant une période de retard, cette période étant le temps jusqu'à l'apparition du mot de canal suivant dans lequel la valeur d'un bit peut être ainsi changée ou le temps jusqu'à l'apparition d'un nombre prédéterminé de mots de canal consécutifs suivants dans lesquels la valeur d'aucun bit ne peut être ainsi changée; et

un moyen (6,9) agencé pour établir le bit de fusion au moins et/ou le bit sélectif au moins dans le premier mot de canal à la fin de la période de retard, avant la sortie du premier mot de canal, pour avoir la valeur qui donne une valeur absolue inférieure de la variation de somme numérique (DSV) des codes de canal à la fin de la période de retard, ou une valeur absolue maximale inférieure de la variation DSV des codes de canal pendant la période de retard.

2. Dispositif selon la revendication 1, dans lequel chacun dudit nombre prédéterminé de mots de canal comporte un seul bit sélectif.

3. Dispositif selon l'une quelconque des revendications 1 et 2, dans lequel chacun desdits mots de canal comporte un seul bit de fusion.

4. Dispositif selon la revendication 1, dans lequel ledit moyen convertisseur (17) comprend: un moyen générateur de données pseudo-aléatoires (70) pour générer des données pseudo-aléatoires qui circulent en synchronisation avec les mots de données d'entrée; et un moyen brouilleur (71) pour brouiller lesdits mots de données d'entrée avec lesdites données pseudo-aléatoires, et dans lequel ledit moyen convertisseur (17) convertit les données de sortie dudit moyen brouilleur en lesdits mots de canal.

5. Dispositif selon l'une quelconque des revendications 1 et 2, dans lequel ledit moyen convertisseur (17) exécute une conversion suivant les règles suivantes :

(i) deux bits à '0' ou plus sont présents entre deux bits à '1' dans un mot de canal si ledit mot de canal contient deux bits à '1' ou plus;

(ii) le bit de poids le plus fort ou le bit de poids le plus faible de chaque mot de canal est mis initialement à '0' en tant que bit de fusion, et, quand les deux bits voisins dudit bit de fusion sont tous les deux à '1', lesdits bits voisins sont mis à '0' et ledit bit de fusion est mis à '1'; et

(iii) ledit bit de fusion est mis à '0' ou à '1', de telle sorte que la valeur absolue de la variation DSV est réduite quand un bit précédent ledit bit de fusion de trois bits est à '1' et ledit bit de fusion est suivi par deux bits consécutifs à '0' ou quand deux bits consécutifs juste avant ledit bit de fusion sont tous les deux à '0' et le bit trois bits après ledit bit de fusion est à '1'.

6. Dispositif selon la revendication 1, dans lequel ledit moyen convertisseur (17) comprend: un convertisseur (1) pour convertir lesdits mots de données en mots de canal initiaux; une mémoire de mémorisation de mots de canal (8) pour mémoriser lesdits mots de canal initiaux; un registre de pointeur (11) pour mémoriser une adresse où est mémorisé dans ladite mémoire un mot de canal initial dans lequel il a été établi qu'un bit peut être ainsi changé; et un moyen (6,7,9,10,13) pour écrire un dernier mot de canal à ladite adresse mémorisée dans ledit registre de pointeur à la fin de ladite période de retard.

7. Dispositif selon la revendication 1, dans lequel ledit moyen convertisseur (17) comprend: une mémoire de mémorisation de mots de données (20) pour mémoriser lesdits mots de données et leurs bits



- supplémentaires; un moyen de lecture (25,26) pour convertir lesdits mots mémorisés dans ladite mémoire en lesdits mots de canal par rapport auxdits bits supplémentaires; un registre de pointeur (11) pour mémoriser une adresse ou sont mémorisés dans ladite mémoire un mot de données, le mot de canal pour lequel il y a un bit qui peut être ainsi changé, et son bit supplémentaire; et un moyen (7,9,24) pour mettre ledit bit supplémentaire dudit mot de données mémorisé dans ladite mémoire à ladite adresse mémorisée dans ledit registre de pointeur, de telle sorte que ledit bit supplémentaire indique le mot de canal établi correspondant audit mot de données.
- 5
8. Méthode pour coder des données binaires, comprenant les étapes qui consistent à:
- 10 convertir une suite de mots de données binaires contenant chacun N bits de données, où N est un entier supérieur à 1, en une suite de mots de canal binaires correspondants respectifs contenant chacun M bits de données, où M est un entier supérieur à N, chaque mot de canal comportant au moins un bit de fusion à une limite du mot de canal dont la valeur peut être établie pour garantir que la suite de mots de canal est en accord avec des règles de longueur de passage données et comporte
- 15 une variation de somme numérique minimale;
- sortir ladite suite de mots de canal;
- moduler ladite suite de mots de canal en codes de canal en codage NRZI,
- caractérisé en ce que :
- un nombre prédéterminé desdits mots de canal comportent au moins un bit sélectif (b4), en plus et
- 20 séparé dudit bit de fusion (b0) au moins, ce bit sélectif pouvant être à '1' ou à '0';
- ladite méthode comprenant les étapes qui consistent à:
- établir la valeur dudit bit sélectif au moins s'il est présent dans un mot de canal afin de garantir que la suite de mots de canal est en accord avec des règles de longueur de passage données;
- 25 établir, pour chaque mot de canal, si la valeur du bit de fusion au moins et/ou du bit sélectif au moins s'il y est présent peut être changée sans contrevenir aux règles de longueur de passage données;
- mémoriser temporairement un signal (2c) indiquant un mot de canal dans lequel la valeur d'un bit peut être ainsi changée;
- 30 dans laquelle la sortie d'un premier mot de canal dans lequel la valeur d'un bit peut être ainsi changée est retardée pendant une période de retard, cette période étant le temps jusqu'à l'apparition du mot de canal suivant dans lequel la valeur d'un bit peut être ainsi changée ou le temps jusqu'à l'apparition d'un nombre prédéterminé de mots de canal consécutifs suivants dans lesquels la valeur d'aucun bit ne peut être ainsi changée; et
- 35 dans laquelle le bit de fusion au moins et/ou le bit sélectif au moins dans le premier mot de canal est établi à la fin de la période de retard, avant la sortie du premier mot de canal, pour avoir la valeur qui donne une valeur absolue inférieure de la variation de somme numérique (DSV) des codes de canal à la fin de la période de retard, ou une valeur absolue maximale inférieure de la variation DSV des codes de canal pendant la période de retard.
- 40 9. Méthode selon la revendication 8, dans laquelle chacun dudit nombre prédéterminé de mots de canal comporte un seul bit sélectif.
10. Méthode selon l'une quelconque des revendications 8 et 9, dans laquelle chacun desdits mots de canal comporte un seul bit de fusion.
- 45 11. Méthode selon l'une quelconque des revendications 8 et 9, dans laquelle la conversion desdits mots de données en lesdits mots de canal est exécutée suivant les règles suivantes:
- (i) deux bits à '0' ou plus sont présents entre deux bits à '1' dans un mot de canal si ledit mot de canal contient deux bits à '1' ou plus;
- 50 (ii) le bit de poids le plus fort ou le bit de poids le plus faible de chaque mot de canal est mis initialement à '0' en tant que bit de fusion, et, quand les deux bits voisins dudit bit de fusion sont tous les deux à '1', lesdits bits voisins sont mis à '0' et ledit bit de fusion est mis à '1'; et
- (iii) ledit bit de fusion est mis à '0' ou à '1', de telle sorte que la valeur absolue de la variation DSV est réduite quand un bit précédant ledit bit de fusion de trois bits est à '1' et ledit bit de fusion est
- 55 suivi par deux bits consécutifs à '0' ou quand deux bits consécutifs juste avant ledit bit de fusion sont tous les deux à '0' et le bit trois bits après ledit bit de fusion est à '1'.