Abstract

METHOD FOR FORMING A T-GATE FOR BETTER SALICIDATION

A method for a T-gate and salicide process that allows narrow bottom gate widths below 0.25 μm and wide top gate widths to allow silicide gate contacts on the top of the T -gate. A dummy gate composed of an insulating material is formed over the substrate. Then we form LDD regions adjacent to the dummy gate preferably by ion implanting f (I/I) impurity ions into the substrate using the dummy gate as a mask. A pad oxide layer and dielectric layer are formed over the substrate surface. The dielectric layer over the dummy gate is removed preferably by a CMP process. We then remove the dummy gate to form a gate opening exposing the substrate surface. A gate dielectric layer is formed over the substrate surface in the gate opening. We form a polysilicon layer over the dielectric layer and the substrate surface in the gate opening. The polysilicon layer is patterned to form a T-gate. The dielectric layer is removed. We forming source/drain (S/D) regions adjacent to the T-gate by an Ion implant process. A silicide layer is formed over the T-gate and the substrate to form silicide contacts to the S/D regions and gate contacts to the T-gate. Then we form a dielectric layer (ILD) over the T-gate and substrate. We form contact opening through the dielectric layer to expose the S/D regions and T-gate. We form contacts to the S/D regions and to the T-gate.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)