CLAIMS

1. An eDRAM memory element comprising

a first storage node having a bottom part;

a bitline node for accessing the value stored in the storage node, wherein the bitline node is shaped so as to extend beyond the bottom part of the first storage node; and

a select transistor controlling access from the bitline node to the storage node;

wherein the select transistor has a front gate with a bottom part and a back gate, and the bitline node is shaped so as to extend beyond the bottom part of the front gate.

2. The eDRAM memory element according to claim 1 wherein the back gate is configured so as to be polarized for increasing the threshold voltage of the select transistor.

3. The eDRAM memory element according to claim 1 wherein the back gate is configured so as to be polarized for increasing the threshold voltage of the select transistor during retention operation of the eDRAM memory element.

4. The eDRAM memory element according to claim 3 wherein the back gate is configured so as to be polarized for decreasing the threshold voltage of the select transistor during reading and/or writing operation of the eDRAM memory element.

5. An eDRAM group comprising

at least a first eDRAM memory element and a second eDRAM memory element, each of the first eDRAM memory element and the second eDRAM memory element having a first storage node, a bitline node for accessing the value stored in the corresponding first storage node, and a select transistor controlling access from the bitline node to the storage node, wherein each select transistor has a front gate and a back gate;

wherein the back gate of the first eDRAM memory element is disconnected from the back gate of the second eDRAM memory element; and

the bitline node of the first eDRAM memory element is the same as the bitline node of the second eDRAM memory element.

6. The eDRAM group of claim 5 wherein the back gate of each of the first eDRAM memory element and the second eDRAM memory element is configured so as to be polarized for increasing the threshold voltage of the select transistor or each of the eDRAM memory elements during a retention operation of each of the eDRAM memory elements.

7. The eDRAM group of claim 6 wherein the back gate of each of the first eDRAM memory element and the second eDRAM memory element is configured so as to be polarized for decreasing the threshold voltage of the select transistor or each of the eDRAM memory elements during a retention operation of each of the eDRAM memory elements.

8. The eDRAM group of claim 5 wherein the back gate of each of the first eDRAM memory element and the second eDRAM memory element is configured so

as to be polarized for decreasing the threshold voltage of the select transistor or each of the eDRAM memory elements during a retention operation of each of the eDRAM memory elements.

9. The eDRAM memory element of claim 1 wherein the select transistor has a bottom part, and the bitline node extend beyond the bottom part of the select transistor.

10. The eDRAM memory element of claim 1 further comprising a first vertical connection directly connected to the first front gate, a second vertical connection directly connected to the second front gate, and a horizontal connection directly connected to the bitline node.

Claims

1. An eDRAM memory element comprising a first storage node (1120, 1220), a bitline node (1040) for accessing the value stored in the storage node, and a select transistor (1130, 1230), controlling access from the bitline node to the storage node, wherein the select transistor has a front gate (1132, 1232) and a back gate (3500, 4510, 4511, 9500, 10510-10515).

2. The eDRAM memory element according to claim 1 wherein the back gate (3500, 9500) is configured so as to be polarized for increasing the threshold voltage of the select transistor.

3. The eDRAM memory element according to claim 1 wherein the back gate (4510, 4511, 10510-10515) is configured so as to be polarized for increasing the threshold voltage of the select transistor during retention operation of the eDRAM memory element.

4. The eDRAM memory element according to claim 3 wherein the back gate (4510, 4511, 10510-10515) is configured so as to be polarized for decreasing the threshold voltage of the select transistor during reading and/or writing operation of the eDRAM memory element.

5. An eDRAM group comprising at least a first (1100) and a second (1200) eDRAM memory element, both in accordance with claim 1 or 2, wherein the back gate (3500) of the first eDRAM memory element is connected to the back gate (3500) of the second eDRAM memory element.

6. The eDRAM group of claim 5 wherein the bitline node of the first eDRAM memory element is the same as the bitline node of the second eDRAM memory element.

7. An eDRAM group comprising at least a first (4100) and a second (4200) eDRAM memory element, both in accordance with claim 1, 3 or 4, wherein the back gate (4510) of the first eDRAM memory element is disconnected from the back gate (4511) of the second eDRAM memory element.

8. The eDRAM group of claim 7 wherein the bitline node of the first eDRAM memory element and the bitline node of the second eDRAM memory element are separated by an insulation element (5004) and are electrically connected to each other via a connection (4610).