

THIN SILICON SOLAR CELL AND METHOD OF MANUFACTURE

Inventors: Seung Bum Rim, Michael Morse, Taeseok Kim, and
Michael J. Cudzinovic

TECHNICAL FIELD

[0001] Embodiments of the subject matter described herein relate generally to solar cell manufacture. More particularly, embodiments of the subject matter relate to thin silicon solar cells and techniques for manufacture.

BACKGROUND

[0002] Solar cells are well known devices for converting solar radiation to electrical energy. They may be fabricated on a semiconductor wafer using semiconductor processing technology. A solar cell includes P-type and N-type diffusion regions. Solar radiation impinging on the solar cell creates electrons and holes that migrate to the diffusion regions, thereby creating voltage differentials between the diffusion regions. In a back contact, back junction (BCBJ) solar cell, the P-type and N-type diffusion regions and the metal contacts coupled to them are on the backside of the solar cell. The metal contacts allow an external electrical circuit to be coupled to and be powered by the solar cell.

[0003] To compete with other energy sources available on the market, solar cells not only have to be efficient but also fabricated at relatively low cost and high yield. Although solar cells can be fabricated using silicon processing steps, operations performed on a silicon wafer necessarily occur after the wafer has been created. Creating silicon wafers for solar cells typically can include, for example, forming a silicon material, shaping the silicon material into an ingot, and wafering the ingot to form silicon wafers. Embodiments of the present invention pertain to novel solar cell fabrication processes and structures that reduce the cost of solar cell fabrication.

BRIEF SUMMARY

[0004] A method of fabricating a solar cell is disclosed. The method includes the steps of forming a sacrificial layer on a silicon substrate, forming a doped silicon layer

atop the sacrificial substrate, forming a silicon film atop the doped silicon layer, forming an oxide layer on the silicon film; forming alternating P-type and N-type doped regions on the oxide layer; contacting each of the P-type and N-type doped regions with a metal contact; and removing the sacrificial layer and the silicon substrate.

[0005] Another method of fabricating a solar cell is disclosed. The method comprises the steps of forming a sacrificial layer on a top surface of a silicon substrate, processing the exposed surface of the sacrificial layer to form a textured surface, forming a heavily doped silicon layer atop the textured surface of the sacrificial layer, forming a lesser doped silicon layer atop the heavily doped silicon layer, epitaxially growing a silicon film atop the lesser doped silicon layer, forming alternating P-type and N-type doped regions over the silicon film; contacting each of the P-type and N-type doped regions with a metal contact; bonding a back side of the solar cell to a carrier, separating the heavily doped silicon layer from the silicon substrate by removing the sacrificial layer, debonding the silicon film from the carrier, and forming an anti-reflective coating over the heavily doped silicon layer.

[0006] Yet another method of fabricating a solar cell is disclosed. The method comprises forming a sacrificial layer on a silicon substrate, forming a doped silicon layer atop the sacrificial substrate, forming a silicon film atop the doped silicon layer, forming a plurality of interdigitated contacts on the silicon film, and separating the doped silicon layer from the silicon substrate.

[0007] This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the detailed description. This summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used as an aid in determining the scope of the claimed subject matter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] A more complete understanding of the subject matter may be derived by referring to the detailed description and claims when considered in conjunction with the following figures, wherein like reference numbers refer to similar elements throughout the figures.

[0009] FIG. 1 is a cross-sectional view of a thin silicon solar cell in accordance with an embodiment of the invention;

[0010] FIGS. 2-11 are cross-sectional representations of a solar cell being fabricated in accordance with an embodiment of the invention;

[0011] FIGS. 12-13 are cross-sectional representations of fabrication steps in accordance with another embodiment of the invention.

DETAILED DESCRIPTION

[0012] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word “exemplary” means “serving as an example, instance, or illustration.” Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0013] One technique for reducing the cost of fabricating a solar cell can be to omit the steps of the process necessary to create the silicon wafer which is processed during traditional photovoltaic solar cell manufacture. To omit the wafer creation steps, the silicon substrate which forms the bulk of the solar cell can be epitaxially grown, together with the other constituent parts of a photovoltaic solar cell, on a sacrificial layer of material. The sacrificial layer can then be removed, detaching the completed, grown solar cell from the formative platform.

[0014] The various tasks performed in connection with the fabrication techniques shown in FIGS. 2-13 may include any number of additional or alternative tasks, the fabrication shown in FIGS. 2-13 need not be performed in the illustrated order, and the fabrication process may be incorporated into a more comprehensive procedure or process having additional functionality not described in detail herein.

[0015] FIG. 1 illustrates a solar cell 1 formed with a thin silicon substrate 10. The solar cell 1 comprises the thin silicon substrate 10, a lightly doped region 20, a heavily doped region 30, and anti-reflective coating (ARC) 40, and a contact structure 50. The solar cell has a first, sunny side 4, which faces the sun during normal operation, and a second, back side 6, which faces away. It should be appreciated that the sunny side-facing surfaces of the thin silicon substrate 10, the lightly and heavily doped regions 20, 30, and the ARC 40 have a random, textured surface which improves the performance of the solar cell 1 in capturing light received on the sunny side 4. These textured surfaces can have truly random shapes, such as those caused by wet etching a material with

surface defects, or a repeating geometric shape, such as a triangular or rectangular pyramidal shape.

[0016] The contact structure 50 can include alternating N and P doped regions 54, 56 formed atop a thin oxide layer 52. The N and P doped regions 54, 56 can be covered by an insulating layer 58, such as an oxide or polyimide, or other insulating material. A contact 60 can be formed through a hole in the insulating layer 58 to provide electrical contact with each of the doped regions 54, 56. The contact 60 can be a single metal, such as copper or aluminum, or a stack of different metals, including tungsten, as desired for the embodiment, and explained in further detail below. The solar cell 1 can be formed, as shown in the embodiment illustrated in FIG. 1, as a back contact, back junction (BCBJ) solar cell. The solar cell 1 can include any of several different contact structures 50 as desired for the embodiment, including different arrangements of the doped regions 54, 56 and the passivating oxides. The formation of the thin silicon substrate 10 can be accomplished by growing the layers toward the sunny side 4 of the solar cell 1 upwards from a sacrificial layer atop a substrate. In certain embodiments, the ARC layer 40 can be omitted during fabrication, and applied later.

[0017] FIGS. 2-11 illustrate a solar cell, such as that of the embodiment of FIG. 1, in sequential steps of fabrication of a thin silicon solar cell using an epitaxial growth technique.

[0018] FIG. 2 illustrates a silicon substrate 100. The silicon substrate 100 can be composed of pure silicon, or can be doped or compound silicon. The silicon substrate 100 has an upper surface 102. The silicon substrate 100 can be a reusable part of the fabrication process. In certain embodiments, as described in greater detail below with respect to FIGS. 12 and 13, the silicon substrate 100 can include a plurality of thin layers.

[0019] As shown in FIG. 3, a sacrificial layer 110 can be formed on the upper surface 102 of the silicon substrate 100. The sacrificial layer 110 can be composed of porous silicon, such as formed in a HF bath with bias. Alternatively, the sacrificial layer 110 can be silicon with, for example, germanium doping and/or a carbon doping, either of which can be formed by epitaxial deposition or a chemical vapor deposition (CVD) process. As used throughout, a CVD process refers to any variant of CVD, such as atmospheric pressure CVD (APCVD), plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), and so on. The desired CVD process for any particular fabrication step

can be selected and used by one of ordinary skill in the art. Other dopants besides germanium and carbon can also be used. The sacrificial layer 110 can be thin, on the order of approximately 700 micrometers, although it can be slightly or significantly larger or smaller, as desired for a particular embodiment to perform the functions described herein. For example, in certain embodiments, the sacrificial layer can be as thin as 10 micrometers. Smaller thicknesses can also be used.

[0020] FIG. 4 illustrates the sacrificial layer 110 after a random texturing step, such as with a wet or dry etch process, including buffered oxide etching (BOE) to create an upper textured surface 114. One etchant that can be used is potassium hydroxide, KOH, although others can also be used in different embodiments. The textured surface 114 of the sacrificial layer 110 thus does not have a planar shape. In certain embodiments, the texture does not include exposure of the underlying silicon substrate 100, although in some embodiments, the silicon substrate 100 can be exposed through the sacrificial layer 110 if desired. The textured surface 114 of the sacrificial layer 110 can have a regular, repeating pattern, such as triangular or rectangular pyramids, or can have a randomly determined pattern. In either case, the sacrificial layer 110 can maintain the shape of the textured surface 114 during subsequent processing.

[0021] As shown in FIG. 5, a doped silicon layer 120 can be formed atop the textured surface 114. The doped silicon layer 120 can be deposited using any desired CVD process. The doped silicon layer can be N+ doped, and have a thickness of between 0.01 and 5 micrometers. In certain embodiments, the doped silicon layer 120 can be doped with germanium. In some embodiments, the dopant concentration can be approximately 1×10^{17} atoms per cubic centimeter, while less or greater concentrations, up to 1×10^{20} atoms per cubic centimeter or greater can also be used.

[0022] In certain embodiments, another doped layer of silicon, an N+ layer 124 can be formed on the doped silicon layer 120. FIG. 6 illustrates the formation of the N+ layer 124. Not all embodiments will include the N+ layer 124, but it is illustrated throughout. The N+ layer 124 can be deposited, such as through a CVD technique or grown using an epitaxial growth technique. The N+ layer 124 can be composed of a silicon-germanium composition, or a silicon-carbon material.

[0023] Relative to the thicker N+ layer 124, the doped silicon layer 120 can be heavily doped, often referred to as an N++ doped layer. In some embodiments, the N+ layer 120 can be referred to as a lightly doped layer, expressed relative to the higher-

doped silicon layer 120. In certain embodiments, the N+ layer 124 can be relatively porous. In some embodiments, undoped silicon can be deposited atop the doped silicon layer 120. A subsequent thermal step can be used to drive dopants from the doped silicon layer 120 into the N+ layer 124, resulting in a relatively light doping of the N+ layer 124. The N+ layer 124 can be, when present, between 0.05 and 1 micrometers thick.

[0024] FIG. 7 illustrates the growth of a silicon film 130 atop the N+ layer 124 or, atop the doped silicon layer 120 when the N+ layer is omitted. The silicon film 130 can be relatively thick as compared to the accompanying layers in the overall structure of the finished solar cell. It can also be relatively thin as compared to the substrate 100, or a traditional solar cell wafer. A silicon film grown by an epitaxial deposition process can also be referred to as a thin silicon film, a thin silicon substrate, the epitaxially-grown substrate, or, more generally, as a grown silicon layer. The silicon film 130 can be formed by a epitaxial growth process, seeding and propagating a polysilicon crystal structure on the exposed surface of the N+ layer 124. The silicon film 130 can be slightly N+ doped, such as a silicon-germanium substrate, or a silicon-carbon substrate. The silicon film 130 can, in some embodiments be a pure silicon substrate. In certain embodiments, the silicon film 130 can be porous silicon. In general, the exact composition of the silicon film 130 can be silicon or some doped silicon material or a compound of silicon sufficient to operate as a photovoltaic solar cell substrate in cooperation with the rest of the elements of the solar cell fabricated.

[0025] In some embodiments, a thermal heating step can follow the epitaxial growth of any layer or substance described herein, including growth of the silicon film 130 to sinter it. The silicon film 130 can be formed with a CVD process step. The silicon film 130 can be between 20 and 150 micrometers thick, and in some embodiments can be 50 micrometers thick. In some embodiments, the silicon film 130 is formed by a process which reduces the surface texture on its rear side. Thus, while the doped silicon layer 120 and N+ layer 124 can be relatively conformal, the thickness of the silicon film 130 can cause planarization, resulting in a relatively flat rear surface, the exposed surface.

[0026] FIG. 8 illustrates the formation of a contact structure 140 on said exposed surface of the silicon film 130. The exact contact structure 140 can vary between embodiments. For example, in certain embodiments, the contact structure can include interdigitated doped polysilicon regions. The illustrated embodiment shows alternating

N and P doped polysilicon regions, 144 and 146, respectively. Additionally, a thin oxide layer 142 can be present between the silicon film 130 and the doped polysilicon regions 144, 146, as described in U.S. Patents Nos. 7,468,485 and 7,633,006 to Swanson, the entirety of which are incorporated by reference herein. The thin oxide layer 142 can function as a tunnel oxide, inhibiting recombination during carrier transport to the doped polysilicon regions 144, 146. The doped polysilicon regions 144, 146 can be formed using print, mask, and etch techniques, such as, without limitation, those described in U.S. Patents Nos. 6,998,288 and 7,135,350 to Smith et al., and 7,820,475 to De Ceuster et al., the entirety of which are incorporated by reference herein.

[0027] In some embodiments, the doped polysilicon regions 144, 146 can be formed using an inkjet printing process. In such a process, an undoped polysilicon layer can be formed atop the thin oxide layer 142. An inkjet dopant deposition process can be used to precisely place the appropriate N and P dopant sources atop their respective polysilicon regions. A thermal drive step can follow, doping the N and P polysilicon regions 144, 146. A mask and etch step can then be used to remove the dopant source, as well as form the trenches between the polysilicon regions 144, 146. A detailed explanation of such a process of forming the contact structure 140 can be found in US Patent No. 7,812,250 to Smith, the entirety of which is incorporated by reference herein.

[0028] An insulating layer 148 can be formed over the doped polysilicon regions 144, including in the trenches therebetween. In addition to a single illustrated insulating layer 148, other insulating layers can also be formed in different embodiments. For example, in certain embodiments, silicon nitride or another back-side ARC can be formed as part of the process of forming the contact structure 140. Other passivating or insulating layers can also be formed during the formation of the contact structure 140. One or more contact holes or vias can be opened in the insulating layer 148 to permit formation of a contact plug 150 which electrically contacts the doped polysilicon regions 144, 146. In certain embodiments, the contact holes or vias can be opened with a mask and etch process, while in others a laser process can be used, as is known in the art. Similarly, although referred to as a contact plug 150, the contact plug 150 can refer to several stacked materials, such as those described in U.S. Patent No. 7,388,147 to Mulligan et al., the entirety of which is incorporated by reference herein.

[0029] In some embodiments, the contact structure 140 can be of an entirely different type, such as that described in U.S. Patent Application, serial number 11/492,282, to De

Ceuster et al., published as U.S. Patent Publication No. 2008/0017243, the entirety of which is incorporated by reference herein. Regardless of the specific components, elements, or features of the contact structure 140, a back-contact, back-junction architecture can be used, wherein the silicon film 130 serves as a silicon substrate for any of the structures described in any reference. In practicing such techniques, it will be observed that the front structure has already been formed, with a randomly-textured surface and an N+ doped region on the front or sunny side of the solar cell, the boundary of which is the doped silicon layer 120 currently bonded with the sacrificial layer 112.

[0030] In certain embodiments, the thermal steps required to produce the contact structure 140 can be used to complete dopant drive-in from the doped silicon layer 120 into the N+ layer 124 or silicon film 130. In some embodiments, dopants from the doped silicon layer 120 be driven into the silicon film 130 through the N+ layer 124 or, in other embodiments, they can be driven directly into the silicon film 130 because the N+ layer 124 has been omitted. Thus, one of skill in the art will appreciate that it may not be necessary to fully drive and activate the dopants in the doped silicon layer 120, N+ layer 124, or silicon film 130 during their respective formation steps if sufficient thermal processes will occur during formation of the contact structure 140.

[0031] Thus, FIG. 8 illustrates a fully-formed contact structure 140. Although one embodiment of such a structure is shown, others can be used without deviating from the inventive techniques described herein. FIG. 9 illustrates a carrier element 160 which can be bonded to the exposed surface of the rear side of the silicon film 130. For example, the carrier element 160 can be bonded to the insulating layer 148 or the contact plugs 150, or both. The carrier element 160 can be any device or structure which has sufficient rigidity and, in some embodiments, flatness, to support the solar cell during the subsequent separation step. Thus, in some embodiments, the carrier element 160 can be a plastic surface, or a metal one, or so on. In some embodiments, the carrier element 160 can be bonded to multiple cells for separate all of them. The carrier element 160 can be bonded using any dissolvable or reversible bonding agent or adhesive. In certain embodiments, a permanent bond can be formed, including those which are not permanent, but have no corresponding debonding agents.

[0032] FIG. 10 illustrates the separation step wherein the sacrificial layer 112 is partially or fully destroyed, releasing the thin silicon solar cell 190 from the silicon substrate 100. Such a separation can be accomplished using, for example, a selective

etch process, including wet etch processes. In certain embodiments, the sacrificial layer 112 is retained by the silicon substrate 100 for reuse. In such embodiments, the surface containing the sacrificial layer 112 can be washed or cleaned prior to re-use. In other embodiments, the sacrificial layer 112 is dissolved entirely, requiring that, if the silicon substrate is to be re-used, a new sacrificial layer 112 be formed. In certain embodiments, portions of the sacrificial layer 112 may not be removed during the separation process, which can be subsequently destroyed. Thus, the sacrificial layer 112 is not re-used in future fabrication steps, but it need not be entirely removed during the separation process. In some embodiments, the selective etchant use does not attack the components of the thin silicon solar cell 190.

[0033] The surface of the doped silicon layer 120 is thus exposed. This surface can be washed and cleaned following the separation from the sacrificial layer 112. The doped silicon layer 120 now forms the uppermost layer on the sunny side of the thin silicon solar cell 190. FIG. 11 illustrates that an ARC layer 170 may be formed over the doped silicon layer 120, enhancing the performance of the thin silicon solar cell 190. In certain embodiments, a backside ARC, or BARC, can be formed as part of the process of forming the contact structure 140.

[0034] In certain embodiments, one or more fabrication steps can be omitted. For example, where the doped silicon layer 120 and the N+ layer 124 are both omitted, the front surface of the silicon film 130 is formed directly on the sacrificial layer 112. In such an embodiment, front-side passivation of the thin silicon solar cell 190 can be performed prior to or together with an ARC step. In certain embodiments, doping of the front side, or exposed side of the silicon film 130 can be performed after separating it from the sacrificial layer 112.

[0035] As shown in FIG. 11, the carrier element 160 can be released from the thin silicon solar cell 190 through any desired debonding process. Such a debonding process can include a solvent or etchant which attacks the adhesive or bonding agent coupling the thin silicon solar cell 190 to the carrier element 160. In certain embodiments, the rear side of the thin silicon solar cell 190 can be cleaned to remove remnants of the bonding process. The thin silicon solar cell 190 is now ready for further processing, such as stringing, interconnection, incorporating in a solar module, and so on. In some embodiments, the front ARC and BARC steps can be performed simultaneously at this

point in the fabrication process. ARC or BARC materials can include nitrides, such as silicon nitride, deposited using a remote plasma deposition technique.

[0036] As can be seen, the thin silicon solar cell 190 has been fabricated without relying on a traditionally-created solar wafer, eliminating the potentially expensive additional steps of ingot creation and wafering.

[0037] Another advantageous feature of the present fabrication technique that can be appreciated is the formation of the textured front surface of the silicon film 130, specifically the textured doped silicon layer 120 and/or N+ layer 124. During some solar cell fabrication processes, texturizing the front surface of the cell includes an etch step for both front and back surfaces. In some embodiments, the contact structure formation steps must accommodate a destructive etch to the rear, contact surface. Thus, some techniques form protective structures for use over sensitive features of the rear surface during the texturizing etch. Having pre-textured the front surface, the now-exposed doped silicon layer 120, the contact structure 140 can be created without accommodating the destructive texturizing etch step. Removing this consideration can reduce the cost of forming the contact structure 140. In those embodiments where the destructive texturizing step is required for rear-side contact formation, it is possible to form a flat sacrificial layer, doped silicon layer 120, N+ layer 124, and silicon film 130. Only after separating from the sacrificial layer can the doped silicon layer 120 be texturized, including a texturing of the rear side, to prepare for BARC processing.

[0038] FIGS. 12 and 13 illustrate steps in an alternative process embodiment for the initial steps of fabrication for the thin silicon solar cell. As shown in FIG. 12, the silicon substrate 200 can itself have a textured surface. This textured surface can, in some embodiments, be doped to aid the use of it as a sacrificial layer. A doped silicon layer 212 can then be conformally formed atop the silicon substrate 200, imparting the textured shape to the doped silicon layer 212. In this way, the upper surface of the silicon substrate 200 can function as the sacrificial layer. During a separation step equivalent to that shown in FIGS. 9 and 10, the upper surface of the silicon substrate 200 can be attacked, releasing the thin silicon solar cell. The silicon substrate 200 can retain its textured shape, permitting re-use, after cleaning, by the formation of a new doped silicon layer 212 atop it.

[0039] As was previously mentioned, the steps of the fabrication process can be carried out in the described and illustrated order, or in other permutations. For example,

in one embodiment of the fabrication steps, the solar cell can be separated from the silicon substrate by partially or entirely destroying the sacrificial layer prior to completing formation of the contact structure.

[0040] While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or embodiments described herein are not intended to limit the scope, applicability, or configuration of the claimed subject matter in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the described embodiment or embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope defined by the claims, which includes known equivalents and foreseeable equivalents at the time of filing this patent application.

CLAIMS

What is claimed is:

1. A method of fabricating a solar cell comprising the steps of:
forming a sacrificial layer on a silicon substrate;
forming a doped silicon layer atop the sacrificial layer;
forming a silicon film atop the doped silicon layer;
forming an oxide layer on the silicon film;
forming alternating P-type and N-type doped regions on the oxide layer;
contacting each of the P-type and N-type doped regions with a metal contact; and
removing the sacrificial layer and the silicon substrate.
2. The method of claim 1, wherein the sacrificial layer comprises silicon and germanium.
3. The method of claim 1, wherein forming the silicon film comprises epitaxially growing the silicon film.
4. The method of claim 1, wherein the alternating P-type and N-type doped regions are formed using an inkjet printer.
5. The method of claim 1, further comprising texturing the surface of the sacrificial layer prior to forming the doped silicon layer.
6. The method of claim 5, wherein forming the doped silicon layer comprises forming a layer of doped silicon conforming to the textured surface of the sacrificial layer.
7. The method of claim 1, further comprising bonding a back side of the solar cell to a carrier before removing the sacrificial layer.
8. The method of claim 7, further comprising the step of debonding the solar cell from the carrier after removing the sacrificial layer.

9. The method of claim 1, further comprising the step of forming a lightly doped silicon layer between the doped silicon layer and the silicon film.

10. A method of fabricating a solar cell comprising the steps of:
forming a sacrificial layer on a top surface of a silicon substrate;
processing an exposed surface of the sacrificial layer to form a textured surface;
forming a heavily doped silicon layer atop the textured surface of the sacrificial layer;
forming a lesser doped silicon layer atop the heavily doped silicon layer;
epitaxially growing a silicon film atop the lesser doped silicon layer;
forming alternating P-type and N-type doped regions over the silicon film;
contacting each of the P-type and N-type doped regions with a metal contact;
bonding a back side of the solar cell to a carrier;
separating the heavily doped silicon layer from the silicon substrate by removing the sacrificial layer;
debonding the solar cell from the carrier; and
forming an anti-reflective coating over the heavily doped silicon layer.

11. The method of claim 10, wherein epitaxially growing the silicon film comprises epitaxially growing a silicon wafer less than 100 micrometers thick.

12. The method of claim 10, wherein forming the heavily doped silicon layer comprises forming a silicon layer of less than 2 micrometers thick.

13. The method of claim 10, wherein the silicon substrate comprises a plurality of sacrificial layers and forming the sacrificial layer comprises doping a top surface of the silicon substrate to form a doped sacrificial layer.

14. The method of claim 10, wherein the sacrificial layer is deposited on the top surface of the silicon substrate using a CVD process.

15. The method of claim 10, wherein forming the lesser doped silicon layer comprises driving dopants from the heavily doped silicon layer into the lesser doped silicon layer.