STRUCTURES FOR WAFER LEVEL TEST AND BURN-IN

Abstract

There is disclosed wafer test and burn-in with state machine or programmable test engines (29) located on the wafer (26) being tested. Each test engine requires less than 10 connections and can be connected to a plurality of chips (28), such as a row or a column of chips on the wafer. Thus, the number of pads (32) of the wafer that must be connected for test is reduced while a large degree of parallel testing is still provided. The test engines also permit on-wafer allocation of redundancy in parallel so that failure chips can be repaired after burn-in is complete. The test engines are used during burn-in to provide high frequency write signals to DRAM arrays that provide a higher effective voltage to the arrays, lowering the time required for burn-in.

Fig 3a