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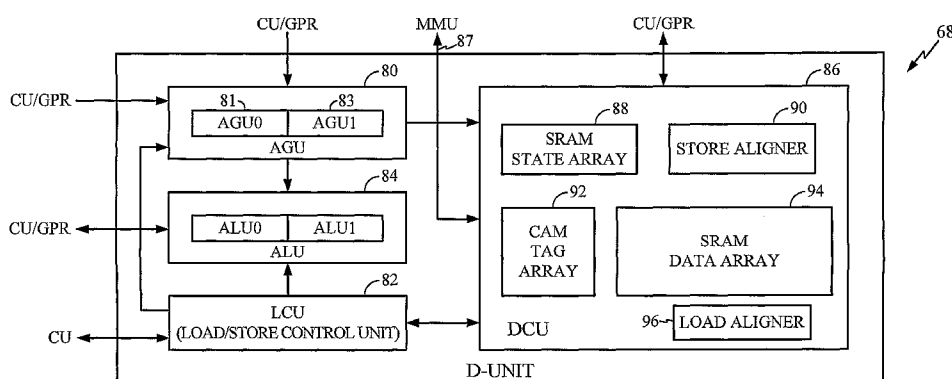
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Declarations under Rule 4.17:

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- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

[Continued on next page]

(54) Title: LOW POWER MICROPROCESSOR CACHE MEMORY AND METHOD OF OPERATION



(57) Abstract: Techniques for processing transmissions in a communications (e.g., CDMA) system including the use of a digital signal processor. The digital signal processor includes a cache memory system and associates a plurality of cache memory match lines with addressable memory lines of an addressable memory. Each of the cache memory match lines associates with one of corresponding sets of the cache memory. The method and system maintain each of the cache memory match lines at a low voltage. Once the digital signal processor initiates a search of the cache memory for retrieving data from a selected one of the corresponding sets of the cache memory, a match line drive circuit drives one of the cache memory match lines from a low voltage to a high voltage. The selected one of the cache memory match lines corresponds to the selected one of the corresponding sets of the cache memory. The digital signal processor compares the selected one of the cache memory match lines to an associated one of the addressable memory lines. Following the comparison step, the process returns the one of the cache memory match lines to the low voltage.



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