

Apparatus comprising an improved ~~d.c. restoration~~ device *for clamp-error compensation*

The present invention relates to an apparatus for receiving a signal conveying analog luminance and chrominance information associated with coded digital signal periods, comprising a d.c. restoration circuit and a decoder circuit for decoding the received digital signal. Such a signal is particularly a signal of the MAC type, which comprises analog luminance and chrominance information components and digital information components coded in packets, as well as analog reference voltage porches for the average grey level.

Such an apparatus is, for example, a television set adapted to receive a signal in the D2-MAC/packet mode, or a satellite tuner, or even any apparatus comprising a device effecting a signal processing operation in a transmission system.

Such an apparatus is known, for example, from the Patent Application FR-A-2,610,773. As described in this document, a television set is provided with means for restoring the d.c. component, in different successive steps which are separate from each other, first on the basis of the peak levels measured on the entire signal, then on the basis of the peak levels measured only on the digital part of the signal, and finally on the basis of the reference voltage porches of the signal.

The problem to be solved stems from the fact that the so-called "d.c." component, which also comprises a low-frequency component, is subject to disturbances which are inherent in all types of transmission systems, whether or not they are correlated with the television signal. These disturbances constitute a spurious signal comprising two components, noise of a frequency which is low relative to the line frequency (low-frequency noise, energy spread, 50 Hz residue, etc.), and the modulation noise whose spectral power distribution depends on the type of transmission.

In the television set described in said document, in the case of peak levels measured on the digital part of the signal, these levels may vary with the digital content of the signal and the recovery of the d.c. component will not be accurate and, when the reference porch is used to extract this component, the theoretical limits of recovery of a signal in the noise will be encountered. As a matter of fact, the porch duration, which is too short, does not permit of an adequate integration over one line. Simple filters have

been proposed which integrate the information of several lines. Based on the principle of a first-order recursive filter, they have the advantage of reducing the noise in the case of unfavourable transmission types, but they lead to a measurement error of the low-frequency component. Tests carried out in the scope of a transmission of a television signal in accordance with the D2-MAC/packet standard have shown how difficult it is to obtain a compromise between noise and low-frequency residues, which compromise must be adapted to each specific case constituted by each modulation type.

The invention provides an apparatus in which these problems are solved. To this end the d.c. restoration circuit comprises a coding device which on the basis of the decoded digital signal performs a coding operation similar that used to generate the received signal, a d.c. component estimation circuit which calculates an estimate from the differences between the coded signal received and the coded signal reconstructed by said coding device, which estimate constitutes a d.c. component correction signal, and a subtracter circuit for subtracting said correction signal from the received signal throughout the duration of one line.

Advantageously, it also comprises a filter circuit at the output of the estimation circuit, which filter circuit is advantageously a simple averager. This has the advantage that it reduces the occurrence of noise in the determination of the d.c. component.

Advantageously the apparatus downstream the d.c. component estimation circuit it includes a filter using the correction signals of several line scanning periods at a time to improve the correction signal, before the subtracter circuit subtracts this correction signal from the received signal, said filter being of the finite impulse response type, for example an averager, and a delay circuit arranged downstream the subtracter circuit, for delaying the received signal to compensate for the delay caused by the filter.

The invention is consequently based on the principle of extracting additional information from the low-frequency component of the signal by efficiently using the digital period and, on the other hand, integrating this information over several lines with the aid of an appropriate filter which preserves the low-frequency component.

Moreover, at the input of the decoder, the apparatus advantageously comprises a subtracting circuit for subtracting the correction signal from the received signal. This improves the reliability of the decoding operation.

Another important characteristic of the invention is based on the recognition that the presence of the coding device allows an estimation of the reliability of the received signal. The apparatus is therefore advantageously comprises a validation circuit which, on the basis of the measurement of the deviation between the received
5 signal and the recovered signal, determines whether the correction signal is to be taken into account.

Fig. 1 is a block diagram of the preferred embodiment of a device for restoring the d.c. component in an apparatus according to the invention.

10 Fig. 2 shows levels taken into account for deciding and recoding in the case of a signal of the duobinary type for a decoder with a threshold.

An amplified signal is available, for example, of the D2-MAC-packet type, which first has a duobinary coded digital data period whose duration is 10 μ s, subsequently an average-grey-level reference porch of only 0.75 μ s duration, followed
15 by an analog signal period representing the chrominance information and an analog signal period representing the luminance information, which completes the line.

In Fig. 1 the amplified signal available at 1 is first applied to a conventional d.c. clamping device 2 based on the line porches. The device further includes a digital data decoder 3 followed by a coding device 4 for coding this
20 data, which device is of the same type as that used to generate the received signal. In customary manner the digital data decoder 3 can take the form of a low-pass filter having a cut-off frequency of 5 MHz followed by a decoder with a threshold or, if desired, a Viterbi decoder.

An associated circuit 5 enables the validity of the reconstructed digital
25 signal to be measured on the basis of the signal present at the input of the decoder 3. In the estimation circuit 6 the reconstructed coded digital signal is compared with the available signal, which is taken from either the input 1 or from the output of the conventional d.c. clamping system 2, which choice is shown symbolically in the Figure by means of a change-over switch 18, which need not be physically present since a
30 definite choice can be made during the design. The estimation circuit 6 produces a correction signal on the basis of this comparison. In its simplest form the estimation circuit 6 is a circuit which subtracts the received signal and the reconstructed signal from each other. Alternatively, in a more sophisticated but not indispensable version, it

may take the form of a recursive circuit which corrects a preceding correction signal by adding thereto a signal calculated from the differences between the received signal and the reconstructed signal (*i.e.* not only the difference in the arithmetic sense but also of other parameters representing a non-similarity) weighted by a fixed or variable coefficient, which may be dependent on characteristics of the transmission channel.

The estimation circuit 6 is followed by a filter circuit 7. In addition to the information present on the normal reference porch (which is always available since the signals of this porch are processed by the circuit 6 as forming part of the duobinary burst) the circuit 7 uses information extracted from the duobinary burst and supplied by the circuit 6, which when validated allow of the reconstruction of the low-frequency component. This circuit 7 which, in a preferred embodiment, is formed by a simple averager, produces a result value per line. A subtraction circuit 19 subtracts the correction signal from signal the received at the input of the decoder 3. Depending on the position of a change-over switch 15 the signal thus subtracted is either the signal available at the output of the estimation circuit 6, or the signal available at the output of the filter circuit 7. In the same way as with the switch 18 there may not be a switch 15 when a definite connection has been chosen during the design. The result value supplied by the filter circuit 7 is subsequently processed by a circuit 8 so as to correct its value by weighting it with those values obtained for the preceding lines. This circuit, which is a filter, can either be a filter of the recursive type and supply information in synchronism with the current line, or it can supply information delayed by the duration of an integral number of lines. Finally, the subtraction circuit 9 subtracts the correction signal, throughout the duration of a line, from the signal available at either the input 1 or, if desired, at the output of the conventional d.c. clamping system 2, which signal may be delayed (in accordance with the delay of the line filter) in a circuit 10 so as to ensure that the two signals are in synchronism.

Fig. 2, in which the reference numerals 14 indicate the decision thresholds and the references 13 indicate three ranges of the same width, said width defining a reliability threshold, illustrates the reconstruction of the duobinary train when the element 3 is a decoder with a threshold.

This reconstruction is summarized by the following logic operations:

if $|c_k - C_c| \leq \text{decision threshold (14)}, \hat{c}_k = 0$
if $c_k - C_c < \text{negative decision threshold (14)}, \hat{c}_k = -0.4$

if $c_k - C_c > \text{positive decision threshold (14)}$, $\hat{c}_k = +0.4$

where c_k represents the value (digital value in volts) of the received duobinary sample, $\hat{c}_k$ represents the value of the reconstructed duobinary sample, and C_c represents the value of the d.c. component subtracted at the input of the decoder 3.

The control circuit 5 provides an estimate of the reliability of the reconstruction of the duobinary signal in the form of a validation signal 12 intended for the filter module 7. To this end it operates in the following manner: the reconstructed signal is compared with the duobinary signal present at the input of the decoder, and a voltage applied to 11 defines a reliability threshold, which represents the maximum permissible difference between the two signals, above which difference the reconstructed sample will be ignored in the calculation of the low-frequency component. In the case of, for example, decoding/recoding into D2-MAC-packets, which is effected over one hundred-and-five bits per line, the decision whether the sample is to be taken into account or is to be ignored is taken for each one of these one hundred-and-five bits.

The function performed by this circuit 5, which is very simple, is summarized by the following logic operation:

if $|c_k - C_c - \hat{c}_k| < \text{reliability threshold}$, validation is effected.

Thus, the device comprises a validation circuit which, on the basis of the measurement of the deviation between the received signal and the reconstructed signal, determines whether the correction signal is to be taken into account.

In a preferred embodiment the circuit 8, which allows the information coming from the filter 7 to be weighted by the values obtained for the preceding lines, is a non-recursive filter, commonly referred to as a "finite impulse response" filter.

This filter has the advantage that it has a response whose delay relative to the input data is fixed for a given filter length and can thus be compensated for so as to ensure a perfect synchronization.

A simple and advantageous embodiment is constituted by an averager, which preferably acts on an odd number of data. The delay generated by the averager is equal to half its length, and is consequently equal to $(N-1)/2$ line periods if the filter acts on N data. In this case the circuit 10 delays the signal available at the input 1 or, if desired, at the output of the conventional d.c. clamping system 2 by this value.

CLAIMS:

1. An apparatus for receiving a signal conveying analog luminance and chrominance information associated with coded digital signal periods, comprising a d.c. restoration circuit and a decoder circuit (3) for decoding the received digital signal, characterised in that the d.c. restoration circuit comprises a coding device (4) which on
5 the basis of the decoded digital signal performs a coding operation similar that used to generate the received signal, a d.c. component estimation circuit (6) which calculates an estimate from the differences between the coded signal received (1) and the coded signal reconstructed by said coding device, which estimate constitutes a d.c. component correction signal, and a subtracter circuit (9) for subtracting said correction signal from
10 the received signal throughout the duration of one line.
2. An apparatus as claimed in Claim 1, characterised in that it includes a filter circuit (7) at the output of the estimation circuit.
3. An apparatus as claimed in Claim 2, characterised in that the filter circuit (7) is a simple averager.
- 15 4. An apparatus as claimed in Claim 1, characterised in that downstream the d.c. component estimation circuit (6) it includes a filter (8) using the correction signals of several line scanning periods at a time to improve the correction signal, before the subtracter circuit (9) subtracts this correction signal from the received signal, said filter being of the finite impulse response type, for example an averager, and a delay circuit
20 (10) arranged downstream the subtracter circuit (9), for delaying the received signal to compensate for the delay caused by the filter (8).
5. An apparatus as claimed in any one of the preceding Claims, characterized in that at the input of the decoder (3) it includes a subtracter circuit (19) which subtracts the correction signal from the received signal.
- 25 6. An apparatus as claimed in any one of the preceding Claims, wherein the decoder (3) is of the type having a threshold, characterised in that the coding device (4) is a logic circuit performing the following logic operations:



if $|c_k - C_c| \leq$ decision threshold, $\hat{c}_k = 0$,

if $c_k - C_c <$ negative decision threshold (14), $\hat{c}_k$ assumes a negative standard value

5 if $c_k - C_c >$ positive decision threshold, $\hat{c}_k$ assumes a positive standard value, where c_k represents the value of the received duobinary sample, $\hat{c}_k$ represents the value of the reconstructed duobinary sample, and C_c represents the value of the correction signal.

7. An apparatus as claimed in any one of the Claims 1 to 6, characterised in
10 that it includes a validation circuit (5) which, on the basis of the measurement of the deviation between the received signal and the reconstructed signal, determines whether the correction signal is to be taken into account.

8. An apparatus as claimed in Claim 7, characterised in that the validation
circuit (5) decides that the correction signal is to be taken into account if $|c_k - C_c - \hat{c}_k|$ is
15 smaller than a given reliability threshold, c_k representing the value of the received duobinary sample, $\hat{c}_k$ representing the value of the reconstructed binary sample, and C_c representing the value of the correction signal.

9. An apparatus as claimed in any one of the preceding Claims, characterised
in that upstream the decoder it further includes a d.c. clamping device (2) based on
20 analog voltage porches contained in the received signal.