

VARIABLE POWER AMPLIFIER BIAS IMPEDANCE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of U.S. Provisional Application No. 62/713,150, filed August 1, 2018, which is hereby incorporated by reference in its entirety.

BACKGROUND

Field

[0002] Embodiments of the described technology relate to electronic systems, and in particular, to systems including power amplifiers for radio frequency (RF) electronics.

Description of the Related Technology

[0003] RF power amplifiers can be used to boost the power of an RF signal having a relatively low power. Thereafter, the boosted RF signal can be used for a variety of purposes, included driving the antenna of a transmitter.

[0004] Power amplifiers can be included in mobile phones to amplify an RF signal for transmission. For example, in mobile phones that communicate using a cellular standard, a wireless local area network (WLAN) standard, and/or any other suitable communication standard, a power amplifier can be used to amplify the RF signal. It can be important to manage the amplification of an RF signal, as amplifying the RF signal to an incorrect power level or introducing significant distortion of the original RF signal can cause a wireless device to transmit out of band or violate compliance with accepted standards. Biasing of a power amplifier device is an important part of managing the amplification because it can determine the voltage and/or current operating point of the amplifying devices within the power amplifier.

[0005] There is a need for improved power amplifier systems. Furthermore, there is a need for improving power amplifier biasing.

SUMMARY

[0006] Aspects of this disclosure relate to techniques and electronic systems which can be used to improve power amplifier biasing. For example, in one example, a power amplifier system, includes a bias circuit configured to receive a bias voltage and generate a bias signal; a power amplifier stage configured to receive an input radio frequency signal and generate an output radio frequency signal. The system further includes a bias impedance component operatively coupled between the bias circuit and the power amplifier stage, the bias impedance component configured to receive a control signal and adjust an impedance value of the bias impedance component in response to the control signal.

[0007] A method of adjusting a gain of a power amplifier stage is provided according to the disclosure. The method includes receiving, at a bias circuit, a bias voltage, generating, by the bias circuit, a bias signal based on the bias voltage, and receiving, at a bias impedance component, the bias voltage and a control signal. The method further includes adjusting, at the bias impedance component, an impedance value of the bias impedance component based on the received control signal, receiving, at a power amplifier stage, an input radio frequency signal and the bias voltage from the bias impedance component, and generating an output radio frequency signal based on the input radio frequency signal and the bias voltage.

[0008] A mobile device is provided according to the disclosure. The mobile device includes a power amplifier configured to amplify an input radio frequency signal and generate an output radio frequency signal and a modulator configured to generate a radio frequency transmit signal based on the output radio frequency signal. The power amplifier includes a bias circuit configured to receive a bias voltage and generate a bias signal, a power amplifier stage configured to receive the input radio frequency signal and generate the output radio frequency signal, and a bias impedance component operatively coupled between the bias circuit and the power amplifier stage. The bias impedance component is configured to receive a control signal and adjust an impedance value of the bias impedance component in response to the control signal. According to an aspect of the disclosure, there is provide a power amplifier system comprising:
a bias circuit configured to receive a bias voltage and generate a bias signal;

a power amplifier stage configured to receive an input radio frequency signal and generate an output radio frequency signal; and

a bias impedance component operatively coupled between the bias circuit and the power amplifier stage, the bias impedance component including a transistor configured to receive a control signal and adjust an impedance value of the transistor in response to the control signal, the bias impedance component configured to apply the impedance value of the transistor to bias the power amplifier stage, the control signal being received separately from the bias circuit. According to another aspect, there is provided a method of adjusting a gain of a power amplifier stage, comprising:

receiving, at a bias circuit, a bias voltage;

generating, by the bias circuit, a bias signal based on the bias voltage;

receiving, at a bias impedance component, the bias voltage and a control signal, the bias impedance component including a transistor, the control signal being received separately from the bias circuit;

adjusting, at the bias impedance component, an impedance value of the transistor based on the received control signal;

applying the impedance value of the transistor to the bias voltage:

receiving, at a power amplifier stage, an input radio frequency signal and the bias voltage from the bias impedance component; and

generating an output radio frequency signal based on the input radio frequency signal and the bias voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a schematic diagram of a power amplifier module for amplifying a radio frequency (RF) signal.

[0010] FIG. 2 is a schematic block diagram of an example wireless device that can include one or more of the power amplifier modules of FIG. 1.

[0011] FIG. 3 is a schematic block diagram of one example of a power amplifier system.

[0012] FIG. 4 is a schematic block diagram of another example of a power amplifier system in accordance with aspects of this disclosure.

[0013] FIG. 5A is a schematic block diagram of yet another example of a power amplifier system in accordance with aspects of this disclosure.

[0014] FIG. 5B is a schematic block diagram of still yet another example of a power amplifier system in accordance with aspects of this disclosure.

[0015] FIGs. 6A-6F are graphs illustrating the effect of changes in the bias impedance on power amplifier characteristics in accordance with aspects of this disclosure.

[0016] FIG. 7 is a graph illustrating the gain at the output stage of a power amplifier as a function of the output power in accordance with aspects of this disclosure.

[0017] FIGs. 8A-8D illustrate a number of power amplifier characteristics in accordance with aspects of this disclosure.

[0018] FIG. 9 illustrates an embodiment of a multi-stage power amplifier system in accordance with aspects of this disclosure.

[0019] FIG. 10 is a schematic block diagram of another example of a power amplifier system in accordance with aspects of this disclosure.

[0020] FIG. 11 is a schematic block diagram of yet another example of a power amplifier system in accordance with aspects of this disclosure.

DETAILED DESCRIPTION

[0021] The headings provided herein, if any, are for convenience only and do not necessarily affect the scope or meaning of the claimed invention.

[0022] Apparatus and methods for biasing power amplifiers are disclosed herein. In certain implementations, a power amplifier system including a power amplifier and a bias circuit is provided. The power amplifier can be used to amplify a radio frequency (RF) signal for transmission, and the bias circuit can be used to generate a bias voltage for biasing the power amplifier. The power amplifier bias circuit can receive an enable signal that can be used to enable or disable the power amplifier so as to pulse the power amplifier's output.

[0023] As is described in greater detail below, the bias impedance of the signal provided to the power amplifier by the bias circuit may affect certain characteristics of the power amplifier, and in particular, the power amplifier gain characteristics. Thus, the design and selection of the bias impedance provided by the bias circuit is an important design characteristic to be considered during power amplifier system design. Aspects of this disclosure relate to a power amplifier system which may have an adjustable bias impedance, which can be used to select power amplifier gain characteristics depending on the design and/or application requirements of the power amplifier system.

Overview of Examples of Power Amplifier Systems

[0024] FIG. 1 is a schematic diagram of a power amplifier module 10 for amplifying a radio frequency (RF) signal. The illustrated power amplifier module (PAM) 10 can be configured to amplify an RF signal RF_IN to generate an amplified RF signal RF_OUT. As described herein, the power amplifier module 10 can include one or more power amplifiers, including, for example, multi-stage power amplifiers.

[0025] FIG. 2 is a schematic block diagram of an example wireless or mobile device 11 that can include one or more of the power amplifier modules of FIG. 1. The wireless device 11 can include power amplifier bias circuits implementing one or more features of the present disclosure.

[0026] The example wireless device 11 depicted in FIG. 2 can represent a multi-band and/or multi-mode device such as a multi-band/multi-mode mobile phone. In the illustrated configuration, the wireless device 11 includes switches 12, a transceiver 13, an antenna 14, power amplifiers 17, a control component 18, a computer readable medium 19, a processor 20, and a battery 21.

[0027] The transceiver 13 can generate RF signals for transmission via the antenna 14. Furthermore, the transceiver 13 can receive incoming RF signals from the antenna 14.

[0028] It will be understood that various functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in FIG. 2 as the transceiver 13. For example, a single component can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate components.

[0029] Similarly, it will be understood that various antenna functionalities associated with the transmission and receiving of RF signals can be achieved by one or more components that are collectively represented in FIG. 2 as the antenna 14. For example, a single antenna can be configured to provide both transmitting and receiving functionalities. In another example, transmitting and receiving functionalities can be provided by separate antennas. In yet another example, different bands associated with the wireless device 11 can be provided with different antennas.

[0030] In FIG. 2, one or more output signals from the transceiver 13 are depicted as being provided to the antenna 14 via one or more transmission paths 15. In the example shown, different transmission paths 15 can represent output paths associated with different bands and/or different power outputs. For instance, the two example power amplifiers 17 shown can represent amplifications associated with different power output configurations (e.g., low power output and high power output), and/or amplifications associated with different bands. Although FIG. 2 illustrates a configuration using two transmission paths 15, the wireless device 11 can be adapted to include more or fewer transmission paths 15.

[0031] The power amplifiers 17 can be used to amplify a wide variety of RF signals. For example, one or more of the power amplifiers 17 can receive an enable signal that can be used to pulse the output of the power amplifier to aid in transmitting a wireless local area network (WLAN) signal or any other suitable pulsed signal. In certain configurations, one or more of the power amplifiers 17 are configured to amplify a Wi-Fi signal. Each of the power amplifiers 17 need not amplify the same type of signal. For example, one power amplifier can amplify a WLAN signal, while another power amplifier

can amplify, for example, a Global System for Mobile (GSM) signal, a code division multiple access (CDMA) signal, a W-CDMA signal, a Long Term Evolution (LTE) signal, or an EDGE signal.

[0032] One or more features of the present disclosure can be implemented in the foregoing example modes and/or bands, and in other communication standards.

[0033] In FIG. 2, one or more detected signals from the antenna 14 are depicted as being provided to the transceiver 13 via one or more receiving paths 16. In the example shown, different receiving paths 16 can represent paths associated with different bands. Although FIG. 2 illustrates a configuration using four receiving paths 16, the wireless device 11 can be adapted to include more or fewer receiving paths 16.

[0034] To facilitate switching between receive and transmit paths, the switches 12 can be configured to electrically connect the antenna 14 to a selected transmit or receive path. Thus, the switches 12 can provide a number of switching functionalities associated with an operation of the wireless device 11. In certain configurations, the switches 12 can include a number of switches that provide functionalities associated with, for example, switching between different bands, switching between different power modes, switching between transmission and receiving modes, or some combination thereof. The switches 12 can also provide additional functionality, including filtering and/or duplexing of signals.

[0035] FIG. 2 shows that in certain configurations, a control component 18 can be provided for controlling various control functionalities associated with operations of the switches 12, the power amplifiers 17, and/or other operating component(s), such as bias circuits. Non-limiting examples of the control component 18 are described herein in greater detail.

[0036] In certain configurations, a processor 20 can be configured to facilitate implementation of various processes described herein. The processor 20 can operate using computer program instructions. These computer program instructions may be provided to the processor 20.

[0037] In certain configurations, these computer program instructions may also be stored in a computer-readable memory 19 that can direct the processor 20 or other programmable data processing apparatus to operate in a particular manner.

[0038] The battery 21 can be any suitable battery for use in the wireless device 11, including, for example, a lithium-ion battery.

[0039] FIG. 3 is a schematic block diagram of one example of a power amplifier system 26. The illustrated power amplifier system 26 includes the switches 12, the antenna 14, the battery 21, a directional coupler 24, a power amplifier bias circuit 30, a power amplifier 32, and a transceiver 33. The illustrated transceiver 33 includes a baseband processor 34, an I/Q modulator 37, a mixer 38, and an analog-to-digital converter (ADC) 39. Although not illustrated in FIG. 3 for clarity, the transceiver 33 can include circuitry associated with receiving signals over one or more receive paths.

[0040] The baseband signal processor 34 can be used to generate an I signal and a Q signal, which can be used to represent a sinusoidal wave or signal of a desired amplitude, frequency, and phase. For example, the I signal can be used to represent an in-phase component of the sinusoidal wave and the Q signal can be used to represent a quadrature component of the sinusoidal wave, which can be an equivalent representation of the sinusoidal wave. In certain implementations, the I and Q signals can be provided to the I/Q modulator 37 in a digital format. The baseband processor 34 can be any suitable processor configured to process a baseband signal. For instance, the baseband processor 34 can include a digital signal processor, a microprocessor, a programmable core, or any combination thereof. Moreover, in some implementations, two or more baseband processors 34 can be included in the power amplifier system 26.

[0041] The I/Q modulator 37 can be configured to receive the I and Q signals from the baseband processor 34 and to process the I and Q signals to generate an RF signal. For example, the I/Q modulator 37 can include DACs configured to convert the I and Q signals into an analog format, mixers for upconverting the I and Q signals to radio frequency, and a signal combiner for combining the upconverted I and Q signals into an RF signal suitable for amplification by the power amplifier 32. In certain implementations, the I/Q modulator 37 can include one or more filters configured to filter frequency content of signals processed therein.

[0042] The power amplifier bias circuit 30 can receive an enable signal ENABLE from the baseband processor 34 and a battery or power high voltage V_{CC} from the battery 21,

and can use the enable signal ENABLE to generate a bias voltage V_{BIAS} for the power amplifier 32.

[0043] Although FIG. 3 illustrates the battery 21 directly generating the power high voltage V_{CC} , in certain implementations the power high voltage V_{CC} can be a regulated voltage generated by a regulator that is powered using the battery 21. In one example, a switching regulator, such as a buck and/or boost converter, can be used to generate the power high voltage V_{CC} .

[0044] The power amplifier 32 can receive the RF signal from the I/Q modulator 37 of the transceiver 33, and can provide an amplified RF signal to the antenna 14 through the switches 12.

[0045] The directional coupler 24 can be positioned between the output of the power amplifier 32 and the input of the switches 12, thereby allowing an output power measurement of the power amplifier 32 that does not include insertion loss of the switches 12. The sensed output signal from the directional coupler 24 can be provided to the mixer 38, which can multiply the sensed output signal by a reference signal of a controlled frequency so as to downshift the frequency content of the sensed output signal to generate a downshifted signal. The downshifted signal can be provided to the ADC 39, which can convert the downshifted signal to a digital format suitable for processing by the baseband processor 34.

[0046] By including a feedback path between the output of the power amplifier 32 and the baseband processor 34, the baseband processor 34 can be configured to dynamically adjust the I and Q signals to optimize the operation of the power amplifier system 26. For example, configuring the power amplifier system 26 in this manner can aid in controlling the power added efficiency (PAE) and/or linearity of the power amplifier 32.

Power Amplifier Bias

[0047] A theoretically ideal power amplifier has linear gain and phase characteristics regardless of the input or output power of the power amplifier. The gain characteristics of a power amplifier may be plotted on an AM/AM graph which illustrates the change in output amplitude vs. the change in input amplitude. As used herein, AM may refer to amplitude variation. The theoretically ideal power amplifier has a variation in the AM/AM

plot of 0 dB/dB. The phase characteristics of a power amplifier may be plotted on an AM/PM graph which illustrates the change in output phase vs. the change in input amplitude. As used herein, PM may refer to phase variations. Similar to the ideal AM/AM characteristics, the theoretically ideal power amplifier has a variation in the AM/PM plot of 0 dB/dB.

[0048] Since real-world power amplifiers cannot achieve the flat gain and phase characteristics of the theoretical ideal power amplifier, one important aspect of power amplifier design is improving the linearity of the gain and phase characteristics of the power amplifier. In certain implementations, there may be trade-offs in terms of the achievable linearity of the gain and phase characteristics of a power amplifier without negatively affecting the output power and efficiency of the power amplifier. In a multi-stage power amplifier system, the gain and phase characteristics of the power amplifiers at each stage in the system may be selected such that the overall gain and phase characteristics are substantially linear.

[0049] FIG. 4 is a schematic block diagram of another example of a power amplifier system in accordance with aspects of this disclosure. In particular, the illustrated power amplifier system 27 includes a power amplifier bias circuit 30, a power amplifier stage 41, a current source 75, and a bias impedance component 80. The power amplifier bias circuit 30 may include a transistor 71 and two diodes 73 and 74. The components of the power amplifier bias circuit 30, together with the current source 75, may be arranged so as to generate a current mirror which mirrors the current generated by the power amplifier stage 41. The output of the power amplifier bias circuit 30 is supplied to the bias impedance component 80, which is in turn coupled to the power amplifier stage 41 to provide a bias signal thereto.

[0050] The power amplifier stage 41 is configured to receive both an input RF signal RFIN and the bias signal from the bias impedance component 80. Based on the received signals, the power amplifier stage 41 is configured to generate an output RF signal RFOUT. The power amplifier stage 41 is configured to generate the output RF signal RFOUT as an amplified version of the input RF signal RFIN having gain and phase characteristics which approach that of the theoretical ideal power amplifier (e.g., the gain and

phase characteristics are designed to be within a threshold range of 0 dB/dB). The power amplifier stage 41 includes a transistor 61, a plurality of capacitors 52, 65, and 64, and a plurality of inductors 53, 63, and 66. The capacitors 52, 65, and 64 and inductors 53, 63, and 66 couple the transistor 61 to receive the input RF signal RFIN, and a power supply voltage Vcc and to generate the output RF signal RFOUT.

[0051] The base of the transistor 61 receives the bias signal generated by the power amplifier bias circuit 30 via the bias impedance component 80. In certain implementations, the impedance value of the bias impedance component 80 may be selected to dominate the overall bias impedance applied to the base of the transistor 61. In certain implementations the bias impedance applied to the base of the transistor 61 may be equal to the sum of the output impedance of the transistor 71 and the impedance value of the bias impedance component 80. Thus, the impedance value of the bias impedance component 80 may be selected to dominate the impedance value of the transistor 71 (e.g., the impedance value of the bias impedance component 80 may be one or more orders of magnitude larger than the impedance value of the transistor 71). In exemplary embodiments, the output impedance of the transistor 71 is inversely related to the trans conductance of the transistor 71, which may result in an output impedance for the transistor 71 on the order of 10 Ω .

[0052] In certain embodiments, the transistor 61 may comprise a heterojunction bipolar transistor (HBT), which may adapted for the high frequency signals the power amplifier system 27 is designed to receive and amplify. In particular, HBTs may have high performance and efficiency for RF power amplification as used in the embodiments disclosed herein. In order to properly generate the mirror current in the power amplifier bias circuit, the transistor 71 may also comprise an HBT in certain embodiments.

[0053] One technique for adjusting the gain and phase characteristics of a power amplifier may be to select a fixed bias impedance to be applied to the bias signal supplied to the base of the transistor 61. The particular bias impedance may be selected during design and development of the power amplifier stage 41 and implemented by selecting the impedance value of the bias impedance component 80. For example, the impedance value of the bias impedance component 80 may be selected via die variants and/or laser trim-able resistors. However, the impedance value of the bias impedance component 80 may be

selected to adjust and/or improve the linearity of the gain and phase characteristics for the power amplifier system 27 for a single power level, modulation, and frequency. Thus, if the power amplifier system 27 is used at a different power level, modulation, and/or frequency from the values used in selecting the value of the bias impedance component 80, the linearity of the gain and/or phase characteristics of the power amplifier system may suffer.

[0054] Accordingly, certain aspects of this disclosure relate to the use of a variable bias impedance component which may be applied to bias a power amplifier. FIG. 5A is a schematic block diagram of yet another example of a power amplifier system in accordance with aspects of this disclosure. Components of the power amplifier system 28 illustrated in FIG. 5A which are similar to, or substantially the same as, components in the power amplifier system 27 illustrated in FIG. 4 are represented by the same reference numerals and detailed descriptions thereof may be omitted for the sake of clarity.

[0055] As shown in FIG. 5A, the power amplifier system 28 includes a power amplifier bias circuit 30, a power amplifier stage 41, a current source 75, and a bias impedance component 81. In FIG. 5A, the bias impedance component may be implemented as a variable bias impedance component 85. Similar to the power amplifier system 27 of FIG. 4, in the embodiment of FIG. 5A, the output of the power amplifier bias circuit 30 is supplied to the variable bias impedance component 85, which is in turn coupled to the power amplifier stage 41 to provide a bias signal thereto. The variable bias impedance component 85 may be configured to receive a control signal CTRL configured to adjust the impedance value of the variable bias impedance component 85. Accordingly, the impedance value of the variable bias impedance component 85 may be adjusted based on the voltage of the control signal CTRL. In the illustrated example, the variable bias impedance component 85 can be implemented using any variable impedance element (e.g., a variable resistor) controllable by a control signal CTRL.

[0056] Certain variable impedance technologies may not be practical for all power amplifier systems 28, and in particular, for power amplifiers which may be implemented in mobile phones to amplify RF signals for transmission. As discussed above, in certain RF power amplifier applications, it is desirable to implement the transistor 61 of the amplifier stage 41 as an HBT transistor since HBTs may have the performance and efficiency

characteristics that are desirable for use in an RF power amplifier. In some semiconductor fabrication techniques, it may be difficult to combine different device technologies on a single semiconductor die. For example, the combination of an HBT with a field effect transistor (FET) onto the same semiconductor die may not result in a device having the desired transistor properties. As discussed in U.S. Patent Number 9,105,488 B2, patented on August 11, 2015, hereby incorporated by reference in its entirety, some attempts to integrate a FET into a GaAs HBT process have resulted only in an n-type FET device. However, recent developments in the fabrication technology as exemplified by U.S. Patent Number 9,105,488 B2 have enabled the fabrication of HBTs and FETs onto a single semiconductor die.

[0057] Using techniques which enable the fabrication of a semiconductor device having both HBT and FET technologies, one embodiment of the power amplifier 28 of FIG. 5A is illustrated in FIG. 5B. FIG. 5B is a schematic block diagram of still yet another example of a power amplifier system in accordance with aspects of this disclosure. The power amplifier 29 illustrated in FIG. 5B includes a power amplifier bias circuit 30, a power amplifier stage 41, and a current source 75, each of which may be the same as or similar to those discussed above in connection with FIG. 5A. The power amplifier 29 further includes a bias impedance component 81 which includes an FET 90 in place of the variable bias impedance component 85 of FIG. 5A. The FET 90 may be configured to receive a control signal CTRL at a gate thereof via an optional resistor 95. The control signal is configured to adjust the impedance value of the FET 90. Accordingly, the impedance value of the FET 90 may be adjusted by selecting the voltage of the control signal CTRL. In exemplary embodiments, the FET 90 may be operated in triode via the selection of the voltage of the control signal CTRL. As understood by those skilled in the art, the triode region of the FET 90 may refer to a range of voltages which can be applied to the gate of the FET 90 such that the FET 90 operates in a fashion similar to a resistor (e.g., the FET 90 may have a substantially linear response while operated in triode). Thus, the impedance of the FET 90 may be controlled by the control signal CTRL when the FET 90 is operated within the triode region.

[0058] The value of the bias impedance supplied to the base of the transistor 61 of the amplifier stage 41 may affect the gain and phase characteristics of the power amplifier 28

or 29. In particular, FIGs. 6A-6F are graphs illustrating the effect of changes in the bias impedance on power amplifier characteristics in accordance with aspects of this disclosure. FIGs. 6A-6C illustrate power amplifier characteristics when a relatively high impedance is applied to the base of the transistor of a power amplifier while FIGs. 6D-6F illustrate power amplifier characteristics when a relatively low impedance is applied to the base of the transistor of a power amplifier. FIGs. 6A-6F are meant only to illustrate how increasing or decreasing the bias impedance value affects the power amplifier characteristics, and thus, the specific values of the bias impedance value which result in the illustrated graphs are not limiting. In certain embodiments, a “low” impedance value may be substantially zero impedance while a “high” impedance value may be an infinite impedance value.

[0059] FIGs. 6A and 6D are graphs which show the base-collector voltage (V) and base current (A) of a transistor (such as transistor 61 of FIG. 5A or 5B) in a power amplifier as a function of the input power (dBm) to the transistor under “high” and “low” bias impedance. Of note in the high bias impedance of FIG. 6A, the base-collector voltage (V) decreases with increasing input power while in the low bias impedance of FIG. 6D, the base-collector voltage (V) is substantially fixed with increasing input power.

[0060] FIGs. 6B and 6E are graphs which show the gain (dB) and output power (dBm) of the transistor in a power amplifier as a function of the input power (dBm) to the transistor under “high” and “low” bias impedance. Here, in the high bias impedance of FIG. 6B, the gain “compresses” or decreases with increasing input power while in the low bias impedance of FIG. 6E, the gain increases with increasing input power. Thus, by selecting the bias impedance with a value between the illustrated “high” and “low” values, the gain characteristics of the power amplifier can be improved by flattening the gain out, thereby improving gain linearity.

[0061] FIGs. 6C and 6F are graphs which show the output current (A) of the transistor in a power amplifier as a function of the input power (dBm) to the transistor under “high” and “low” bias impedance. Here, in the high bias impedance of FIG. 6C, the DC output current is substantially fixed with respect to input power while in the low bias impedance of FIG. 6F, the DC output current increases with increasing input power.

[0062] FIG. 7 is a graph illustrating the gain at the output stage of a power amplifier as a function of the output power in accordance with aspects of this disclosure. Various gain curves are illustrated in FIG. 7 at different impedance bias levels which range from an impedance of 5 Ω to an impedance of 1000 Ω as shown in the legend. As the bias impedance is increased the gain drops with increasing output power. In the illustrated embodiment, an impedance bias of 50 Ω may be selected to provide a substantially flat gain. However, other power amplifier topologies may result in different output stage gain plots, and thus, the specific impedance bias which results in a substantially flat gain may depend on the particular implementation of the power amplifier.

[0063] FIGs. 8A-8D illustrate a number of power amplifier characteristics in accordance with aspects of this disclosure. In particular, FIG. 8A illustrates the gain (dB) as a function of output power for a power amplifier at a number of different bias impedance values; FIG. 8B illustrates the phase (deg) as a function of output power for a power amplifier at the different bias impedance values; FIG. 8C illustrates the power amplifier efficiency (%) as a function of output power for a power amplifier at the different bias impedance values; and FIG. 8D illustrates the transistor collector current (mA) as a function of output power for a power amplifier at the different bias impedance values.

[0064] As shown in FIGs. 8B-8D, the bias impedance value does not have a significant effect on the phase, power amplifier efficiency, or transistor collector current characteristics of the power amplifier. However, as shown in FIG. 8A, the bias impedance value affects the gain characteristics of the power amplifier, with increasing gate control voltage (e.g., increasing bias impedance) resulting in an increase in gain as a function of output power. Thus, the adjustment of the bias impedance may be an effective tool for adjusting the gain characteristics of the power amplifier without significantly affecting the phase, power amplifier efficiency, and transistor collector current characteristics of the power amplifier.

[0065] FIG. 9 illustrates an embodiment of a multi-stage power amplifier system in accordance with aspects of this disclosure. In particular, the power amplifier system 121 of FIG. 9A includes a first power amplifier 120 and a second power amplifier 125 connected in series between an RF input port RFIN and an RF output port RFOUT. Each of the first

and second power amplifiers 120 and 125 may be the same as or similar to the power amplifier 29 illustrated in FIG. 5B. Thus, a detailed description of each of the constituent components will not be provided. In the embodiment of FIG. 9, the bias impedance value supplied to the base of the transistors 61 of each of the power amplifiers 120 and 125 may be individually selected in accordance with the particular implementations of the amplifier stages 41 and the power amplifier bias circuits 30 in each of the first and second power amplifiers 120 and 125. Further, the bias impedances selected by the gate control voltages Gate CTRL applied to the respective amplifier stages 41 may be selected such that the overall gain of the power amplifier system 121 (e.g., the gain at the output port RFOUT for a signal applied to the input port RFIN) is sufficiently flat. Thus, in certain implementations, the gains of each of the first and second power amplifiers 120 and 125 may not be substantially flat so long as the overall gain of the power amplifier system 121 has a variation that is less than a threshold value from the ideal variation of 0 dB/dB.

[0066] FIG. 10 is a schematic block diagram of another example of a power amplifier system in accordance with aspects of this disclosure. The power amplifier 130 illustrated in FIG. 10 includes a power amplifier bias circuit 30, a power amplifier stage 41, and a current source 75, each of which may be the same as or similar to those discussed above in connection with FIG. 5A or FIG. 5B. The power amplifier 130 further includes a bias impedance component 81 which includes a pair of FETs 91 and 92 in place of the single FET 90 of FIG. 5B. The control signal CTRL may be applied to the gate of each of the FETs 91 and 92 via respective resistors 95 and 97. Depending on the implementation, the use of two FETs 91 and 92 may increase the range of values for the impedance bias provided by the combination of the FETs 91 and 92 while maintaining the FETs 91 and 92 in triode. Although not illustrated in FIG. 10, a similarly structured circuit (including two FETs and input resistors) may be included in the power amplifier bias circuit to preserve the correct current mirror ratio.

[0067] FIG. 11 is a schematic block diagram of yet another example of a power amplifier system in accordance with aspects of this disclosure. The power amplifier 131 illustrated in FIG. 11 is similar to the power amplifier 130 illustrated in FIG. 10, except for the inclusion of three or more FETs 91 to 92 in the bias impedance component 81, where the

inclusion of additional FETs is illustrated by the ellipses. By including three or more FETs 91 to 92 in the bias impedance component 81, the range of bias impedance values that can be generated while maintaining the FETs 91 and 92 in triode increases. As described above in connection with FIG. 10, the same structure (including the same number of FETs and resistors) can be included in the power amplifier bias circuit to preserve the current mirror ratio.

Conclusion

[0068] Unless the context clearly requires otherwise, throughout the description and the claims, the words “comprise,” “comprising,” and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of “including, but not limited to.” The word “coupled”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word “connected”, as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words “herein,” “above,” “below,” and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word “or” in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0069] Moreover, conditional language used herein, such as, among others, “can,” “could,” “might,” “e.g.,” “for example,” “such as” and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0070] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0071] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0072] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

Claims

1. A power amplifier system, comprising:
a bias circuit configured to receive a bias voltage and generate a bias signal;
a power amplifier stage configured to receive an input radio frequency signal and generate an output radio frequency signal; and
a bias impedance component operatively coupled between the bias circuit and the power amplifier stage, the bias impedance component including a transistor configured to receive a control signal and adjust an impedance value of the transistor in response to the control signal, the bias impedance component configured to apply the impedance value of the transistor to bias the power amplifier stage, the control signal being received separately from the bias circuit.
2. THE POWER AMPLIFIER SYSTEM OF CLAIM 1 WHEREIN THE CONTROL SIGNAL HAS A VOLTAGE CONFIGURED TO OPERATE THE TRANSISTOR IN A TRIODE REGION OF THE TRANSISTOR.
3. THE POWER AMPLIFIER SYSTEM OF CLAIM 2 WHEREIN THE TRANSISTOR INCLUDES A FIELD EFFECT TRANSISTOR AND THE POWER AMPLIFIER INCLUDES A HETEROJUNCTION BIPOLAR TRANSISTOR CONFIGURED TO AMPLIFY THE INPUT RADIO FREQUENCY SIGNAL.
4. THE POWER AMPLIFIER SYSTEM OF CLAIM 3 WHEREIN THE FIELD EFFECT TRANSISTOR AND THE HETEROJUNCTION BIPOLAR TRANSISTOR ARE FABRICATED ON A SINGLE SEMICONDUCTOR DIE.
5. THE POWER AMPLIFIER SYSTEM OF CLAIM 1 WHEREIN THE IMPEDANCE VALUE OF THE TRANSISTOR IS SELECTED SUCH THAT VARIATION IN A GAIN OF THE POWER AMPLIFIER STAGE IS LESS THAN A THRESHOLD VALUE FROM 0 DB/DM.
6. THE POWER AMPLIFIER SYSTEM OF CLAIM 1, FURTHER COMPRISING:
AN ADDITIONAL BIAS CIRCUIT CONFIGURED TO RECEIVE THE BIAS VOLTAGE AND GENERATE AN ADDITIONAL BIAS SIGNAL;
AN ADDITIONAL POWER AMPLIFIER STAGE CONFIGURED TO RECEIVE THE OUTPUT RADIO FREQUENCY SIGNAL FROM THE POWER AMPLIFIER STAGE AND GENERATE AN ADDITIONAL RADIO FREQUENCY OUTPUT SIGNAL; AND

AN ADDITIONAL BIAS IMPEDANCE COMPONENT OPERATIVELY COUPLED BETWEEN THE ADDITIONAL BIAS CIRCUIT AND THE ADDITIONAL POWER AMPLIFIER STAGE, THE ADDITIONAL BIAS IMPEDANCE COMPONENT CONFIGURED TO RECEIVE AN ADDITIONAL CONTROL SIGNAL AND ADJUST AN IMPEDANCE VALUE OF THE ADDITIONAL BIAS IMPEDANCE COMPONENT IN RESPONSE TO THE ADDITIONAL CONTROL SIGNAL.

7. THE POWER AMPLIFIER SYSTEM OF CLAIM 6, WHEREIN THE IMPEDANCE VALUE OF THE TRANSISTOR AND THE IMPEDANCE VALUE OF THE ADDITIONAL BIAS IMPEDANCE COMPONENT ARE SELECTED SUCH THAT VARIATION IN AN OVERALL GAIN OF THE POWER AMPLIFIER STAGE AND THE ADDITIONAL POWER AMPLIFIER STAGE IS LESS THAN A THRESHOLD VALUE FROM 0 DB/DM.

8. THE POWER AMPLIFIER SYSTEM OF CLAIM 1 FURTHER COMPRISING AN ADDITIONAL BIAS IMPEDANCE COMPONENT OPERATIVELY COUPLED BETWEEN THE BIAS IMPEDANCE COMPONENT AND THE POWER AMPLIFIER STAGE, THE ADDITIONAL BIAS IMPEDANCE COMPONENT CONFIGURED TO RECEIVE THE CONTROL SIGNAL AND ADJUST AN IMPEDANCE VALUE OF THE ADDITIONAL BIAS IMPEDANCE COMPONENT IN RESPONSE TO THE CONTROL SIGNAL.

9. THE POWER AMPLIFIER SYSTEM OF CLAIM 1 WHEREIN THE POWER AMPLIFIER STAGE IS CONFIGURED TO GENERATE THE OUTPUT RADIO FREQUENCY SIGNAL HAVING A FIRST CURRENT, THE BIAS CIRCUIT CONFIGURED TO GENERATE THE BIAS SIGNAL HAVING A SECOND CURRENT THAT MIRRORS THE FIRST CURRENT.

10. A METHOD OF ADJUSTING A GAIN OF A POWER AMPLIFIER STAGE, COMPRISING:
RECEIVING, AT A BIAS CIRCUIT, A BIAS VOLTAGE;
GENERATING, BY THE BIAS CIRCUIT, A BIAS SIGNAL BASED ON THE BIAS VOLTAGE;
RECEIVING, AT A BIAS IMPEDANCE COMPONENT, THE BIAS VOLTAGE AND A CONTROL SIGNAL, THE BIAS IMPEDANCE COMPONENT INCLUDING A TRANSISTOR, THE CONTROL SIGNAL BEING RECEIVED SEPARATELY FROM THE BIAS CIRCUIT;
ADJUSTING, AT THE BIAS IMPEDANCE COMPONENT, AN IMPEDANCE VALUE OF

THE TRANSISTOR BASED ON THE RECEIVED CONTROL SIGNAL;
APPLYING THE IMPEDANCE VALUE OF THE TRANSISTOR TO THE BIAS VOLTAGE:
RECEIVING, AT A POWER AMPLIFIER STAGE, AN INPUT RADIO FREQUENCY SIGNAL
AND THE BIAS VOLTAGE FROM THE BIAS IMPEDANCE COMPONENT; AND
GENERATING AN OUTPUT RADIO FREQUENCY SIGNAL BASED ON THE INPUT
RADIO FREQUENCY SIGNAL AND THE BIAS VOLTAGE.

11. THE METHOD OF CLAIM 10 WHEREIN THE CONTROL SIGNAL HAS A VOLTAGE
CONFIGURED TO OPERATE THE TRANSISTOR IN A TRIODE REGION OF THE
TRANSISTOR.

12. THE METHOD OF CLAIM 11 WHEREIN THE TRANSISTOR INCLUDES A FIELD
EFFECT TRANSISTOR AND THE POWER AMPLIFIER INCLUDES A HETEROJUNCTION
BIPOLAR TRANSISTOR, THE METHOD FURTHER COMPRISING AMPLIFYING, AT THE
HETEROJUNCTION BIPOLAR TRANSISTOR, THE INPUT RADIO FREQUENCY SIGNAL.

13. THE METHOD OF CLAIM 12 WHEREIN THE FIELD EFFECT TRANSISTOR AND THE
HETEROJUNCTION BIPOLAR TRANSISTOR ARE FABRICATED ON A SINGLE
SEMICONDUCTOR DIE.

14. THE METHOD OF CLAIM 10 FURTHER COMPRISING SELECTING A VOLTAGE OF
THE CONTROL SIGNAL TO PRODUCE THE IMPEDANCE VALUE OF THE TRANSISTOR
SUCH THAT VARIATION IN A GAIN OF THE POWER AMPLIFIER STAGE IS LESS THAN
A THRESHOLD VALUE FROM 0 DB/DM.

15. THE METHOD OF CLAIM 10 FURTHER COMPRISING:
RECEIVING, AT AN ADDITIONAL BIAS IMPEDANCE COMPONENT, THE BIAS
VOLTAGE FROM THE BIAS IMPEDANCE COMPONENT AND THE CONTROL SIGNAL;
AND
ADJUSTING, AT THE ADDITIONAL BIAS IMPEDANCE COMPONENT, AN IMPEDANCE
VALUE OF THE ADDITIONAL BIAS IMPEDANCE COMPONENT BASED ON THE
RECEIVED CONTROL SIGNAL, THE ADDITIONAL BIAS IMPEDANCE COMPONENT
OPERATIVELY COUPLED BETWEEN THE BIAS IMPEDANCE COMPONENT AND THE
AMPLIFIER STAGE.

16. A MOBILE DEVICE, COMPRISING:

A POWER AMPLIFIER CONFIGURED TO AMPLIFY AN INPUT RADIO FREQUENCY SIGNAL AND GENERATE AN OUTPUT RADIO FREQUENCY SIGNAL; AND

A MODULATOR CONFIGURED TO GENERATE A RADIO FREQUENCY TRANSMIT SIGNAL BASED ON THE OUTPUT RADIO FREQUENCY SIGNAL,

THE POWER AMPLIFIER INCLUDING A BIAS CIRCUIT CONFIGURED TO RECEIVE A BIAS VOLTAGE AND GENERATE A BIAS SIGNAL, A POWER AMPLIFIER STAGE

CONFIGURED TO RECEIVE THE INPUT RADIO FREQUENCY SIGNAL AND GENERATE THE OUTPUT RADIO FREQUENCY SIGNAL, AND A BIAS IMPEDANCE COMPONENT

OPERATIVELY COUPLED BETWEEN THE BIAS CIRCUIT AND THE POWER AMPLIFIER STAGE, THE BIAS IMPEDANCE COMPONENT INCLUDING A TRANSISTOR

CONFIGURED TO RECEIVE A CONTROL SIGNAL AND ADJUST AN IMPEDANCE

VALUE OF THE TRANSISTOR IN RESPONSE TO THE CONTROL SIGNAL, THE BIAS

IMPEDANCE COMPONENT CONFIGURED TO APPLY THE IMPEDANCE VALUE OF THE

TRANSISTOR TO BIAS THE POWER AMPLIFIER STAGE, THE POWER AMPLIFIER

FURTHER INCLUDES AN ADDITIONAL BIAS IMPEDANCE COMPONENT OPERATIVELY COUPLED BETWEEN THE BIAS IMPEDANCE COMPONENT AND THE POWER

AMPLIFIER STAGE, THE ADDITIONAL BIAS IMPEDANCE COMPONENT CONFIGURED

TO RECEIVE THE CONTROL SIGNAL AND ADJUST AN IMPEDANCE VALUE OF THE

ADDITIONAL BIAS IMPEDANCE COMPONENT IN RESPONSE TO THE CONTROL

SIGNAL.

17. THE MOBILE DEVICE OF CLAIM 16 WHEREIN THE CONTROL SIGNAL HAS A VOLTAGE CONFIGURED TO OPERATE THE TRANSISTOR IN A TRIODE REGION OF THE TRANSISTOR.

18. THE MOBILE DEVICE OF CLAIM 17 WHEREIN THE TRANSISTOR INCLUDES A FIELD EFFECT TRANSISTOR AND THE POWER AMPLIFIER INCLUDES A HETEROJUNCTION BIPOLAR TRANSISTOR CONFIGURED TO AMPLIFY THE INPUT RADIO FREQUENCY SIGNAL.

19. THE MOBILE DEVICE OF CLAIM 18 WHEREIN THE FIELD EFFECT TRANSISTOR AND THE HETEROJUNCTION BIPOLAR TRANSISTOR ARE FABRICATED ON A SINGLE

SEMICONDUCTOR DIE.

20. THE MOBILE DEVICE OF CLAIM 16 WHEREIN THE IMPEDANCE VALUE OF THE TRANSISTOR IS SELECTED SUCH THAT VARIATION IN A GAIN OF THE POWER AMPLIFIER STAGE IS LESS THAN A THRESHOLD VALUE FROM 0 DB/DM.