

Mixer Circuit And Mixer Circuit Arrangement

[01] The present application claims the benefit of United States provisional application 60/863,732 (filed on 31 October 2006), the entire contents of which are incorporated herein by reference for all purposes.

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Field of the invention

[02] This invention relates to a mixer circuit and a mixer circuit arrangement.

Background of the invention

10 [03] In a MB-OFDM UWB (Multi-Band Orthogonal Frequency Division Multiplexing Ultra-Wide Band) spectrum, one of the challenges is to design a frequency synthesiser that can generate multiple carriers which can span across several GHz, with the ability to hop frequencies in less than about 9.47ns. To avoid interference to Industrial, Scientific and Medical (ISM) applications using the frequencies of 2.4GHz and 5GHz, the
15 spurious tones of mixing output are required to be below -50dBc.

[04] Known multiplexers that switch channel frequencies have a high power consumption and occupy a larger silicon area due to the use of multiple phase-locked loops (PLL). Another known fast hopping channel frequency device makes use of the frequency conversion function of known SSB (Single Side Band) mixers. Fast frequency hopping
20 realized through known SSB mixers need auxiliary circuits to select the polarity of input signals to generate either up-side or down-side mixing output. Such auxiliary circuits include dc sources, inverting amplifiers, switches, ROM, DAC and so on, leading to a complex circuit structure. Such known SSB mixers are unable to maintain the purity of the generated carriers.

[05] There is thus a need for a SSB mixer circuit that addresses one or more of the above problems.

Summary of the Invention

5 [06] In a first aspect of the invention, a mixer circuit is provided, comprising: a voltage-to-current converter stage; a switching stage comprising a plurality of switches, the switching stage being coupled with the voltage-to-current converter stage to controlled passing electrical current from the voltage-to-current converter stage through the switches; and a frequency conversion stage coupled to the switching stage.

10 [07] In a second aspect of the invention, a mixer circuit is provided, comprising: a voltage-to-current converter stage; a switching stage comprising a plurality of switches, the switching stage being coupled with the voltage-to-current converter stage to controlled passing electrical current from the voltage-to-current converter stage through the switches; and a frequency conversion stage coupled to the switching stage.

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Brief Description of the Drawings

[08] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference

20 to the following drawings, in which:

[09] Figure 1A shows a block level representation of the architecture of a SSB mixer circuit built in accordance to a first embodiment of the present invention.

- [10] Figure 1B shows a block level representation of the architecture of a SSB mixer circuit built in accordance to a second embodiment of the present invention.
- [11] Figure 2 shows the frequency spectrum of a MB-OFDM UWB.
- [12] Figure 3 shows a block level representation of the architecture for a MB-OFDM UWB system according to an embodiment of the present invention.
- [13] Figure 4A shows a circuit level implementation of the SSB mixer circuit.
- [14] Figure 4B shows digital logic used to generate various switching signals.
- [15] Figure 4C shows a π network optimization of switches in the load adjusting stage of the SSB mixer circuit.
- [16] Figure 5 shows a graph illustrating the switching time required for the three operation modes of the SSB mixer circuit.
- [17] Figure 6 illustrates the output spectrum of VOP and VON when the SSB mixer circuit is operating in a down-converter mode.
- [18] Figure 7 illustrates the output spectrum of VOP and VON when the SSB mixer circuit is operating in an up-converter mode.
- [19] Figure 8 illustrates the output spectrum of VOP and VON when the SSB mixer circuit is operating in the amplifier mode.
- [20] Figure 9 shows a die microphotograph of a tri-mode SSB mixer circuit fabricated onto a silicon substrate.
- [21] Figure 10 shows the output spectrum of a fabricated circuit operating in the down-converter mode.
- [22] Figure 11 shows the output spectrum of the fabricated circuit operating in the amplifier mode.
- [23] Figure 12 illustrates the frequency hopping performance of the fabricated circuit switched from the amplifier operating mode to the down-converter operating mode.

[24] Figure 13 summarizes the performance of the fabricated circuit.

Detailed Description

[25] As used herein the terms connected and coupled are intended to include both
5 direct and indirect connection and coupling, respectively.

[26] Exemplary embodiments of a Single Side Band (SSB) mixer circuit for fast
frequency hopping carrier generation in a Multi-Band Orthogonal Frequency Division
Multiplexing Ultra-Wide Band (MB-OFDM UWB) system are described in detail below
with reference to the accompanying figures. It will be appreciated that the exemplary
10 embodiments described below can be modified in various aspects without changing the
essence of the invention.

[27] Figure 1A shows a block level representation of the architecture of a SSB
mixer circuit 100 built in accordance to a first embodiment of the present invention, for a
MB-OFDM UWB system. The architecture of the SSB mixer circuit 100 includes the
15 following functional blocks, namely a voltage-to-current converter stage 102, a switching
stage 104, a frequency conversion stage 106 and a controlled passing electrical current
110. The switching stage 104 includes a plurality of switches 108, where the switching
stage 104 is coupled with the voltage-to-current converter stage 102 to the controlled
passing electrical current 110 through the plurality of switches 108. The frequency
20 conversion stage 106 is coupled to the switching stage 104.

[28] In use, the voltage-to-current converter stage 102 will convert around 528MHz
frequency band spacing input voltage signals 116 to current signals. The voltage-to-
current converter stage 102 is also referred to as the transconductor stage. The switching
stage 108 controls the polarity of the differential current signal coupled to the frequency

conversion stage 106. Current switching ensures minimal signal loss and enables a faster frequency hopping function. At the same time, current switching provides a better isolation and hence much lower level of image frequency.

[29] The switching stage 104 serves to realize the frequency hopping function of the SSB mixer circuit 100 by selecting the polarity of the 528MHz current signals that are electrically communicated from the voltage-to-current converter stage 102 to the frequency conversion stage 106. Frequency hopping is effected by control signals 120, where the control signals 120 will in turn generate internal control signals (not shown), which will be further elaborated below with reference to Figure 4A. The frequency conversion stage 106 will receive a carrier frequency input 118 of around 3.96GHz, where the carrier frequency input 118 will be modulated by the 528 MHz current signals.

[30] Figure 1B shows a block level representation of the architecture of a SSB mixer circuit 128 built in accordance to a second embodiment of the present invention, for a MB-OFDM UWB system. The second embodiment includes a first mixer circuit 130 and a second mixer circuit 150.

[31] The architecture of the first mixer circuit 130 includes the following functional blocks, namely a voltage-to-current converter stage 132, a switching stage 134, a frequency conversion stage 136 and a controlled passing electrical current 140. The switching stage 134 includes a plurality of switches 138, where the switching stage 134 is coupled with the voltage-to-current converter stage 132 to the controlled passing electrical current 140 through the plurality of switches 138. The frequency conversion stage 136 is coupled to the switching stage 134.

[32] Similarly, the architecture of the second mixer circuit 150 includes the following functional blocks, namely a voltage-to-current converter stage 152, a switching stage 154, a frequency conversion stage 156 and a controlled passing electrical current

160. The switching stage 154 includes a plurality of switches 158, where the switching stage 154 is coupled with the voltage-to-current converter stage 152 to the controlled passing electrical current 160 through the plurality of switches 158. The frequency conversion stage 156 is coupled to the switching stage 154.

5 [33] The same input signals 116, 118 and 120 that are applied to the SSB mixer circuit 100 are also similarly applied to the SSB mixer circuit 128.

[34] In use, the voltage-to-current converter stages 132 and 152 will convert the around 528 MHz band spacing frequency input voltage signals 116 to current signals and each of the plurality of switches 138 and 158 will control the polarity of the differential
10 current signal coupled from the voltage-to-current converter stages 132 and 152 to the frequency conversion stages 136 and 156. The voltage-to-current converter stages 132 and 152 are also referred to as the transconductor stages. Current switching ensures minimal signal loss and enables a faster frequency hopping function. At the same time, current switching provides a better isolation and hence much lower level of frequency hopping.

15 [35] The switching stages 134 and 154 serve to realize the frequency hopping function of the SSB mixer circuit 128 by selecting the polarity of the 528MHz current signals that are electrically communicated from the voltage-to-current converter stages 132 and 152 to the respective frequency conversion stages 136 and 156. Frequency hopping is effected by the control signals 120. The frequency conversion stages 136 and 156 will
20 each receive the carrier frequency input 118 of around 3.96GHz, where the carrier frequency input 118 will be modulated by the 528 MHz current signals.

[36] A circuit level implementation of the SSB mixer circuit 128 will be described later, with reference to Figure 4A.

[37] Figure 2 shows the frequency spectrum 200 of the MB-OFDM UWB. The
25 spectrum 200 is divided into bands 202 that have a bandwidth of around 528MHz. The

SSB mixer circuit 100 (Figure 1) uses the frequency bands 202 that are within the first band group 210, where the carrier frequency 118 is around 3.96 GHz (3960MHz). The side bands 204 and 206 are both spaced around 528MHz from the carrier frequency 118, to define an upper side band 204 that has a frequency of around 4.488GHz and a lower side band 206 that has a frequency of around 3.432GHz.

[38] Figure 3 shows a block level representation of the architecture for the MB-OFDM UWB system 300 according to an embodiment of the present invention, where the objective is to have a fast frequency hopping circuit where the hopping time between the different frequencies within a band group is less than about 9.47ns and where the output of the desired frequencies have spurious tones that are below -50dBc.

[39] The architecture of the system 300 includes the following functional blocks, a first phase locked loop (PLL) frequency synthesiser 302 operating at around 7920MHz, a second phase locked loop (PLL) frequency synthesiser 304 operating at around 1056MHz and the SSB mixer circuit 128. The first and second synthesizers 302 and 304 are coupled to the SSB mixer circuit 128 via their respective frequency dividers 306 and phase trimmers 308.

[40] As a first input, the SSB mixer circuit 128 receives quadrature differential signal inputs 312 and in-phase differential signal inputs 314, both having a carrier frequency of around 3.96GHz, from the first PLL frequency synthesiser 302 after processing by the respective frequency divider 306 and phase trimmer 308. As a second input, the SSB mixer circuit 128 receives quadrature differential signal inputs 322 and in-phase differential signal inputs 324, both having a modulation frequency of around 528MHz, from the second PLL frequency synthesiser 306 after processing by the respective frequency divider 306 and phase trimmer 308.

[41] Depending on the 2-bit control signals 120, the output 310 from the SSB mixer circuit 128 facilitates fast frequency hopping capability to generate one of the three output frequencies 310 of around 3.432GHz, around 3.96GHz or around 4.488GHz. Compared with known MB-OFDM UWB systems, the MB-OFDM UWB system 300 can be realized with fewer PLL frequency synthesizers, thus avoiding signal leakage occurring in the multiple paths used in multiplexers present in the known MB-OFDM UWB system. Further, as the frequency hopping is achieved using switches 138 and 158 that are integrated into the SSB mixer circuit 128, the architectural complexity of the SSB mixer circuit 128 is reduced when compared with known SSB mixers that require auxiliary circuitry to achieve the frequency hopping function.

[42] Figure 4A shows the circuit level implementation of the SSB mixer circuit 128 of Figure 1B.

[43] The first mixer circuit 130 and the second mixer circuit 150 are double balanced and have a symmetrical arrangement with each other, implemented by a plurality of transistors (M1 to M24) that are suitably connected, as described in further detail below.

[44] The plurality of transistors of the voltage-to-current converter stage 132 of the first mixer circuit 130 includes a first transistor M1, a second transistor M2, a third transistor M3 and a fourth transistor M4. Control terminals M1_G, M2_G, M3_G and M4_G of the first, second, third and fourth transistors, M1 to M4, are respectively coupled to a supply voltage V_{DC}, a first differential in-phase input signal having a first frequency I_{LO2+}, a second differential in-phase input signal having the first frequency I_{LO2-}; and the supply voltage V_{DC}.

[45] The plurality of transistors of the voltage-to-current converter stage 152 of the second mixer circuit 150 includes a ninth transistor M5, a tenth transistor M6, an eleventh transistor M7 and a twelfth transistor M8. Control terminals M5_G, M6_G, M7_G and M8_G of

the ninth, tenth, eleventh and twelfth transistors, M5-M8 are respectively coupled to a first differential quadrature input signal having a first frequency Q_LO2+ , a second differential quadrature input signal having the first frequency Q_LO2- , the second differential quadrature input signal having the first frequency Q_LO2- and the first differential quadrature input signal having the first frequency Q_LO2+ .

[46] Each of the voltage-to-current converter stages 132 and 152 includes a resistor R1 and R2 respectively, where the resistor R1 and R2 can be a variable resistor.

[47] The resistor R1 of the voltage-to-current converter stage 132 of the first mixer circuit 130 is connected between a first controlled terminal $M2_S$ of the second transistor M2 and a first controlled terminal $M3_S$ of the third transistor M3.

[48] The resistor R2 of the voltage-to-current converter stage 152 of the second mixer circuit 150 is connected between a first controlled terminal $M6_S$ of the tenth transistor M6 and a first controlled terminal $M7_S$ of the eleventh transistor M7.

[49] A first controlled terminal $M1_S$ of the first transistor M1 is coupled with the first controlled terminal $M2_S$ of the second transistor M2. Further, the first controlled terminal $M1_S$ of the first transistor M1 and the first controlled terminal $M2_S$ of the second transistor M2 are coupled with a node reference potential 402.

[50] The first controlled terminal $M3_S$ of the third transistor M3 is coupled with a first controlled terminal $M4_S$ of the fourth transistor M4. Further, the first controlled terminal $M3_S$ of the third transistor M3 and the first controlled terminal $M4_S$ of the fourth transistor M2 are coupled with a node reference potential 404.

[51] A first controlled terminal $M5_S$ of the ninth transistor M5 is coupled with the first controlled terminal $M6_S$ of the tenth transistor M6. Further, the first controlled terminal $M5_S$ of the ninth transistor M5 and the first controlled terminal $M6_S$ of the tenth transistor M6 are coupled with a node reference potential 406.

[52] The first controlled terminal $M7_S$ of the eleventh transistor M7 is coupled with a first controlled terminal $M8_S$ of the twelfth transistor M8. Further, the first controlled terminal $M7_S$ of the eleventh transistor M7 and the first controlled terminal $M8_S$ of the twelfth transistor M8 are coupled with a node reference potential 408.

5 [53] In the SSB mixer circuit 128, the nodes reference potentials 402, 404, 406 and 408 are electrical connection points which are respectively connected to reference potential GND through controlled passing electrical current sources 140A, 140B, 160A and 160B.

[54] Turning to the switching stages 134 and 154, the switching stage 134 of the
10 first mixer circuit 130 includes a plurality of switches 138, while the switching stage 154 of the second mixer circuit 150 includes a plurality of switches 158. In the SSB mixer circuit 128, the switches 138 and 158 include transistors M9 – M16.

[55] The plurality of switches 138 of the first mixer circuit 130 includes a first switch M9, a second switch M10, a third switch M11 and a fourth switch M12.

15 [56] Control terminals $M9_G$, $M10_G$, $M11_G$ and $M12_G$ of the first, second, third and fourth switches, M9 - M 12 are respectively coupled to a fourth switching signal sw4, a fifth switching signal sw5, the fifth switching signal sw5 and the reference potential GND.

[57] A first controlled terminal $M9_S$ of the first switch M9 is coupled with a second controlled terminal $M1_D$ of the first transistor M1. A first controlled terminal $M10_S$ of the
20 second switch M10 is coupled with a second controlled terminal $M2_D$ of the second transistor M2. A first controlled terminal $M11_S$ of the third switch M11 is coupled with a second controlled terminal $M3_D$ of the third transistor M3. A first controlled terminal $M12_S$ of the fourth switch M12 is coupled with a second controlled terminal $M4_D$ of the fourth transistor M4.

[58] The plurality of switches 158 of the second mixer circuit 150 includes a fifth switch M13, a sixth switch M14, a seventh switch M15 and an eighth switch M16.

[59] Control terminals M13_G, M14_G, M15_G and M16_G of the fifth, sixth, seventh and eighth switches, M13 - M16 are respectively coupled to the first switching signal sw1, a
 5 second switching signal sw2, the first switching signal sw1 and the second switching signal sw2.

[60] A first controlled terminal M13_S of the fifth switch M13 is coupled with a second controlled terminal M5_D of the ninth transistor M5. A first controlled terminal M14_S of the sixth switch M14 is coupled with a second controlled terminal M6_D of the
 10 tenth transistor M6. A first controlled terminal M15_S of the seventh switch M15 is coupled with a second controlled terminal M7_D of the eleventh transistor M7. A first controlled terminal M16_S of the eighth switch M16 is coupled with a second controlled terminal M8_D of the twelfth transistor M8.

[61] The frequency conversion stages 136 and 156 include a plurality of transistors
 15 M17 - M24.

[62] The plurality of transistors M17 - M20 of the frequency conversion stage 136 of the first mixer circuit 130 includes a fifth transistor M17, a sixth transistor M18, a seventh transistor M19 and an eighth transistor M20.

[63] Control terminals M17_G, M18_G, M19_G and M20_G of the fifth, sixth, seventh and
 20 eighth transistors, M17 - M20, are respectively coupled to a first differential in-phase input signal having a second frequency I_{LO1+}, a second differential in-phase input signal having the second frequency I_{LO1-}, the second differential in-phase input signal having the second frequency I_{LO1-} and the first differential in-phase input signal having a second frequency I_{LO1+}.

[64] A first controlled terminal $M17_S$ of the fifth transistor $M17$ is coupled with a second controlled terminal $M9_D$ of the first switch $M9$. A first controlled terminal $M18_S$ of the sixth transistor $M18$ is coupled with a second controlled terminal $M10_D$ of the second switch $M10$. A first controlled terminal $M19_S$ of the seventh transistor $M19$ is coupled with a second controlled terminal $M11_D$ of the third switch $M11$. A first controlled terminal $M20_S$ of the eighth transistor $M20$ is coupled with a second controlled terminal $M12_D$ of the fourth switch $M12$.

[65] The plurality of transistors $M21 - M24$ of the frequency conversion stage 156 of the second mixer circuit 150 includes a thirteenth transistor $M21$, a fourteenth transistor $M22$, a fifteenth transistor $M23$ and a sixteenth transistor $M24$.

[66] Control terminals $M21_G$, $M22_G$, $M23_G$ and $M24_G$ of the thirteenth, fourteenth, fifteenth and sixteenth transistors, $M21 - M24$, are respectively coupled to a first differential quadrature input signal having a second frequency Q_{LO1+} , a second differential quadrature input signal having the second frequency Q_{LO1-} , the second differential quadrature input signal having the second frequency Q_{LO1-} ; and the first differential quadrature input signal having the second frequency Q_{LO1+} .

[67] A first controlled terminal $M21_S$ of the thirteenth transistor $M21$ is coupled with a second controlled terminal $M13_D$ of the fifth switch $M13$. A first controlled terminal $M22_S$ of the fourteenth transistor $M22$ is coupled with a second controlled terminal $M14_D$ of the sixth switch $M14$. A first controlled terminal $M23_S$ of the fifteenth transistor $M23$ is coupled with a second controlled terminal $M15_D$ of the seventh switch $M15$. A first controlled terminal $M24_S$ of the sixteenth transistor $M24$ is coupled with a second controlled terminal $M16_D$ of the eighth switch $M16$.

[68] The frequency conversion stage 136 of the first mixer circuit 130 includes a first output terminal 410 and a second output terminal 412. Similarly, the frequency

conversion stage 156 of the second mixer circuit 150 includes a first output terminal 418 and a second output terminal 416. In other words, each of the frequency conversion stages 136 and 156 comprises both a first output terminal (410 and 418) and a second output terminal (412 and 416) respectively.

5 [69] The first output terminal 410 of the frequency conversion stage 136 of the first mixer circuit 130 is coupled with the second output terminal 416 of the frequency conversion stage 156 of the second mixer circuit 150, while the second output terminal 412 of the frequency conversion stage 136 of the first mixer circuit 130 is coupled with the first output terminal 418 of the frequency conversion stage 156 of the second mixer circuit
10 150.

[70] A second controlled terminal M17_D of the fifth transistor M17 is coupled with the first output terminal 410 of the frequency conversion stage 136 of the first mixer circuit 130, while a second controlled terminal M18_D of the sixth transistor M18 is coupled with the second output terminal 412 of the frequency conversion stage 136 of the first
15 mixer circuit 130. A second controlled terminal M19_D of the seventh transistor M19 is coupled with the first output terminal 410 of the frequency conversion stage 136 of the first mixer circuit 130, while a second controlled terminal M20_D of the eighth transistor M20 is coupled with the second output terminal 412 of the frequency conversion stage 136 of the first mixer circuit 130.

20 [71] Turning to the second mixer circuit 150, a second controlled terminal M21_D of the thirteenth transistor M21 is coupled with the second output terminal 416 of the frequency conversion stage 156 of the second mixer circuit 150. A second controlled terminal M22_D of the fourteenth transistor M22 is coupled with the first output terminal 418 of the frequency conversion stage 156 of the second mixer circuit 150, while a second
25 controlled terminal M23_D of the fifteenth transistor M23 is coupled with the second output

terminal 416 of the frequency conversion stage of the second mixer circuit. A second controlled terminal $M24_D$ of the sixteenth transistor $M24$ is coupled with the first output terminal 418 of the frequency conversion stage 156 of the second mixer circuit 150.

[72] A first controlled terminal $M17_S$ of the fifth transistor $M17$ is coupled with a second controlled terminal $M9_D$ of the first switch $M9$. A first controlled terminal $M18_S$ of the sixth transistor $M18$ is coupled with a second controlled terminal $M10_D$ of the second switch $M10$. A first controlled terminal $M19_S$ of the seventh transistor $M19$ is coupled with a second controlled terminal $M11_D$ of the third switch $M11$. A first controlled terminal $M20_S$ of the eighth transistor $M20$ is coupled with a second controlled terminal $M12_D$ of the fourth switch $M12$.

[73] Each of the first mixer circuit 130 and the second mixer circuit 150 further includes a loading adjusting stage 438 and 458 to adjust the frequency response of the loading. The loading adjusting stage 438 of the first mixer circuit 130 is coupled with the first output terminal 410 of the first mixer circuit 130. The loading adjusting stage 458 of the second mixer circuit 150 is coupled with the first output terminal 418 of the second mixer circuit 150.

[74] Each of the loading adjusting stages 438 and 458 includes an inductance 424 and 426 coupled between the respective first output terminal 410 and 418 and a reference potential 420.

[75] In addition to the inductance 424, the loading adjusting stage 438 of the first mixer circuit 130 includes capacitors 428 and 432 that are coupled between the first output terminal 410 and the reference potential GND. Adjusting switches 436 and 442 are respectively coupled between the capacitors 428 and 432 and the reference potential GND.

[76] In addition to the inductance 420, the loading adjusting stage 458 of the second mixer circuit 150 includes capacitors 430 and 434 that are coupled between the first output

terminal 418 and the reference potential GND. Adjusting switches 440 and 444 are respectively coupled between the capacitors 430 and 434 and the reference potential GND.

[77] As such, each of the loading adjusting stages 438 and 458 includes at least one capacitance (428, 432, 430 and 444) coupled between the respective first output terminal
 5 410 and 418, and the reference potential GND. Each of the loading adjusting stages 438 and 458 include at least one adjusting switch (436, 442, 440 and 444) coupled between the at least one capacitance (428, 432, 430 and 444) and the reference potential GND.

[78] The inductor (424; 426)-capacitor (436, 432; 430, 434) tanks resonant
 10 frequencies are shifted with the respective loading adjusting stages 438 and 458 to maximize output signals at differential output nodes VOP and VON.

[79] In the SSB mixer circuit 128 of Figure 4A where the adjusting switches (436, 442, 440 and 444) are transistors, each of the loading adjusting stages (438 and 458) includes a first capacitance (428 and 430), a first adjusting switch (436 and 440), a second
 15 capacitance (432 and 434) and a second adjusting switch (442 and 444). A first terminal of the first capacitance (428 and 430) is coupled with the respective first output terminal (410 and 418). For the first adjusting switch (436 and 440), a first controlled terminal (436_S and 440_S) is coupled with the reference potential GND, a second controlled terminal (436_D and 440_D) is coupled with a respective second terminal of the first capacitance (428
 20 and 430), and a control input (436_G and 440_G) is coupled with the first switching signal sw1. A first terminal of the second capacitance (432 and 434) is coupled with the respective first output terminal (410 and 418). For the second adjusting switch (442 and 444), a first controlled terminal (442_S and 444_S) is coupled with the reference potential GND, a second controlled terminal (442_D and 444_D) is coupled with a respective second

terminal of the second capacitance (432 and 434), and a control input (442_G and 444_G) is coupled with the third switching signal sw3.

[80] I_{_LO1+} and I_{_LO1-} are the in-phase differential input carrier signals of frequency f₁ of around 3.96GHz, while Q_{_LO1+} and Q_{_LO1-} are the quadrature differential input carrier signals at the same frequency f₁ of around 3.96GHz. Similarly, I_{_LO2+} and I_{_LO2-} are the in-phase differential input modulation signals of frequency f₂ of around 528MHz, while Q_{_LO2+} and Q_{_LO2-} are the quadrature differential input modulation signals at the same frequency f₂ of around 528MHz. The supply voltage V_{_DC} is the bias voltage signal. A typical sample bias voltage is around 1.1V to around 1.35V. VOP and VON are the differential output nodes for the SSB mixer circuit 128, where VOP outputs the signal emitted from both the first output terminal 410 of the first mixer circuit 130 and the second output terminal 416 of the second mixer circuit 150, while VON outputs the signal emitted from both the first output terminal 418 of the second mixer circuit 150 and the second output terminal 412 of the first mixer circuit 130.

[81] The first switching signal sw1 and the second switching signal sw2 are 2-bit configuration signals, having logic levels "0" or "1". The switching signals sw1 and sw2 are used to control which of the three operation modes: an up-converter, a down-converter or an amplifier, the tri-mode SSB mixer circuit 128 will function in. Figure 4B shows digital logic 480 used to generate the switching signals sw1, sw2, sw3, sw4 and sw5 in the SSB mixer circuit 128 (Figure 4A). The digital logic 480 includes a NOR gate 482 and two NOT gates 484 and 486. The first and the second switching signals sw1 and sw2 are input into the NOR gate 482 while only the second switching signal sw2 is input into the NOT gate 484. The first and the second switching signals sw1 and sw2 generate the fourth switching signal sw4 at the output of the NOR gate 482, and the fourth switching signal sw4 is input into the NOT gate 486 to generate the fifth switching signal sw5 at the output

of the NOT gate 486. The second switching signal sw2 also generates the third switching signal sw3 at the output of the NOT gate 484.

[82] Returning to Figure 4A, setting the first switching signal to sw1=0 and the second switching signal to sw2=0, which in turn sets the third switching signal to sw3=1; the fourth switching signal sw4=1; and the fifth switching signal to sw5=0, will cause the tri-mode SSB mixer circuit 128 to operate as an amplifier to produce an amplified output frequency of f1, i.e. an amplified around 3.96GHz carrier signal, at the output terminals VOP and VON. The third switching signal sw3 is only used to shift the resonant peak of the respective inductor (424; 426)-capacitor (436, 432; 430, 434) tanks in the loading adjusting stages 438 and 458. In this manner, the third switching signal sw3 ensures maximum output swing appearing at the differential output nodes VOP and VON when the SSB mixer circuit 128 performs frequency band hopping.

[83] Setting the first switching signal to sw1=0 and the second switching signal to sw2=1, which in turn sets the third switching signal to sw3=0; the fourth switching signal sw4=0; and the fifth switching signal to sw5=1, will cause the tri-mode SSB mixer circuit 128 to operate in the up-converter mode to obtain an output signal of frequency (f1 + f2), i.e. an around 3.96GHz + 528MHz signal, at the output terminals VOP and VON .

[84] Setting the first switching signal to sw1=1 and the second switching signal to sw2=0, which in turn sets the third switching signal to sw3=1; the fourth switching signal sw4=0; and the fifth switching signal to sw5=1, will cause the tri-mode SSB mixer circuit 128 to operate in the down-converter mode to obtain an output signal of frequency (f1 - f2), i.e. an around (3.96GHz - 528MHz) signal, at the output terminals VOP and VON. The scenario where the first and the second switching signals are set to sw1=sw2=1 is not used in the tri-mode SSB mixer circuit 128. In the amplifier mode, the tri-mode SSB

mixer circuit 128 consumers half the current that is used in the other two modes, the up-converter and the down-converter modes.

[85] For the first channel 210 (Figure 2), the transistors M1 - M8, which form the voltage-to-current converter stages 132 and 152, convert input side bands 204 and 206 of around 528MHz input voltage signals to current signals. The transistors M17 - M24, which form the frequency conversion stages 136 and 156, realise the frequency conversion function of the tri-mode SSB mixer circuit 128 to switch the around 528MHz current signals across a load (not shown) using the 3.96GHz carrier frequency 118 (Figure 2).

[86] Transistors M9 - M16, which form the switching stages 134 and 154, function as means to realise the frequency hopping function of the tri-mode SSB mixer circuit 128. The transistors M9 - M16 select the polarity of the around 528MHz current signals that enter the transistors M17 to M24, based on the switching signals sw1 and sw2 (as earlier described with reference to the digital logic gate representational level 480), thereby controlling the signal output at the output terminals VOP and VON.

[87] As opposed to known SSB mixer systems which use auxiliary mixer circuitry, the switching stages 134 and 136 (implemented by cascading the transistors M9 - M16) are integrated into the tri-mode SSB mixer circuit 128. Also, different from known SSB mixer systems, the switching stages 134 and 136 are not used to switch voltage signals, but current signals. Current switching has the advantage of providing minimal signal loss and a faster frequency hopping performance. Current switching also achieves a better isolation performance and hence a lower level of image frequency. Cascading the various transistors, M9 - M16, further facilitates better isolation performance, while the symmetrical circuit arrangement of the SSB mixer circuit 128 further facilitates the lower level of image frequency by ensuring that the differential input signals (Q_LO1+ , Q_LO1- , I_LO1+ and I_LO1-) and (Q_LO2+ , Q_LO2- , I_LO2+ and I_LO2-) are well matched.

[88] Image rejection performance depends mainly on the phase mismatch and amplitude imbalance of input in-phase differential signals and quadrature differential input modulation signals. Thus, the double balanced structure and symmetry of the first mixer circuit 130 and the second mixer circuit 150 of the tri-mode SSB mixer circuit 128 minimize the probability of introducing phase and amplitude mismatch to the differential input modulation signals at frequency f_2 (around 528MHz), Q_LO2+ , Q_LO2- , I_LO2+ and I_LO2- , and the differential input carrier signals at frequency f_1 (around 3.96GHz) Q_LO1+ , Q_LO1- , I_LO1+ and I_LO1- . When the MB-OFDM UWB system 300 (Figure 3) employs the SSB mixer circuit 128, the phase trimmers 308 (Figure 3) serve to compensate any unavoidable residual amplitude and phase mismatch present in the SSB mixer circuit 128 and thus improve the image rejection performance of the tri-mode SSB mixer circuit 128. Thus, the tri-mode SSB mixer circuit 128 can obtain better image rejection performance. The symmetrical structure, degeneration resistance (not shown) in the transconductance (gm) (not shown) stage and good isolation performance ensure that the output of the desired frequencies have lower spurious tones when compared with conventional SSB mixers.

[89] As there is reduced switching losses in the input of the tri-mode SSB mixer circuit 128, the input swing for the differential input modulation signals at frequency f_2 (around 528MHz), Q_LO2+ , Q_LO2- , I_LO2+ and I_LO2- can be reduced. It will also be appreciated that the size of the transistors M9 – M16 can be carefully optimised, through known techniques, to obtain a compromise between hopping speed and limited voltage headroom.

[90] The inductors 424 and 426 in each of the loading adjusting stages 438 and 458 shunts the respective first adjusting switch (436, 440) – capacitor (428, 430) and the respective second adjusting switch (442, 432) – capacitor (432, 434) arrangements. Thus,

the response frequency of the loading adjusting stages 438 and 458 can be adjusted according to the output frequencies selected by the first and the second switching signals sw1 and sw2. In this way, maximum output swing and better sideband rejection is achieved. However, the conversion gain and frequency hopping selection of the tri-mode SSB mixer circuit 128 suffer from the decreased quality factor of the capacitors 428, 432, 430 & 434 due respectively to the adjusting switches 436, 442, 440 and 444. To alleviate this problem, the switches 436, 442, 440 and 444 are optimised in a π network 490 (also refer Figure 4C) to reduce the equivalent resistance, thus improving quality factor and hence the output signal level.

[91] The variable resistors R1 and R2, both having resistive values of 60 to 250 Ω , are used to adjust the conversion gain of the tri-mode SSB mixer circuit 128 to ensure that the performance is the same under various temperature and corner conditions.

[92] A simulation under ADS2004A with the SSB mixer circuit 128 being fabricated using Fujitsu 90nm CMOS technology was conducted. The simulation results are discussed with reference to Figures 5 to 8, where the carrier frequency, f_1 = around 3.96GHz and the modulation frequency, f_2 = around 528MHz.

[93] Figure 5 shows a graph 502 plotting the output (in volts) at VOP and VON of the SSB mixer circuit 128 (Figure 2) against time (in ns); and a graph 504 of a plot of the input (in volts) first and second switching signals sw1 and sw2 against time (in ns). The graph 502 shows the corresponding output VOP and VON in response to the first and second switching signals sw1 and sw2 shown in the graph 504.

[94] The transient simulation results of Figure 5 show the switching time required for the three operation modes: the up-converter ($f_1 + f_2$), the down-converter ($f_1 - f_2$) or the amplifier (f_1).

[95] When the first and the second switching signals change respectively from $sw1=1$ and $sw2=0$ to $sw1=0$ and $sw2=1$, the time needed for the output frequency signal to change from $(f1 - f2)$ to $(f1 + f2)$ is around 1.5ns, as indicated using reference numeral 506.

5 [96] When the second switching signal changes from $sw2=1$ to $sw2=0$, while the first switching signal remains at $sw1=0$, the time needed for the output frequency signal to change from $(f1 - f2)$ to $(f1)$ is around 2ns, as indicated using reference numeral 508.

[97] Figure 6 illustrates the output spectrum of VOP and VON when the SSB mixer circuit 128 (Figure 4A) is operating in the down-converter $(f1 - f2)$ mode. A graph 602
10 plots the output power of VOP and VON in dB against frequency in GHz. The graph 602 demonstrates that the output spectrum in the down converter $(f1 - f2)$ mode can achieve image rejection of around 50dB.

[98] Figure 7 illustrates the output spectrum of VOP and VON when the SSB mixer circuit 128 (Figure 4A) is operating in the up-converter $(f1 + f2)$ mode. A graph 702 plots
15 the output power of VOP and VON in dB against frequency in GHz. The graph 702 demonstrates that the output spectrum in the up-converter $(f1 + f2)$ mode can achieve image rejection of around 50dB.

[99] Figure 8 illustrates the output spectrum of VOP and VON when the SSB mixer circuit 128 (Figure 4A) is operating in the amplifier $(f1)$ mode. A graph 802 plots the
20 output power of VOP and VON in dB against frequency in GHz. The graph 802 demonstrates that the carrier frequency $f1$ of around 3.96 GHz (see m1) is amplified a greater extent than the other respective side band frequencies m3 and m2 of 3.432GHz and 4.488GHz.

[100] The above simulation results demonstrate that the tri-mode SSB mixer circuit 128 (Figure 4A) can switch output frequencies in less than 9ns to meet the specification for a fast switching multi-band UWB system.

[101] Figure 9 shows a die microphotograph of the tri-mode SSB mixer circuit 128 (Figure 4A) implemented with Fujitsu 90nm CMOS technology fabricated onto a silicon substrate through known methods to those skilled in the art. Prior to fabrication, the parasitic parameter of the physical layout was carefully estimated which included modelling important on-chip traces.

[102] The die size of the core circuit 900 is $2 \times 1.8 \text{mm}^2$.

[103] To obtain better device matching performance, the core circuit 900 has symmetrical matching layouts 902 and 904. Portions 906 and 912 respectively designate the input signal paths for the quadrature differential signals and the in-phase differential signals, both signals being of band spacing frequency at around 528MHz. The corresponding input pads for the portions 906 and 912 are designated 906a and 912a respectively. Portions 908 and 914 respectively designate the input signal paths for the quadrature differential signals and the in-phase differential signals, both signals being of carrier frequency at around 3.96GHz. The corresponding input pads for the portions 908 and 914 are designated 908a and 914a respectively. Portion 920 designates the output pads for the core circuit 900. Portion 910 designates signal paths for calibration bits. Portion 916 designates signal paths for first and second switching signals sw1 and sw2 (Figure 4A). Portion 918 designates the circuitry for the adjusting switch – capacitor arrangements in the loading adjusting stages 438 (Figure 4A) and 458 (Figure 4A).

[104] The tri-mode SSB mixer in the core circuit 900 draws about 7mA under an about 1.2V supply. The voltage supply can be adjusted from about 1.1V to about 1.35V with an operating temperature from about -40 °C to about 85 °C.

[105] The results of tests conducted on the fabricated circuit 900 are discussed with reference to Figures 10 to 13, where a carrier frequency, f_1 = around 3.96GHz and a modulation frequency, f_2 = around 528MHz were used.

[106] Figure 10 shows the output spectrum of the fabricated circuit 900 (Figure 9) when the tri-mode SSB mixer is operating in the down-converter mode. The output spectrum is a graph 1000 of output power against frequency, where the desired output 1002 frequency is at around 3.432GHz. The measured image rejection 1008 achieves up to 67dBc using externally phase trimmed quadrature input signals. As the second band 1004 (or LO) leakage at frequency around 3.96GHz is better than -35dBc and the third 10 harmonic spurious level 1006 at around 5.544GHz is -54dBc, WLAN 802.11a applications are not affected.

[107] Figure 11 shows the output spectrum of the fabricated circuit 900 (Figure 9) when the tri-mode SSB mixer is operating in the amplifier mode. The output spectrum is a graph 1100 of output power against frequency, where a 3.96GHz carrier signal 1102 is 15 generated. In the amplifier mode, the consumption current is reduced to around 3.5mA. The spur 1104 located at 3.432GHz is as low as -64dBc.

[108] For the third band application (Figure not shown), the measured image rejection performance of the up converted output is about -50dBc, while the LO leakage at around 3.96GHz level is -35dBc. The third harmonic spurious level at around 2.374GHz is 20 only -53dBc.

[109] Figure 12 illustrates the frequency hopping performance of the fabricated circuit 900 (Figure 9) when the tri-mode SSB mixer is switched from the amplifier operating mode to the down-converter operating mode. The hopping time 1202 is less than 1ns which is well below the requirement for a MB-OFDM UWB system.

[110] The performance summary of the fabricated circuit 900 (Figure 9) is tabulated 1302 as shown in Figure 13. The measured results demonstrate that the tri-mode SSB mixer circuit 128 (Figure 4A) has good linearity and fast frequency hopping performance for MB-OFDM UWB applications.

5 [111] From the results presented with reference to Figures 10 to 13, it will be observed that the performance of the actual fabricated circuit 900 agrees well with the simulation results discussed earlier with reference to Figures 5 to 8.

[112] While embodiments of the invention have been particularly shown and described with reference to specific embodiments, it should be understood by those skilled
10 in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

Claims

What is claimed is:

1. A mixer circuit, comprising:
 - 5 a voltage-to-current converter stage;
 - a switching stage comprising a plurality of switches, the switching stage being coupled with the voltage-to-current converter stage to controlled passing electrical current from the voltage-to-current converter stage through the switches; and
 - 10 a frequency conversion stage coupled to the switching stage.
2. The mixer circuit of claim 1,
wherein the voltage-to-current converter stage comprises a plurality of transistors.
- 15 3. The mixer circuit of claim 2,
wherein the plurality of transistors comprises:
 - a first transistor, a control terminal of which is coupled to a supply voltage;
 - 20 a second transistor, a control terminal of which is coupled to a first differential in-phase input signal having a first frequency;
 - a third transistor, a control terminal of which is coupled to a second differential in-phase input signal having the first frequency;

a fourth transistor, a control terminal of which is coupled to the supply voltage.

4. The mixer circuit of claim 1,
5 wherein the voltage-to-current converter stage comprises a resistor.
5. The mixer circuit of claim 4,
wherein the resistor is a variable resistor.
- 10 6. The mixer circuit of claim 3 and claim 4,
wherein the resistor is connected between a first controlled terminal of the second transistor and a first controlled terminal of the third transistor.
7. The mixer circuit of claim 3,
15 wherein a first controlled terminal of the first transistor is coupled with a first controlled terminal of the second transistor.
8. The mixer circuit of claim 7,
wherein the first controlled terminal of the first transistor and the first
20 controlled terminal of the second transistor are coupled with a reference potential.
9. The mixer circuit of claim 3,
wherein a first controlled terminal of the third transistor is coupled with a first
25 controlled terminal of the fourth transistor.

10. The mixer circuit of claim 9,
wherein the first controlled terminal of the third transistor and the first
controlled terminal of the fourth transistor are coupled with a reference
5 potential.
11. The mixer circuit of claim 1,
wherein the switches comprise one or more transistors.
- 10 12. The mixer circuit of claim 1,
wherein the plurality of switches comprises:
a first switch, a control terminal of which is coupled to a fourth
switching signal;
a second switch, a control terminal of which is coupled to a fifth
15 switching signal;
a third switch, a control terminal of which is coupled to the fifth
switching signal;
a fourth switch, a control terminal of which is coupled to a reference
potential.
- 20 13. The mixer circuit of claim 3 and claim 12,
wherein
a first controlled terminal of the first switch is coupled with a second
controlled terminal of the first transistor;

a first controlled terminal of the second switch is coupled with a second controlled terminal of the second transistor;

a first controlled terminal of the third switch is coupled with a second controlled terminal of the third transistor;

5 a first controlled terminal of the fourth switch is coupled with a second controlled terminal of the fourth transistor.

14. The mixer circuit of claim 1,
wherein the frequency conversion stage comprises a plurality of transistors.

10

15. The mixer circuit of claim 14,
wherein the plurality of transistors comprises:

a fifth transistor, a control terminal of which is coupled to a first differential in-phase input signal having a second frequency;

15 a sixth transistor, a control terminal of which is coupled to a second differential in-phase input signal having the second frequency;

a seventh transistor, a control terminal of which is coupled to the second differential in-phase input signal having the second frequency;

20 an eighth transistor, a control terminal of which is coupled to the first differential in-phase input signal having a second frequency.

16. The mixer circuit of claim 15,
wherein

25 a first controlled terminal of the fifth transistor is coupled with a second controlled terminal of the first switch;

a first controlled terminal of the sixth transistor is coupled with a second controlled terminal of the second switch;

a first controlled terminal of the seventh transistor is coupled with a second controlled terminal of the third switch;

5 a first controlled terminal of the eighth transistor is coupled with a second controlled terminal of the fourth switch.

17. The mixer circuit of claim 1,

wherein the frequency conversion stage comprises a first output terminal and a
10 second output terminal.

18. The mixer circuit of claim 16 and claim 17,

wherein

a second controlled terminal of the fifth transistor is coupled with the
15 first output terminal;

a second controlled terminal of the sixth transistor is coupled with the second output terminal;

a second controlled terminal of the seventh transistor is coupled with the first output terminal;

20 a second controlled terminal of the eighth transistor is coupled with the second output terminal.

19. The mixer circuit of claim 17, further comprising:

a loading adjusting stage to adjust the frequency response of the loading;

25 wherein the loading adjusting stage is coupled with the first output terminal.

20. The mixer circuit of claim 17,
wherein the loading adjusting stage comprises an inductance coupled between
the first output terminal and a reference potential.
- 5
21. The mixer circuit of claim 17,
wherein the loading adjusting stage comprises at least one capacitance coupled
between the first output terminal and another reference potential.
- 10 22. The mixer circuit of claim 21,
wherein the loading adjusting stage comprises at least one adjusting switch
coupled between the at least one capacitance and the other reference potential.
23. The mixer circuit of claim 17,
15 wherein the loading adjusting stage comprises
a first capacitance, a first terminal of which is coupled with the first
output terminal;
a first adjusting switch,
a first controlled terminal of which is coupled with the other
20 reference potential;
a second controlled terminal of which is coupled with a second
terminal of the first capacitance;
a control input of which is coupled with a first switching signal;
a second capacitance, a first terminal of which is coupled with the first
25 output terminal;

a second adjusting switch,

a first controlled terminal of which is coupled with the other
reference potential;

a second controlled terminal of which is coupled with a second
terminal of the second capacitance;

a control input of which is coupled with a third switching
signal.

24. A mixer circuit arrangement, comprising:

a first mixer circuit, comprising:

a voltage-to-current converter stage;

a switching stage comprising a plurality of switches, the switching
stage being coupled with the voltage-to-current converter stage to
controlled passing electrical current from the voltage-to-current
converter stage through the switches; and

a frequency conversion stage coupled to the switching stage;

a second mixer circuit, comprising:

a voltage-to-current converter stage;

a switching stage comprising a plurality of switches, the switching
stage being coupled with the voltage-to-current converter stage to
controlled passing electrical current from the voltage-to-current
converter stage through the switches; and

a frequency conversion stage coupled to the switching stage.

25. The mixer circuit arrangement of claim 24,

wherein each voltage-to-current converter stage of the voltage-to-current converter stages comprises a plurality of transistors.

26. The mixer circuit arrangement of claim 25,

5 wherein the plurality of transistors of the voltage-to-current converter stage of the first mixer circuit comprises:

a first transistor, a control terminal of which is coupled to a supply voltage;

10 a second transistor, a control terminal of which is coupled to a first differential in-phase input signal having a first frequency;

a third transistor, a control terminal of which is coupled to a second differential in-phase input signal having the first frequency;

a fourth transistor, a control terminal of which is coupled to the supply voltage.

15

27. The mixer circuit arrangement of claim 25,

wherein the plurality of transistors of the voltage-to-current converter stage of the second mixer circuit comprises:

20 a ninth transistor, a control terminal of which is coupled to a first differential quadrature input signal having a first frequency;

a tenth transistor, a control terminal of which is coupled to a second differential quadrature input signal having the first frequency;

an eleventh transistor, a control terminal of which is coupled to the second differential quadrature input signal having the first frequency;

a twelfth transistor, a control terminal of which is coupled to the first differential quadrature input signal having the first frequency.

28. The mixer circuit arrangement of claim 24,
5 wherein each voltage-to-current converter stage of the voltage-to-current converter stages comprises a resistor.
29. The mixer circuit arrangement of claim 28,
wherein the resistors are variable resistors.
- 10 30. The mixer circuit arrangement of claim 26, claim 27 and claim 28,
wherein the resistor of the voltage-to-current converter stage of the first mixer circuit is connected between a first controlled terminal of the second transistor and a first controlled terminal of the third transistor;
15 wherein the resistor of the voltage-to-current converter stage of the second mixer circuit is connected between a first controlled terminal of the tenth transistor and a first controlled terminal of the eleventh transistor;
31. The mixer circuit arrangement of claim 26,
20 wherein a first controlled terminal of the first transistor is coupled with a first controlled terminal of the second transistor.
32. The mixer circuit arrangement of claim 31,

wherein the first controlled terminal of the first transistor and the first controlled terminal of the second transistor are coupled with a reference potential.

5 33. The mixer circuit arrangement of claim 26,
wherein a first controlled terminal of the third transistor is coupled with a first controlled terminal of the fourth transistor.

34. The mixer circuit arrangement of claim 33,
10 wherein the first controlled terminal of the third transistor and the first controlled terminal of the fourth transistor are coupled with a reference potential.

35. The mixer circuit arrangement of claim 27,
15 wherein a first controlled terminal of the ninth transistor is coupled with a first controlled terminal of the tenth transistor.

36. The mixer circuit arrangement of claim 35,
wherein the first controlled terminal of the ninth transistor and the first
20 controlled terminal of the tenth transistor are coupled with a reference potential.

37. The mixer circuit arrangement of claim 27,
wherein a first controlled terminal of the eleventh transistor is coupled with a
25 first controlled terminal of the twelfth transistor.

38. The mixer circuit arrangement of claim 37,
wherein the first controlled terminal of the eleventh transistor and the first
controlled terminal of the twelfth transistor are coupled with a reference
5 potential.
39. The mixer circuit arrangement of claim 24,
wherein the switches comprise one or more transistors.
- 10 40. The mixer circuit arrangement of claim 24,
wherein the plurality of switches of the first mixer circuit comprises:
a first switch, a control terminal of which is coupled to a fourth
switching signal;
a second switch, a control terminal of which is coupled to a fifth
15 switching signal;
a third switch, a control terminal of which is coupled to the fifth
switching signal;
a fourth switch, a control terminal of which is coupled to a reference
potential.
- 20
41. The mixer circuit arrangement of claim 26 and claim 40,
wherein
a first controlled terminal of the first switch is coupled with a second
controlled terminal of the first transistor;

a first controlled terminal of the second switch is coupled with a second controlled terminal of the second transistor;

a first controlled terminal of the third switch is coupled with a second controlled terminal of the third transistor;

5 a first controlled terminal of the fourth switch is coupled with a second controlled terminal of the fourth transistor.

42. The mixer circuit arrangement of claim 24,

wherein the plurality of switches of the second mixer circuit comprises:

10 a fifth switch, a control terminal of which is coupled to a first switching signal;

a sixth switch, a control terminal of which is coupled to a second switching signal;

15 a seventh switch, a control terminal of which is coupled to the first switching signal;

an eighth switch, a control terminal of which is coupled to the second switching signal.

43. The mixer circuit arrangement of claim 27 and 42,

20 wherein

a first controlled terminal of the fifth switch is coupled with a second controlled terminal of the ninth transistor;

a first controlled terminal of the sixth switch is coupled with a second controlled terminal of the tenth transistor;

a first controlled terminal of the seventh switch is coupled with a second controlled terminal of the eleventh transistor;

a first controlled terminal of the eighth switch is coupled with a second controlled terminal of the twelfth transistor.

5

44. The mixer circuit arrangement of claim 24,
wherein each frequency conversion stage of the frequency conversion stages comprises a plurality of transistors.

10 45. The mixer circuit arrangement of claim 44,
wherein the plurality of transistors of the frequency conversion stage of the first mixer circuit comprises:

a fifth transistor, a control terminal of which is coupled to a first differential in-phase input signal having a second frequency;

15 a sixth transistor, a control terminal of which is coupled to a second differential in-phase input signal having the second frequency;

a seventh transistor, a control terminal of which is coupled to the second differential in-phase input signal having the second frequency;

20 an eighth transistor, a control terminal of which is coupled to the first differential in-phase input signal having a second frequency.

46. The mixer circuit arrangement of claim 45,
wherein

25 a first controlled terminal of the fifth transistor is coupled with a second controlled terminal of the first switch;

a first controlled terminal of the sixth transistor is coupled with a second controlled terminal of the second switch;

a first controlled terminal of the seventh transistor is coupled with a second controlled terminal of the third switch;

5 a first controlled terminal of the eighth transistor is coupled with a second controlled terminal of the fourth switch.

47. The mixer circuit arrangement of claim 44,

wherein the plurality of transistors of the frequency conversion stage of the second mixer circuit comprises:

a thirteenth transistor, a control terminal of which is coupled to a first differential quadrature input signal having a second frequency;

15 a fourteenth transistor, a control terminal of which is coupled to a second differential quadrature input signal having the second frequency;

a fifteenth transistor, a control terminal of which is coupled to the second differential quadrature input signal having the second frequency;

20 a sixteenth transistor, a control terminal of which is coupled to the first differential quadrature input signal having the second frequency.

48. The mixer circuit arrangement of claim 47,

wherein

25 a first controlled terminal of the thirteenth transistor is coupled with a second controlled terminal of the fifth switch;

a first controlled terminal of the fourteenth transistor is coupled with a second controlled terminal of the sixth switch;

a first controlled terminal of the fifteenth transistor is coupled with a second controlled terminal of the seventh switch;

5 a first controlled terminal of the sixteenth transistor is coupled with a second controlled terminal of the eighth switch.

49. The mixer circuit arrangement of claim 24,
wherein each frequency conversion stage of the frequency conversion stages
10 comprises a first output terminal and a second output terminal.

50. The mixer circuit arrangement of claim 49,
wherein the first output terminal of the frequency conversion stage of the first
mixer circuit is coupled with the second output terminal of the frequency
15 conversion stage of the second mixer circuit;
wherein the second output terminal of the frequency conversion stage of the
first mixer circuit is coupled with the first output terminal of the frequency
conversion stage of the second mixer circuit;

20 51. The mixer circuit arrangement of claim 46 and claim 49,
wherein

a second controlled terminal of the fifth transistor is coupled with the
first output terminal of the frequency conversion stage of the first
mixer circuit;

a second controlled terminal of the sixth transistor is coupled with the second output terminal of the frequency conversion stage of the first mixer circuit;

a second controlled terminal of the seventh transistor is coupled with the first output terminal of the frequency conversion stage of the first mixer circuit;

a second controlled terminal of the eighth transistor is coupled with the second output terminal of the frequency conversion stage of the first mixer circuit.

10

52. The mixer circuit arrangement of claim 48 and claim 49,
wherein

a second controlled terminal of the thirteenth transistor is coupled with the second output terminal of the frequency conversion stage of the second mixer circuit;

15

a second controlled terminal of the fourteenth transistor is coupled with the first output terminal of the frequency conversion stage of the second mixer circuit;

a second controlled terminal of the fifteenth transistor is coupled with the second output terminal of the frequency conversion stage of the second mixer circuit;

20

a second controlled terminal of the sixteenth transistor is coupled with the first output terminal of the frequency conversion stage of the second mixer circuit.

25

53. The mixer circuit arrangement of claim 49,
wherein each of the first mixer circuit and the second mixer circuit further
comprises a loading adjusting stage to adjust the frequency response of the
loading;
5 wherein the loading adjusting stage of the first mixer circuit is coupled with
the first output terminal of the first mixer circuit;
wherein the loading adjusting stage of the second mixer circuit is coupled with
the first output terminal of the second mixer circuit.
- 10 54. The mixer circuit arrangement of claim 53,
wherein each of the loading adjusting stages comprises an inductance coupled
between the respective first output terminal and a reference potential.
- 55 The mixer circuit arrangement of claim 53,
15 wherein each of the loading adjusting stages comprises at least one
capacitance coupled between the respective first output terminal and another
reference potential.
56. The mixer circuit arrangement of claim 55,
20 wherein each of the loading adjusting stages comprises at least one adjusting
switch coupled between the at least one capacitance and the another reference
potential.
57. The mixer circuit arrangement of claim 49,
25 wherein each of the loading adjusting stages comprises

a first capacitance, a first terminal of which is coupled with the respective first output terminal;

a first adjusting switch,

5

a first controlled terminal of which is coupled with the other reference potential;

a second controlled terminal of which is coupled with a respective second terminal of the first capacitance;

a control input of which is coupled with a first switching signal;

10

a second capacitance, a first terminal of which is coupled with the respective first output terminal;

a second adjusting switch,

a first controlled terminal of which is coupled with the other reference potential;

15

a second controlled terminal of which is coupled with a respective second terminal of the second capacitance;

a control input of which is coupled with a third switching signal.