

**APPARATUS AND METHOD FOR INDEPENDENT
THRESHOLD VOLTAGE CONTROL OF MEMORY
CELL AND SELECT GATE IN A SPLIT-GATE EEPROM**

5 FIELD OF THE INVENTION

The present invention relates generally to split-gate p-channel Electrically Erasable Programmable Read Only Memory (EEPROM) cells, and more particularly to a split-gate memory cell having select and memory transistors that share an active channel region and have independent and distinct threshold voltage (V_t) adjusts that optimize the programming window of the memory cell.

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BACKGROUND OF THE INVENTION

EEPROM memory cells are a class of nonvolatile semiconductor memory in which information may be electronically programmed into and erased from each memory element or cell. Split-gate EEPROM memory cells are one type of EEPROM cell in which the select and memory transistors are merged so that they share the same polysilicon gate, commonly known as the poly 2 or select gate. The poly 2 gate forms both the wordline or gate electrode of the select transistor and the control gate of the memory transistor. This configuration allows for a smaller cell size and thus provides a more efficient design.

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Information is stored in split-gate EEPROM memory cells by placing electronic charge on a "floating gate", which is typically a region of conductive polysilicon (commonly known as poly 1) that is electrically isolated from other conducting regions of the device by insulating dielectric layers that surround it. The charge on the floating gate can be detected in reading the memory cell because it changes the threshold voltage of the memory transistor. This change in threshold voltage changes the amount of current that

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flows through the cell when voltages are applied to it during the read operation and the current can be detected by a sense amplifier circuit.

In a typical EEPROM design, n-channel cells are produced over a p-well substrate. In U.S. Patent No. 5,790,455 entitled "Low Voltage Single Supply CMOS Electrically Erasable Read-Only Memory", which is issued to Caywood and licensed to the assignee of the present application and incorporated herein by reference, however, the opposite configuration is described, namely, p-channel devices over an n-well, which itself resides in a p-type substrate. The advantage of this configuration is that it reduces the magnitude of the applied voltage required for erasing and writing to the device, while maintaining a similar writing speed as compared to the prior art. This configuration also eliminates certain components functionally necessary in the prior art.

Referring to Figure 1, the Caywood approach is illustrated in general terms for a single memory transistor 1. The n-well 3 is created within a p-type substrate 2 and the p-type diffusion regions for the source 4 and drain 5 is created within the n-well 3. Thus, in this design, the select and memory transistors share a common active channel region. The poly 1 or floating gate 6 of the memory transistor 1 is created after the active region for the source 4 and drain 5. The poly 2 or select gate 7 of the memory transistor 1 is fabricated over the floating gate 6. Various non-conductive layers 8 (not shown) insulate the source 4 and drain 5, the floating gate 6 and the select gate 7 from each other.

In the Caywood approach and other prior p-channel designs, the channels of both the memory cell and select transistors are embedded with the same threshold voltage adjust implants or adjusts. The threshold voltage adjust in these devices is used to set the threshold voltage of the select transistor to its desired value. The threshold voltage of the

memory transistor, however, is not set to any value, but rather assumes a "natural" V_t value (zero charge on the floating gate). The drawback of this solution is that when the p-channel memory transistor is "programmed" into the conductive state, its threshold voltage can be much more positive than the select transistor. In this case, the threshold voltage of the select transistor alone controls the combined threshold voltage of the memory transistor and select transistor. Thus, part of the threshold window (V_t window) of the cell, i.e., the difference between the threshold voltages of the cell in the programmed (V_{tw}) and the erased (V_{te}) states, is lost.

For example, the memory cell transistor alone might have a programmed V_t of +3.0 V (volts) and an erased V_t of -5.0 V, while the select transistor would typically have its V_t set at -0.8V. The overall threshold window of the memory cell and select gate would be from -0.8 V to -5.0 V, and not the threshold window of the memory cell alone which is from +3.0 V to -5.0 V. The part of the threshold window from +3.0 V to -0.8 V is lost. The disadvantage of this is that it reduces the working life of the memory cell.

In particular, the V_t window of a cell changes with the number of program and erase cycles that it undergoes. The V_t window typically collapses with increasing program/erase cycles due to electron trapping in the tunnel oxide. Figure 2 illustrates for a p-channel split-gate EEPROM cell how the V_t window decreases with cycles. The solid lines for V_{tw} and V_{te} indicate the average values of the thresholds of a large population of cells. The dashed lines on either side indicate the spread in V_{tw} and V_{te} due to processing variations. In addition to the process variations and V_t window collapse with program/erase cycling, some loss of charge with time from an erased or written cell must also be accounted for. This is indicated as an inner pair of dotted lines,

which reduces the minimum V_t window even more. The minimum V_t window, at any given number of cycles is taken inside the dotted line envelope. Beyond all of this, there are still other effects, such as a sense amplifier trip point variations and variations due to operation over a range of temperatures, that require that the V_t window be made even wider.

There are a number of ways of increasing the V_t window, but they all have drawbacks. For example, the V_t window can be made wider by using a larger programming voltage, V_{pp} . However, if V_{pp} is increased, then the tunnel oxide is subjected to a larger electric field stress in each program/erase cycle and the V_t window collapse with cycling becomes worse. The V_t window can also be made wider by making the tunnel oxide thinner. However, making the tunnel oxide thinner, makes it more likely that charge stored on the floating gate will leak off over time after the tunnel oxide has been stressed with program/erase cycles. This effect is known as stress-induced leakage current (SILC). The V_t window can further be widened by increasing the coupling ratio of the cell. An increase in the coupling ratio of the cell is possible only by either increasing the silicon chip area consumed by the cell or by decreasing the interpoly dielectric thickness. It is not desirable to increase the silicon chip area for obvious reasons, and decreasing the interpoly dielectric can also reduce the ability of the cell to retain charge, as well as make it more difficult to manufacture the cell in a high yielding process.

Accordingly, it is desirable to optimize the programming window of the memory cells in a p-channel split-gate EEPROM without any of the drawbacks associated with the solutions mentioned above.

SUMMARY OF THE INVENTION

In one aspect of the present invention, a split-gate EEPROM memory cell is provided. The memory cell includes a memory transistor and select transistor that share a common gate. The memory cell further includes two independent and distinct threshold voltage adjusts implanted in different portions of a channel region of substrate of the memory cell. One of the threshold voltage adjusts is disposed in relation to the memory transistor so as to influence its threshold voltage. The other threshold voltage adjust is disposed in relation to the select transistor so as to influence its threshold voltage. In the preferred embodiment of the present invention the threshold voltage adjust associated with the memory transistor is formed of an n-type dopant, preferably Arsenic or Phosphorus. In this embodiment, the threshold voltage adjust associated with the select transistor is formed of a p-type dopant, preferably Boron or BF_2 .

In another aspect of the present invention, a method of fabricating a split-gate memory cell is provided. The method includes the step of implanting a threshold voltage adjust associated with the memory transistor in a channel region of a substrate of the memory cell. The method further includes the step of implanting a threshold voltage adjust associated with the select transistor in a different portion of the channel region of the cell substrate. In the preferred method, the threshold voltage adjust associated with the memory transistor is formed by implanting an n-type dopant into the channel region of the substrate. In this method, the threshold voltage adjust associated with the select transistor is formed by implanting a p-type dopant into the channel region of the substrate. During this step, implantation of the p-type dopant in the portion of the

channel region associated with the memory transistor is prevented by the floating gate, which acts as a self-aligning mask.

In one embodiment of the invention, the step of implanting the n-type of dopant is performed before the floating gate is formed. In another embodiment, this step is performed after the floating gate is formed.

The use of independent and distinct threshold voltage adjusts widens the threshold voltage window of the memory transistor and select transistor, and thus extends the operational life of the memory cell.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

Figure 1 is cross-sectional view of a prior art memory cell in a p-channel split-gate EEPROM;

Figure 2 is a graph of the threshold voltage of a memory cell in the programmed and erased states as a function of the number of program/erase cycles that the cell undergoes;

Figure 3 is a plan view of a portion of memory cell array of a p-channel split-gate EEPROM according to the present invention;

Figure 4 is a cross-sectional view taken along line A-B of the memory cell in the upper-left hand corner of memory cell array shown in Figure 3;

Figure 5 is a graph illustrating the write and erase threshold voltages (V_t) of the split-gate EEPROM according to the present invention as a function of program voltage (V_{pp});

Figures 6-18 illustrate the process steps that are performed in carrying out one method of forming separate threshold voltage adjust implants for the memory transistor and the select transistor according to the present invention;

Figures 19-29 illustrate the process steps that are performed in carrying out another method of forming separate threshold voltage adjust implants for the memory transistor and the select transistor according to the present invention.

While the present invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to the drawings, the preferred embodiments of the present invention will now be described. Referring initially to Figure 3, a portion of a memory cell array according to the present invention, the upper left-hand corner, is shown. The figure shows 8 columns (8 bitlines) of cells running vertically and 8 rows (8 wordlines) of cells running horizontally. To the right and below this portion of the memory cell, many additional columns and rows that form the rest of the array are indicated. To the left and above the portion of the memory cells shown is the peripheral circuitry, which is used to access the memory array and perform other chip functions. For ease of illustration, the present invention will be described with reference to a single memory cell, which is shown in

Figure 4, which is a cross-sectional view of the memory cell in the upper left-hand corner of the array 10 through line A-B.

With reference to Figure 4, the single memory cell according to the present invention is illustrated generally by reference numeral 11. The memory cell 11 includes a
5 memory transistor 12 and select transistor 14 formed on a p-type silicon substrate 16. The memory cell 11 resides in an n-well 22, which in turn is formed in the substrate 16. The substrate 16 has p-type diffusions regions, which form a source 18 and drain 20. Reference numeral 24 refers to the metal source contact, which is disposed on p-type region 18 and reference numeral 26 refers to the metal bitline (drain) contact, which is disposed on p-type
10 region 20. The memory transistor 12 includes a floating gate 28, which is a conductive layer, and a select gate 30, which is a conductive layer shared with the wordline of the select transistor 14.

The memory cell 11 further includes separate threshold voltage adjusts 34 and 36 for the memory transistor 12 and the select transistor 14, respectively. The threshold
15 adjust implant 34 is an n-type dopant and is preferably Arsenic ($_{75}\text{As}^+$) or Phosphorus ($_{31}\text{P}^+$). The threshold voltage adjust 36 is a p-type dopant and is preferably Boron ($_{11}\text{B}^+$) or BF_2^+ . The advantage of the n-type dopant is that it has the effect of reclaiming the lost threshold voltage window, which results from the merged cell construction. This implant shifts the threshold of the memory transistor 12 in the negative direction for both
20 programmed and erased states. For example, with an implant of Arsenic at a dose of $1.0 \times 10^{13} \text{ cm}^{-2}$ (per centimeter squared) in the cell channel only, the programmed V_t of the cell alone might be shifted to 0.0V (a shift of 3V in the negative direction) and the erased V_t would be shifted by the same amount to -8.0V. The threshold window of the memory

transistor 12 and the select transistor 14 together would then be from $-0.8V$ to $-8.0V$, giving an increase of $3V$ in the threshold window of the cell ($window = |V_{te} - V_{tw}|$). It is critical that the select transistor 14 V_t is not shifted negatively along with the memory transistor 12 because then the entire V_t window could be shifted negatively without becoming any wider. Having the two threshold voltage adjusts independent of one another prevents this from happening.

Graphs of the threshold voltage in the erased state, V_{te} , and the threshold voltage in the programmed state, V_{tw} , as a function of the program voltage V_{pp} of the memory cell 11 is shown in Figure 5. In the drawing, two curves are illustrated, one that indicates the dependence of V_{te} on V_{pp} (the V_{te} - V_{pp} Curve) and one that indicates the dependence of V_{tw} on V_{pp} (the V_{tw} - V_{pp} Curve). With respect to the V_{te} - V_{pp} Curve, each value of V_{te} is obtained by first programming the cell into a written state with $V_{pp}=16V$, and then erasing the cell with a different value of V_{pp} . It can be seen that as V_{pp} increases, V_{te} becomes increasingly negative. In fact, for every 1-Volt increase in V_{pp} , V_{te} becomes approximately 1-Volt more negative. The erased threshold voltage, V_{te} , is measured in the following manner. In the erased state, the overall threshold of the select transistor plus cell transistor is controlled by the threshold of the cell transistor, because it is much more negative than the select transistor. As the voltage, V_g , on the shared polysilicon gate of the two transistors is swept from 0-Volts to larger negative values, the select transistor first turns on (at, for example, $V_g = -1.3V$), but no current, I_d , flows because the cell transistor has not been turned on. Eventually, the V_g reaches a large enough negative value that the cell transistor turns on and, finally, current flows because both transistors are on together. The gate voltage at which the current, I_d ,

reaches a value of 1-microampere (μA) is considered the threshold voltage in the erased state, $V_g = V_{te}$.

With respect to the V_{tw} - V_{pp} Curve, each value of V_{tw} is obtained by first erasing the cell with $V_{pp} = 16\text{V}$. Then, from this erased state, the cell is programmed to a written state with a different value of V_{pp} . It can be seen that at low values of V_{pp} , V_{tw} increases by approximately 1-Volt for every 1-Volt increase in V_{pp} , but only up to a point. At about $V_{pp} = 12\text{V}$, the curve starts to level off at a value of $V_{tw} \sim -1.0\text{V}$ to -1.5V , and remains at this value as V_{pp} increases further. At this point, the select transistor has a more negative V_t than the cell transistor. Thus, in this situation, it is the select transistor that controls the activation or "turn on" of the two-transistor combination. (The line through the V_{tw} data points is an extrapolation of the V_{tw} curve from the linearly increasing portion to indicate that the threshold of the cell transistor alone is becoming increasingly positive, but it is not possible to measure its individual V_t , because the select transistor is in series with it and controls the overall threshold.)

Figure 5 also illustrates the V_t window that is actually obtained and a so-called "virtual" V_t window. The "virtual" V_t window is the V_t window that would be obtained if the select transistor were not limiting the written state threshold. In the present invention, the sloped portions of the V_{te} - V_{pp} and V_{tw} - V_{pp} Curves, which is where the cell transistor controls the overall threshold, are made to shift downward, while the flat part of the V_{tw} - V_{pp} curve, which is controlled by the V_t of the select transistor alone, is held constant, which is preferably at between -0.5V and -2.0V . The fabrication process according to the present invention allows the thresholds of the cell transistor and select

transistor to be adjusted independently, allowing the flat part of the V_{tw} - V_{pp} curve to remain stationary, while the sloped parts of both curves are shifted downward. This has the overall effect of making the actual V_t window wider for a given value of V_{pp} .

Two alternate methods of fabricating the memory cell 11 shown in Figure 4 will now be described. In one of the methods, two photoresist masking steps are used, in the other method, only one photoresist masking step is used. The first method is illustrated with reference to Figures 6-18, and the second method is illustrated with reference to Figures 19-29.

After other steps in the process of manufacturing the memory cell 11 have been performed, such as n-well formation, device isolation, and field oxide growth, which do not form a part of the present invention, the threshold adjust implant 34 for the memory transistor is formed. This phase in the fabrication process proceeds in one method according to the present invention depicted in Figure 6-18. First, a sacrificial oxide, such as a SiO_2 layer 100 is formed on the n-well 22 of the substrate 16 adjacent to a field SiO_2 layer 102, as shown in Figure 6. Preferably, the SiO_2 layer 100 is formed at a thickness in the range of 50-500 Å (angstroms). The sacrificial SiO_2 layer 100 may be formed by thermally growing the layer (not shown), or depositing it, or by any other method known in the art. Next, a photoresist layer 104 is patterned with a mask that exposes n-well 22 over the silicon substrate 16, as shown in Figure 7. With reference to Figure 3, the photoresist layer 104 remains over the peripheral circuitry, but is not present over at least a portion of the memory array 10.

Next, an n-type dopant 106 is implanted into the near-surface region of the n-well 22, using an atomic beam, known conventionally as an ion implanter, as shown in Figure 8.

The n-type dopant that is implanted in this step augments the concentration of n-type dopant already in the n-well. When the n-type dopants are incorporated on lattice sites in the silicon substrate they give up an extra electron, and thus leave behind a singly ionized positive ion core. For this reason, the implanted region is indicated with "+" signs.

5 Examples of n-type dopants that may be used are Arsenic and Phosphorus. The implant dose is preferably in the range of 0 to 5.0×10^{14} cm⁻². The implant energy needs to be enough to allow the implanted ions to get through the sacrificial SiO₂ layer 100. As those of ordinary skill in the art will appreciate, other methods may be used to implant the n-type dopant 106. The precise method of implanting the n-type dopant 106 is not critical to the

10 present invention. The photoresist layer 104 is then removed by a dry plasma or wet chemical etching process or other equivalent process known in the art, as shown in Figure 9. Next, the sacrificial SiO₂ layer 100 is removed by a wet chemical etch or other equivalent process known in the art, as shown in Figure 10.

In the next phase of the process, the tunnel dielectric (gate oxide of the memory

15 transistor) and the floating gate 28 are formed. These steps proceed as follows. First, the tunnel dielectric layer 108 is formed on the channel region of the memory transistor 12/select transistor 14, as shown in Figure 11. As those of ordinary skill in the art will appreciate, the layer 108 preferably has a thickness in the range of 60-120Å. Next, the floating gate 28 is formed by depositing a polysilicon layer 110 on the tunnel dielectric 108,

20 as shown in Figure 12. Preferably the polysilicon layer 110 is between approximately 600 and 5000 Å thick, and more preferably is approximately 1500 Å thick. Next, the polysilicon layer 110 is doped to make the layer conductive. In this step, preferably n- or p-type dopants are introduced into the polysilicon layer. This may be accomplished by either

annealing the layer in a Phosphorus oxychloride (POCl_3) gas, by doping the polysilicon layer in-situ when deposited, *i.e.*, during the depositing step, or by implantation. As those of ordinary skill in the art will appreciate, other methods may be used to dope the polysilicon layer. Next, a dielectric layer 112 is formed over the polysilicon layer 110. The dielectric layer 112 may be formed of one or more layers of material known in the art.

Next, a photoresist layer 114 is deposited on the stack of layers formed, as shown in Figure 13. The photoresist layer 114 is patterned with a mask and used to define the floating gate 28 (Figure 4). The stack of layers is then anisotropically etched, preferably using a dry plasma process, down to the tunnel dielectric 108, so as to leave at least a portion of the SiO_2 layer 108 on the channel region, as shown in Figure 14. The photoresist layer 114 protects the floating gate 28 areas during etching. The photoresist layer 114 is then removed by a dry plasma or wet chemical etching process, thus leaving a floating gate pattern 28, as shown in Figure 15.

In the next phase of the process, the threshold voltage adjust implant 36 (Figure 4) is formed. This is accomplished first by depositing a photoresist layer 116 over the peripheral circuitry. A portion or all of the memory array 10, including at least some and possibly all of the individual memory cells 11, however, is not masked by the photoresist layer 116 during this step, as shown in Figures 3 and 16. Next, a p-type dopant 118 is implanted in the surface region of the n-well 22. The p-type dopant 118 compensates or more than compensates for the n-type dopant 106 that was previously implanted. Furthermore, since p-type dopants accept an extra electron when they are incorporated into lattice sites in the silicon, they have a net negative charge. Thus, the implanted region is indicated in the drawings with a "-" sign. The implantation step is preferably performed as described above

using an ion implanter. The p-type dopant is preferably Boron (B^{+}) or BF_3 and is preferably implanted at a dose of 0 to $5.0 \times 10^{14} \text{ cm}^{-2}$. Furthermore, the energy of the implanted ions needs to be large enough to allow them to penetrate the tunnel dielectric 108.

5 The floating gate 110 (28 in Figure 4) blocks implantation of the p-type dopant 118 into the part of the memory transistor part of the channel, and thus acts as a mask separating the p-type dopant from the n-type dopant. The advantage of using the floating gate 110 as the mask is that it auto-aligns the implants, and thus avoids any misalignment that may occur if a separate photoresist layer were used. Thus, the memory transistor 12 and select
10 transistor 14 threshold voltage adjust implants 34 and 36 are independent and distinct, one being an n-type, and the other being a p-type, respectively, and self-aligned. Next, the photoresist layer 116 is removed by a dry plasma or wet chemical process, as shown in Figure 18.

 The shared gate electrode or select gate of the select and memory transistors 30,
15 source and drain regions 18 and 20 of the memory cell 11 (Figure 4), and metal interconnect are then all formed using techniques well known in the art. Indeed, the exact steps in forming these latter components are not critical to the present invention.

 In an alternate method the threshold voltage adjust implants 34 and 36 are formed using only one photoresist masking step rather than two. This is done to reduce the process
20 cost. In this alternate method, the n-type dopants are not implanted into the channel region before the polysilicon layer making up the floating gate 28 is deposited and patterned. Rather, after the floating gate 28 is patterned, a new photoresist mask is applied and two implants are done in succession. The memory cell or transistor implant 34 may be done

first using an n-type of dopant (e.g., P or As) at an energy level that is high enough to completely penetrate the polysilicon layer making up the floating gate and the tunnel oxide layers. In this case, the n-type dopant enters the cell channel near the surface to shift cell V_t , but goes very deep into the silicon outside of the polysilicon layer making up the floating gate 28 where the select transistor 14 channel is located. A second p-type dopant (e.g., B or BF_2) is then implanted with the photoresist mask still in place. This implant is done at a low energy so that it is blocked by the polysilicon layer over the memory cell channel region, but goes into the surface of the select transistor 14 channel to adjust its V_t . It should be appreciated by those of ordinary skill in the art, however, the exact order in which the dopants are implanted is not critical, i.e., the p-type of dopant may be implanted before the n-type of dopant. An advantage of this method is that there is a reduced process cost, since one less photoresist masking step, and one less photoresist strip, has to be performed. Another advantage of this method is that the implants are subjected to less fabrication steps at high temperatures, which makes them redistribute less due to diffusion, and thus makes them more effective in controlling the thresholds. Yet, another advantage of this method is that the deep n-type dopant implanted in the select transistor 14 channel region acts as a deep punch-through suppression implant for the select transistor 14, which helps it to shut off current flow more ideally when the cell is deselected.

The steps of the alternate method will now be described in more detail with reference to Figures 19-29. After the preliminary steps such as n-well formation, device isolation, field oxide 200 growth, and sacrificial SiO_2 layer 202 formation are performed, which are shown in Figure 19, the sacrificial SiO_2 layer 202, which is approximately 50-500 Å thick, is removed by a wet chemical etch process, as shown in Figure 20. Next, a

thin tunnel dielectric film 204, approximately 60-120A thick is formed on the channel region of the memory transistor 12/select transistor 14, as shown in Figure 21.

Next, a layer of polysilicon 206 is deposited, which is preferably between approximately 600 and 5000A thick, as shown in Figure 22. The polysilicon layer 206 later becomes the floating gate 28 (Figure 4). Next, the polysilicon layer 206 is doped in the same manner that the polysilicon layer 110 described above is doped. A dielectric layer 208 is then formed over the polysilicon layer 206, as also shown in Figure 22. Like the dielectric layer 112, the dielectric layer 208, may be formed of one or more layers of material known in the art.

Next, a photoresist layer 210 is deposited on the stack of layers formed, as shown in Figure 23. The photoresist layer 210 is patterned with a mask and used to define the floating gate 28 (Figure 4). The stack of layers is then anisotropically etched, preferably using a dry plasma process, down to the tunnel dielectric 204, so as to leave at least a portion of the tunnel dielectric on the channel region, as shown in Figure 24. The photoresist layer 210 is then removed by a dry plasma or wet chemical etching process, thus leaving a floating gate pattern 28, as shown in Figure 25.

In the next phase of the process, the threshold voltage adjust implants 34 and 36 are formed. This is accomplished first by depositing a photoresist layer 212 over the peripheral circuitry. A portion or all of the memory array 10, including at least some and possibly all of the individual memory cells 11, is not masked by the photoresist layer 212 during this step, as shown in Figures 3 and 26. An n-type dopant 214 (such as Phosphorus or Arsenic) is then implanted at an energy level sufficient to cause the dopant atoms to penetrate through the dielectric layer 208, the polysilicon layer 206, and the tunnel oxide layer 204 in

the cell channel region, as shown in Figure 27. Outside of the cell channel region, which is covered by the dielectric layer 208 and the polysilicon layer 206, the n-type dopant penetrates much deeper into the silicon substrate, as also shown in Figure 27. This outside region is the select transistor channel 14 region. Because the n-type dopant in this region is far away from the surface, it has little impact on the select transistor threshold voltage. As explained above, since n-type dopants give up an extra electron when they are incorporated into lattice site in the silicon, they create a positively charged ion core. For this reason, the implanted region is indicated with "+" sign. Also, as in the above described method, the implant dose is preferably in the range of 0 to $5.0 \times 10^{14} \text{ cm}^{-2}$.

10 In the next step, the p-type dopant 216 is implanted at a high enough energy to allow the dopant atoms to penetrate the tunnel dielectric layer 204, but not so high as to permit the dopant atoms to penetrate through the dielectric layer 208, the polysilicon layer 206, and the tunnel dielectric 204 in the area defining the memory transistor channel region. Outside of this region, the p-type dopant is able to penetrate the tunnel dielectric 204, as shown in Figure 28. Again, this latter area defines the select transistor channel region. Because in this region the p-type dopant is close to the surface, it changes the select transistor 14 threshold voltage. Again, as discussed above, since p-type dopants accept an extra electron when they are incorporated into lattice sites in the silicon substrate, they create a negatively charged ion core. For this reason, the implanted region is indicated with
15 "-" sign. Again, the p-type dopants are preferably Boron or BF_2 , and the implant dose is preferably in the range of 0 to $5.0 \times 10^{14} \text{ cm}^{-2}$. Next, the photoresist layer 212 is removed by a dry plasma or wet chemical etching process, as shown in Figure 29.
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The shared gate electrode or select gate of the select and memory transistors 30, source and drain regions 18 and 20 of the memory cell 11 (Figure 4), and metal interconnect are then all formed using techniques well known in the art. Indeed, the exact steps in forming these latter components are not critical to the present invention.

5 While the embodiments discussed above involve the fabrication of p-channel cells, those of ordinary skill in the art will appreciate, the present invention is equally applicable to n-channel cells. In such an application, the threshold voltage adjusts would be reversed. That is, a p-type of dopant such as Boron or BF_2 would be used to form the threshold voltage adjust for the memory transistor 12 (Figure 4) and an n-type dopant such as Arsenic
10 or Phosphorus would be used to form the threshold voltage adjust for the select transistor 14 (Figure 4). In addition, those of ordinary skill in the art should appreciate that other process steps (not forming a part of the present invention) are involved in fabrication of a memory cell than those described herein. It should therefore be evident that the particular embodiments disclosed above might be altered or modified and all such variations are
15 considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS



What is claimed is:

1. A memory cell of the type having a memory transistor and select transistor that share a common gate, said memory cell comprising two independent and distinct threshold voltage adjusts implanted in different portions of a channel region of a substrate of said memory cell, one threshold voltage adjust being disposed in relation to the memory transistor so as to influence the threshold voltage of said memory transistor and the other threshold voltage adjust being disposed in relation to the select transistor so as to influence the threshold voltage of said select transistor.
2. The memory cell according to Claim 1, wherein the threshold voltage adjust disposed in relation to the memory transistor is formed of an n-type dopant.
3. The memory cell according to Claim 2, wherein the n-type dopant is selected from the group consisting of Arsenic and Phosphorus.
4. The memory cell according to Claim 1, wherein the threshold voltage adjust disposed in relation to the select transistor is formed of a p-type dopant.
5. The memory cell according to Claim 4, wherein the p-type dopant is selected from the group consisting of Boron and BF_2 .
6. A split-gate memory cell of a semi-conductor device comprising:
 - a. a substrate having a channel region;



- b. a memory transistor having a floating gate, said channel region having a portion adjacent to the floating gate and a portion outside of the floating gate;
 - c. a first threshold voltage adjust implanted in the portion of the channel region adjacent to the floating gate;
 - d. a select transistor having a gate electrode that is shared with the memory transistor; and
 - e. a second threshold voltage adjust implanted in the portion of the channel region outside of the floating gate.
7. The split-gate memory cell according to Claim 6, wherein the first threshold voltage adjust is formed of an n-type dopant selected from the group consisting of Arsenic and Phosphorus.
8. The split-gate memory cell according to Claim 6, wherein the second threshold adjust is formed of a p-type dopant selected from the group consisting of Boron and BF_2 .
9. A method of fabricating a split-gate memory cell comprising the steps of:
- a. implanting a first threshold voltage adjust in a channel region of a substrate of said memory cell;



- b. forming a floating gate over a portion of a channel region of the substrate,
and
- c. implanting a second threshold voltage adjust in the channel region of the
substrate outside of the portion of the channel region covered by the floating
gate.
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10. The method of fabricating a split-gate memory cell according to Claim 9, wherein
the step of implanting the first threshold voltage adjust comprises the steps of
forming an oxide layer on the substrate and implanting a dopant through the oxide
layer.
- 10 11. The method of fabricating a merged split-gate memory cell according to Claim 10,
wherein the step of implanting a dopant through the oxide layer includes the step of
implanting an n-type dopant through the oxide layer that is selected from the group
consisting of Arsenic and Phosphorus.
12. The method of fabricating a split-gate memory cell according to Claim 9, wherein
15 the step of forming the floating gate over a portion of the channel region of the
substrate comprise the steps of:
- a. depositing a layer of polysilicon material over the substrate;
- b. placing a protective photoresist layer over a portion of the layer of
polysilicon material;



- c. etching away the portion of the layer of polysilicon material not covered by the protective photoresist layer; and
 - d. removing the protective photoresist layer.
- 13. The method of fabricating a split gate memory cell according to Claim 9, wherein
5 the step of implanting the second threshold voltage implant includes the step of implanting a p-type dopant into the portion of the channel region not covered by the floating gate.
- 14. The method of fabricating a split-gate memory cell according to Claim 9, further comprising the step of forming a select gate over the floating gate and a portion of
10 the channel region outside of the floating gate.
- 15. The method of fabricating a split-gate memory cell according to Claim 14, wherein the step of forming the select gate comprises the steps of:
 - a. depositing a layer of polysilicon material over the floating gate and substrate;
 - 15 b. placing a protective photoresist layer over a portion of the layer of polysilicon material.
 - c. etching away the portion of the layer of polysilicon material not covered by the protective photoresist layer; and
 - d. removing the protective photoresist layer.



16. The method of fabricating a split-gate memory cell according to Claim 14, further comprising the step of forming a dielectric layer between the floating gate and the select gate.
17. The method of fabricating a split-gate memory cell according to Claim 9, wherein
5 step of forming a floating gate over a portion of a channel region of the substrate is performed prior to the step of implanting a first threshold voltage adjust in a channel region of a substrate of said memory cell and the step of implanting a second threshold voltage adjust in the channel region of the substrate outside of the portion of the channel region covered by the floating gate.
- 10 18. The method of fabricating a split-gate memory cell according to Claim 17, wherein the step of implanting a first threshold voltage adjust includes the step of implanting an n-type dopant at an energy level sufficient to enable the n-type dopant atoms to penetrate through the floating gate and implant themselves in the channel region of the substrate covered by the floating gate, and penetrate into the substrate outside of
15 the floating gate deeply enough to have a negligible effect on the threshold voltage in this region.
19. The method of fabricating a split-gate memory cell according to claim 18, wherein the step of implanting a second threshold voltage adjust includes the step of implanting a p-type dopant at an energy level sufficient to enable the p-type dopant
20 atoms to implant themselves into the channel region of the substrate outside of the portion of the channel region covered by the floating gate, but not so high as to



enable the p-type dopant atoms to penetrate the floating gate and implant themselves in the channel region covered by the floating gate.

20. The method of fabricating a split-gate memory cell according to claim 9, wherein the step of implanting a first threshold voltage adjust includes the step of implanting a dopant at a dose in the range of 0 to $5.0 \times 10^{14} \text{ cm}^{-2}$ and the step of implanting a second threshold voltage adjust includes the step of implanting a dopant at a dose in the range of 0 to $5.0 \times 10^{14} \text{ cm}^{-2}$.