

METHOD FOR FORMING A HIGH RESISTIVITY HANDLE SUPPORT FOR A COMPOSITE SUBSTRATE

FIELD OF THE INVENTION

The present invention relates to a high resistivity handle for a composite substrate. It also relates to a method for forming such a handle substrate.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

WO2017144821 describes a high resistivity handle substrate for a composite substrate comprising a charge-trapping layer disposed on a base substrate. The composite substrate may be, for instance, a silicon on insulator substrate comprising a silicon thin film transferred onto the handle substrate.

In one embodiment described in the aforementioned document, the charge-trapping layer is made of an intermediate layer and of a polycrystalline main layer. The intermediate layer is composed of a silicon and carbon alloy (or of carbon) and is disposed directly on the base substrate. The main layer is disposed on, and in contact with, the intermediate layer.

The multilayer structure of the charge trapping layer makes it possible to prevent the phenomenon of recrystallization of the main polycrystalline layer when the substrate is exposed to a high temperature, for example during its manufacture or during the manufacture of integrated devices on the composite substrate. When the trapping layer recrystallizes, even partially, the RF (Radio Frequency) performances of the substrate and of the integrated devices that will be formed thereon are affected, which is of course not desirable.

To prepare the high resistivity handle substrate, the document proposes to place the base substrate in a conventional deposition chamber. A flow of a first precursor gas travel through the chamber. The first precursor gas may be a silicon containing precursor, for example SiH_4 , to grow the main polycrystalline layer. A second precursor gas comprising carbon is introduced into the chamber to form the intermediate layer. This precursor gas may be composed of methane (CH_4), ethane (C_2H_6), propane (C_3H_8), acetylene (C_2H_2), ethylene (C_2H_4)...

When the two precursor gases flow simultaneously into the chamber to grow the intermediate silicon and carbon alloy layer, there is a risk of forming deposit on the chamber walls and on the susceptor onto which the base substrate resides. Such deposits require extensive cleaning of the chamber, for instance by etching, that is time consuming and reduces manufacturing throughput. Such a problem is for instance documented in the publication WO2019002376. Also, deposits of silicon and carbon species may create particles that may be transported onto the base substrate or handle substrate surfaces, and render the substrate unsuitable for further use.

It has also been observed that doping species, like boron, could be incorporated into the intermediate layer and/or main layer, in particular when the base substrate is a standard CZ silicon substrate (i.e. not design to present high resistivity characteristics). Such CZ silicon substrate comprises some residual concentration of boron and other dopants, that may migrate toward the base wafer surface during growth of the charge trapping layer. When present in the charge trapping layer, the dopant reduces the resistivity of that layer and the overall RF performance of the handle substrate.

SUBJECT MATTER OF THE INVENTION

Embodiments of the present invention aim to overcome all or some of the aforementioned drawbacks. They aim in particular to provide a method for forming a handle substrate presenting high resistivity characteristics and being easy to manufacture.

BRIEF DESCRIPTION OF THE INVENTION

An aspect of the present invention provides a method for forming a high resistivity handle substrate for a composite substrate, the method comprising :

- providing a base substrate made of monocrystalline silicon;
- exposing the base substrate to a carbon single precursor at a pressure below atmospheric pressure to form a polycrystalline silicon carbide layer of at least 10 nm on the surface of the base substrate; and then
- growing a polycrystalline charge trapping layer on the polycrystalline silicon carbide layer.

According to other advantageous and non-limitative features of the invention, taken alone or in any technically achievable combination :

- the base substrate has a resistivity greater than 1000 ohm.cm;
- the base substrate has a resistivity smaller than 1000 ohm.cm;
- the method further comprises forming a silicon intrinsic epitaxial layer directly on the base substrate before exposing the base substrate to the carbon single precursor;

- the charge trapping layer has a thickness greater than 5 or 10 microns;
- the charge trapping layer is made of polycrystalline silicon;
- the carbon single precursor presents a temperature comprised between 700°C and 1200°C;
- the method further comprises exposing the base substrate to a reducing atmosphere at a temperature of at least 900°C to remove a native oxide layer from the base substrate, before exposing the base substrate to the carbon single precursor;
- the polycrystalline silicon carbide layer is stoichiometric.

There is also disclosed a high resistivity handle substrate for a composite substrate comprising :

- a base substrate made of monocrystalline silicon;
- a polycrystalline silicon carbide layer presenting a thickness of least 10 nm directly on the surface of the base substrate ;
- a polycrystalline charge trapping layer on the polycrystalline silicon carbide layer.

Optionally, the polycrystalline silicon carbide layer may comprise a concentration of dopant less than 10^{14} at/cm³ and the high resistivity handle substrate may further comprise a silicon intrinsic epitaxial layer in contact with the base substrate and with the polycrystalline silicon carbide layer. The polycrystalline silicon carbide layer is stoichiometric.

There is also disclosed a composite substrate comprising a high resistivity handle substrate as previously

described and, on top of the handle substrate, a thin film made of crystalline material.

Advantageously, the composite substrate further comprises a dielectric layer disposed between the handle substrate and the thin film.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will emerge from the detailed description of the invention that follows with reference to the accompanying figures, in which:

[Fig. 1] Figure 1 shows schematically a handle substrate for a semiconductor structure according to the invention;

[Fig. 2] Figure 2 shows schematically a composite substrate using a handle substrate according to the invention;

[Fig. 3]

[Fig. 4]. Figures 3 and 4 are respective SRP measurement for two handle substrates.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows schematically a high resistivity handle support for a composite substrate according to an embodiment of the present disclosure. The handle substrate 1 may be in the form of a circular wafer, of standardized size, for example 200 mm or 300 mm, or even 450 mm in diameter. However, the invention is in no way limited to these dimensions or to this form.

The handle substrate 1 comprises a monocrystalline silicon base substrate 3, typically several hundreds of microns thick. The silicon base substrate presents a smooth surface, with a roughness below 0,5 nm RMS. Preferentially, the silicon base substrate has high resistivity, greater than 1000 ohm.cm, and more preferentially greater than 3000 ohm.cm. In this way the density of the charges, holes or electrons that are liable to move in the base substrate is limited. It may for example be a CZ substrate with a small interstitial oxygen content that has, as is well known per se, a resistivity that may be greater than 500 ohm.cm or greater than 1000 ohm.cm.

However, the invention is not limited to a silicon base substrate having such resistivity, and also procures advantages in RF performances when the base substrate has a more usual resistivity, around a few hundreds of ohm.cm or less, for instance less than 1000 ohm.cm or less than 500 ohm.cm or even less than or equal to 10 ohm.cm.

When the base substrate 3 has a more usual resistivity of less than 1000 or 500 ohm.cm, it may be advantageous to provide a silicon intrinsic epitaxial layer disposed directly on top of the base substrate 3. By "intrinsic" it is meant that this layer is not intentionally doped. The silicon epitaxial layer is grown to present in this case a resistivity higher than 2000 ohm.cm, preferentially between 2000 ohm.cm and 20000 ohm.cm. Said epitaxial layer 2 has a thickness typically ranging from 2 to 100 microns. This approach is particularly advantageous when the base substrate is made of silicon, as it provides a substrate with appropriate surface resistivity, without the drawback in terms of cost and availability associated with base substrates that exhibit a high resistivity across their total thickness.

The handle substrate 1 also comprises, on the base substrate 3, a polycrystalline charge trapping layer 2. The function of the charge trapping layer is to trap any charge carriers that may be present in the handle substrate 1 and to limit the mobility thereof.

For reasons of availability and cost, the charge trapping layer 2 is preferentially made from polycrystalline silicon. However, it may be formed from another semiconductor and polycrystalline material, or comprise a part made from another semiconductor and polycrystalline material. It may be a case for example of germanium, silicon germanium, etc.

In all cases, the polycrystalline charge trapping layer 2 has a high resistivity, typically above 3000 ohm.centimetre. For this purpose, this layer is not intentionally doped, that is to say it has a concentration of dopants of less than 10^{14} atoms per cubic centimeter. It may be rich in nitrogen or carbon in order to improve its resistivity characteristic.

The high resistivity handle substrate 1 also comprises, interposed between the base substrate 3 and the polycrystalline charge trapping layer 2, a polycrystalline silicon carbide layer 4 of at least 10 nm thick. Such a thickness of silicon carbide forms an efficient barrier against the diffusion of dopants, such as boron, that may be contained in the base substrate 3. This layer typically presents a resistivity above 1000 ohm.centimeters. By "silicon carbide layer", it is meant that the silicon and carbon species forming the layer are present in stoichiometric or close to stoichiometric proportion in the layer.

The high resistivity handle substrate 1 thus consists of the base substrate 3 (optionally comprising a top silicon intrinsic

epitaxial layer), of the polycrystalline silicon carbide layer 4 directly in contact with the base substrate 3, and of a polycrystalline charge trapping layer 2 on, and directly in contact with, the silicon carbide polycrystalline layer 4.

Provision is not made, in this particular embodiment, for incorporating other layers, in particular electrically insulating layers in or below the polycrystalline charge trapping layer 2, which might modify the properties of the proposed structure.

The polycrystalline charge trapping layer 2 may have a thickness greater than 1, or greater than 5 microns, or even greater than 10 microns. Whether its thickness is greater or lesser than these limits, the charge trapping layer 2 may be composed of grains with a size of between 100 and 1000 nanometers.

Finally, and as shown in figure 1, the handle substrate 1 may optionally have a dielectric layer 5 directly on the trapping layer 2. This dielectric layer 5, which is optional, may facilitate the assembly of the handle substrate 1 with another substrate. It may for example be made of silicon oxide or silicon nitride.

For the sake of completeness, figure 2 represents a composite substrate that comprises a handle substrate 1 according to the present disclosure. As it is very apparent from that figure, the composite substrate comprises, on top of the handle substrate 1, a thin film 6, made preferably of crystalline material. For instance and without limitation, thin film 6 may be made of semiconductor material, such as silicon, or made of piezoelectric material, such as lithium tantalate (LiTaO_3), lithium niobate (LiNbO_3), lithium aluminum oxide (LiAlO_3), barium titanate (BaTiO_3), lead zirconate titanate (PbZrTiO_3), potassium niobate (KNbO_3), barium zirconate (BaZrO_3), calcium

titanate (CaTiO_3), lead titanate (PbTiO_3), potassium tantalite (KTaO_3), etc.

The structure of figure 2 may be formed in many ways from the handle substrate 1, but advantageously this formation comprises a step of transferring the thin film 6 onto the handle substrate 1. As it is well known *per se*, this transfer is usually carried out by assembling the face of a donor substrate on the handle substrate 1. This may be performed with the presence of the dielectric layer 5 or without it.

When the thin film 6 is made of piezoelectric material, its crystal orientation is chosen according to the intended application. For SAW filters made of LiTaO_3 material, it is usual to choose an orientation between 30° and 60°XY , or between 40° and 50°XY . For LiNbO_3 material, it is common to choose an orientation around 128°XY . But the invention is by no means limited to a particular crystal orientation of a piezoelectric thin film. The donor substrate may have been taken off from an ingot of ferroelectric materials such that the donor substrate presents the chosen crystal orientation. Alternatively, the donor substrate may include a thick layer of ferroelectric material assembled to a support substrate.

After this assembly step, the donor substrate is reduced in thickness in order to form the thin film 6. This reduction step can be carried out by mechanical or chemical thinning. It may also be performed by fracture at a fragile zone previously introduced into the donor substrate, for example in accordance with the principles of the Smart Cut™ technology.

Steps for finishing the thin film 6, such as a polishing step, a heat treatment under reducing or neutral atmosphere or a

sacrificial oxidation can be concatenated with the step of reduction in thickness.

When the donor substrate is a simple substrate, that is to say
5 does not comprise any integrated device, a composite substrate of the "semiconductor on insulator" type is formed, in which the thin film 6 is a layer of blank semiconductors, comprising the handle substrate 1 of the invention. The composite substrate can then be used for forming integrated devices.

10 When the donor substrate has previously been treated in order to form integrated devices on its surface, at the end of this method a thin film 6 that comprises these devices is available.

15 Manufacturing of the handle substrate 1 of the present disclosure is particularly simple and achievable with standard deposition equipment of the industry.

20 The base substrate 3 is provided and placed in a conventional deposition chamber. As it is well known *per se*, the base substrate 3 may be prepared before deposition, for example in order to eliminate a layer of native oxide from its surface. This can be performed by exposing the base substrate in the
25 chamber to a reducing atmosphere at a temperature of at least 900°C. This step is, however, not obligatory and this oxide may be kept. It is in fact sufficiently fine, from 1 to 2 nm, not to have any insulating effect (conduction through this layer by tunnel effect) insofar as future heat treatments have not made
30 it completely disappear by dissolution.

The flat surface of the silicon base substrate 3 is then exposed to a single carbon precursor gas at a pressure below atmospheric pressure, for instance comprised between 0,01 Torr and 760 Torr.

The carbon precursor gas may be composed of methane (CH_4), ethane (C_2H_6), propane (C_3H_8), acetylene (C_2H_2), ethylene (C_2H_4)... The precursor gas may be flown into the chamber (or heated into the chamber) at a temperature comprised between 700°C and 1200°C ,
5 such that carbon species nucleate onto the base substrate surface. A flow of transport gas (such as H_2) may also be introduced simultaneously into the chamber, but no other precursor gas than the carbon precursor gas is flown over the base substrate 3. By avoiding the reaction of the carbon species
10 to react with other species of a second precursor, deposition of carbon compound on the chamber wall is limited, and particles generation is avoided.

It has been surprisingly observed that when this deposition step
15 is performed under reduced carbon partial pressure (i.e. below atmospheric pressure), this nucleation of the carbon species is performed on isolated island on the surface. Silicon atoms from the base wafer diffuse then into the carbon island, forming stoichiometric or close to stoichiometric silicon carbide
20 islands of the $3\text{C}/6\text{H}$ and 4H types. The islands coalesce to form a relatively thick polycrystalline silicon carbide layer, of stoichiometric or close to stoichiometric proportion. When the flow of carbon precursor gas is maintained for a couple of minutes, the thickness of the polycrystalline layers grows to
25 multiple nm.

In a particular example, a carbon precursor gas of C_3H_8 mixed with H_2 in a proportion of 180sccm/5slm is introduced and flown for 5 minutes at a pressure of 10 torr in the chamber and heated
30 at 1000°C . A polycrystalline layer 4 of silicon carbide of 10 nm was then observed on the surface of the silicon base substrate 3.

When the deposition step is performed at or above atmospheric pressure, such as documented in WO2019002376 cited in the introduction, a completely different phenomenon is taking place on the surface of the base substrate 3. The carbon species
5 nucleate with a great density on the surface of the base wafer and block the diffusion of the silicon atoms from that surface. A crystalline or partly crystalline carbon layer then grows slowly on the surface, aligned with the silicon lattice, in a 3C structure. Such a layer presents typically a thickness of 2nm
10 after 10 minutes of deposition.

It appears therefore that flowing a single carbon precursor gas at reduced pressure over the base substrate 3 is a very effective way of forming a relatively thick (more than or equal to 10nm)
15 layer of polycrystalline silicon carbide. Such a layer is advantageous because, thanks to its polycrystalline nature, it allows to then prepare and preserve the polycrystalline nature of the charge trapping layer that is grown on top of it. Also, the relatively large thickness of the silicon carbide
20 polycrystalline layer is formed quite rapidly, and constitute an effective diffusion barrier to avoid the migration of doping species from the base wafer 3 to the charge trapping layer.

In addition, it has been observed that such a growth method,
25 under reduce pressure, was incorporating very few dopants (like boron) in the silicon carbide intermediate layer. Measures have shown a concentration of boron less than 10^{14} at/cm³ into such a silicon carbide layer. It is believed that the doping species (that may be present on the surface of the base wafer or
30 incorporated into the base wafer) are out diffused from the silicon carbide layer during its formation and evacuated from the deposition chamber with the precursor and transport gas.

After the silicon carbide polycrystalline layer has been grown onto the base substrate, the chamber has a flow of a second precursor gas travel through it, for example SiH_4 , at a temperature of around 1000°C , in order to form a polycrystalline charge trapping layer, in a conventional manner. The duration of circulation of the second precursor gas determines the thickness of the polycrystalline layer 2, and this duration may be selected such that a layer of 5 microns, 10 microns or more is grown.

Advantageously, the silicon carbide polycrystalline layer and the polycrystalline charge trapping layer are formed in situ, in the same deposition chamber. This avoid contaminating the stack of layers with dopants or contaminants from the atmosphere, and preserve the high resistivity characteristics of the handle substrate 1.

To be complete, the handle substrate 1 may be provided with a dielectric layer 5, for example a silicon oxide or silicon nitride, deposited conventionally. This insulator 4 may also be polished.

When the base substrate 3 is provided with a silicon intrinsic epitaxial layer, the formation of this layer may be realised in-situ with the formation of the silicon carbide polycrystalline layer. This approach avoids breaking the vacuum in the deposition chamber and thus improves the raw processing time and overall method efficiency. It also prevents the handle substrate to catch contaminations from the ambient atmosphere, such as particles or boron residues that may be present in the cleanroom. The two layers may also be formed in separate deposition chambers, but the chambers sharing a common transfer module. In addition to the advantage already cited, this approach of using separate chambers allows a better management of the required chambers

cleans. Obviously, it also possible to form the two layers in completely separate chambers.

5 To show the benefit of the manufacturing method, figure 3 represents a SRP measurement (spreading resistance profile) along the depth of a handle wafer according to the invention. In that particular measurement, the base wafer was a high resistivity silicon wafer (of 3500 ohm.cm), onto which a silicon
10 carbide polycrystalline layer of 10 nm, and a silicon polycrystalline charge trapping layer of 2 microns were successively grown. As it can be seen from this figure, the resistivity of the layers grown on top of the base substrate are greater than 3500 ohm.cm for its complete depth profile.

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Figure 4 represents a SRP measurement of a handle wafer made of a base substrate presenting in this case a resistivity of 4000 ohm cm. On top of this substrate a carbon layer of 2 nm, formed at atmospheric pressure and therefore mostly crystalline, and a
20 silicon polycrystalline charge trapping layer of 2 microns were successively grown. It is this time very apparent from figure 4 that the resistivity of the layers grown on top of the base substrate is reaching a low value at and close to the interface with the base substrate (less than 10 ohm.cm). Such a poor
25 resistivity is forming a conductive plane in the handle substrate, which affects the performance of the devices.

This comparative example clearly shows the interest of exposing the base substrate to a carbon single precursor at a pressure
30 below atmospheric pressure.

Of course, the invention is not limited to the embodiment described and variants of realization can be made without going beyond the scope of the invention as defined by the claims.

CLAIMS

1. A method for forming a high resistivity handle substrate for a composite substrate, the method comprising :
 - providing a base substrate made of monocrystalline silicon;
 - exposing the base substrate to a carbon single precursor at a pressure below atmospheric pressure to form a polycrystalline silicon carbide layer of at least 10 nm on the surface of the base substrate; and then
 - growing a polycrystalline charge trapping layer on the polycrystalline silicon carbide layer.
2. The method of claim 1 wherein the base substrate has a resistivity greater than 1000 ohm.cm.
3. The method of claim 1 wherein the base substrate has a resistivity smaller than 1000 ohm.cm.
4. The method of claim 3 wherein the method further comprises forming a silicon intrinsic epitaxial layer directly on the base substrate before exposing the base substrate to the carbon single precursor.
5. The method of any preceding claims, wherein the charge trapping layer has a thickness greater than 5 or 10 microns.
6. The method of any preceding claims, wherein the charge trapping layer is made of polycrystalline silicon.
7. The method of any preceding claims wherein the carbon single precursor presents a temperature comprised between 700°C and 1200°C.
8. The method of any preceding claims further comprising, exposing the base substrate to a reducing atmosphere at a temperature of at least 900°C to remove a native oxide layer

from the base substrate, before exposing the base substrate to the carbon single precursor.

9. The method of any preceding claims wherein the polycrystalline silicon carbide layer is stoichiometric.