

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR DEVICES

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464, Ellis Street, Mountain View, California 94040, United States of America, a corporation organised and existing under the laws of the States of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices.

Lateral transistors are well known and have been employed in integrated circuit technology for some time as appears for example from U.S. Patent 3,571,674. Conventional lateral transistors, however, and in particular PNP lateral transistors, have operated at frequencies much lower than desirable for modern integrated circuits. This relatively low frequency response has been substantially attributed to two factors. First, the relatively large base width of the lateral transistor increases the transit time for minority carriers passing through the base from the emitter. The relatively large base width results principally from the minimum photoresist line width consistently available during manufacture of the devices. Second, for a given amount of base impurity, the uniform base concentration profile further increases the transit time over that achievable in devices having graded base concentration profiles.

Double-diffused vertical transistors are also well known for example, from U.S. Patent 3,025,589, and U.S. Patent 3,648,125. The process by which vertical double-diffused transistors are made has several advantages over other processes, such as the mesa process. First, the base width of the transistor can be varied by controlling the diffusion processes, rather than by altering the dimensions of the masks used in

the diffusion processes. Second, the concentration profile of the base can be graded; that is, the base impurity concentration at the emitter-base junction can be made greater than the base impurity concentration at the collector-base junction. It is well known that increases in this difference for a given amount of base impurity increase the high frequency response of the transistor. See *Transistor Engineering*, by A. B. Phillips, McGraw-Hill, 1962.

In summary, prior art integrated circuits have included vertical double-diffused NPN and PNP transistors, and lateral NPN and PNP transistors with a uniform concentration of base dopant. Because the frequency response of lateral PNP transistors has been lower than desired, the prior art integrated circuits for applications requiring high frequency response have typically used (1) NPN type lateral transistors, as these are approximately three times faster than PNP type lateral transistors, or (2) complementary double-diffused vertical PNP and NPN devices on the same chip. The first alternative eliminates PNP transistors from many applications where their used would otherwise be beneficial. The second alternative involves the technology of complementary vertical double-diffused transistors—a very complicated technology resulting in many defects in the wafers, and a low yield, high cost product. Additionally, the complementary double-diffused vertical NPN and PNP transistors have large masking tolerances and thus their packing density is lower than desirable.

The invention accordingly provides a semiconductor device fabricated from semiconductor material having one surface which is substantially flat and having insulating material adjacent said surface, the top surface of said insulating material being formed substantially coplanar with

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said surface to produce an insulating border around the active regions of said semiconductor device, a collector region formed in a first portion of said semiconductor material emerging at said surface at a location within said insulating border, an emitter region formed in a second portion of said semiconductor material emerging at said surface at a location within said insulating border, with said emitter being laterally spaced from said collector, and a base region separating said emitter region from said collector region, said base region having a graded impurity concentration, and means for making electrical communication with said base region comprising a conducting channel which contacts said base region within said device and which provides electrical communication with said surface at a location exterior to said insulating border.

The insulating material may be formed by any one of a number of processes, each well known. For example, see U.S. Patent 3,648,125, cited above. The active regions of the semiconductor device of the invention may be formed in the semiconductor material utilizing a mask. This mask is formed upon the flat surface of semiconductor material and overlies portions of what are to be the emitter, base, and collector regions. The mask prevents impurities from reaching underlying semiconductor material, resists thermal oxidation, prevents thermal oxidation of the underlying semiconductor surface, resists attack by many etching solutions, and exhibits a differential etch rate when compared with SiO_2 . A typical mask material which exhibits the above characteristics is silicon nitride. Silicon nitride etches faster than silicon dioxide in hot phosphoric acid and slower than silicon dioxide in buffered hydrofluoric acid.

The invention will be readily understood from the following illustrative description and accompanying drawings, in which:

Figures 1A and 1B show a portion only of a double-diffused lateral transistor structure embodying the invention and a typical concentration profile for this transistor, respectively;

Figures 2 and 3 show cross-sectional and top views, respectively of a second embodiment of this invention comprising a double-diffused, lateral transistor structure fabricated utilizing oxide isolation and a self-aligning mask together with a photoresist mask used for forming the emitter;

Figure 4 shows a third embodiment of this invention wherein complementary PNP/NPN transistors are formed within the same isolation area;

Figure 5A shows schematically the circuit represented by the device of Figure 4;

Figure 5B shows an embodiment of this invention utilizing a plurality of the devices shown in Figure 4;

Figures 6A to 6F show a first process which does not itself produce the transistor structure of this invention, but which is included to facilitate understanding of the description relating to Figures 7A to 7I;

Figure 7A to 7I show schematically a second process, by which a transistor embodying this invention may be formed; and

Figure 8 shows a third process, for forming a transistor embodying this invention.

Figure 1A shows a portion only of a double-diffused, lateral transistor structure 11. Semiconductor material 12 having a substantially flat surface 13 is subdivided into regions of active and passive material by insulating material 16. Insulating material 16 (of which cross-sections 16A and 16B are shown) is typically formed by removing part of the semiconductor material 12 overlying the field of the semiconductor device, and oxidizing the remaining semiconductor material as disclosed in the above-mentioned U.S. Patent No. 3,648,125. However, other techniques may also be used to form insulating material 16. Insulating material 16 is an integral part of the structure 11. A feature of this invention is that the top surface of insulating material 16 is substantially coplanar with the top surface 13 of semiconductor material 12.

A collector region 17 is formed adjacent to both the flat surface and a portion of insulating material 16. A base region 22 is formed in this collector region 17 by diffusion or by ion implantation, for example. In accordance with this invention, emitter region 19 is formed in base region 22 adjacent another portion of insulating material 16 and adjacent surface 13.

Each of the emitter 19, base 22 and collector 17 regions is adjacent the flat surface 13, and the base region 22 separates the emitter region 19 from the collector region 17. Insulating region 16 serves to partially isolate the active region of the transistor 11 shown in Figure 1A from any other active devices formed in semiconductor material 12. Regions 16A and 16B form a continuous closed path abutting surface 13 and surrounding the active region of transistor 11 but leaving exposed the top surface of the active region. In addition, in some situations semiconductor material 12 will extend beneath insulation 16 to contact the bottom portions of other active regions formed in material

2. In all cases, however, electrical communication is to be provided with the base region 22 by a path extending therefrom within the device to provide an electrically conductive path to the surface 13 at a location exterior to the insulating border 16.

Figure 1B shows a concentration profile for the transistor structure 11 shown in Figure 1A when the base and emitter regions of this transistor are produced by diffusion processes. The lateral transistor structure of this invention, which has a graded base, can be formed using ion implantation techniques as well as diffusion techniques. The concentration level 28 of collector 17 is shown as a horizontal line, while the impurity concentration of the base 22 is represented by line 29, and the impurity concentration of the emitter 19 by line 27. The emitter-base junction occurs in the vicinity of point 31 corresponding to concentration level C_{EB} and distance R_{EB} . The collector-base junction occurs at point 32 and corresponds to concentration level C_{CB} and distance R_{CB} . The distance W between R_{EB} and R_{CB} is known as the base width, while the slope of a straight line connecting points 31 and 32 is called the grade constant α and is defined as $\alpha = (C_{CB} - C_{EB})/W$. It is well known that reductions in W improve the high frequency performance of the transistor, as do increases in the grade constant for a given amount of impurity in the base region. This invention utilizes both of these effects to improve the high frequency performance of lateral transistor structures over that heretofore obtained.

Figure 2 shows a double-diffused lateral transistor structure fabricated utilizing Peltzer's isolation technique described in U.S. Patent 3,648,125, and a self-aligning mask. This lateral transistor structure will be discussed for a PNP transistor; however, the discussion is made equally applicable to NPN transistors by merely reversing the conductivity type of the materials involved.

Employing Peltzer's technique, an N+ type buried layer 53 is formed at a selected location in P- type substrate 51. Then a P- type epitaxial layer 52 is formed on substrate 51. Hereinafter, substrate 51 and any attached layers of material will be called wafer 50. The PN junction 53a between substrate 51 and N type buried layer 53 terminates at field oxide isolation regions 55A and 55B. When reverse biased, this PN junction together with insulating material 55 forms a pocket in the wafer and isolates active devices within the pocket. On the surface of P- type epitaxial layer 52 is deposited a self-aligning mask 56. This mask prevents diffusion of impurities into P- type epitaxial material 52 throughout

the regions it overlies. As will be discussed, however, active semi-conductor devices may still be formed underneath mask 56 because impurities may diffuse laterally beneath its edges, for example, edge 57.

As shown in Figure 2 the base region 58 and emitter region 59 of the lateral PNP transistor are formed by diffusing the N type base 58 and the P- type emitter 59 laterally into the silicon epitaxial layer 52 beneath edge 57 of mask 56. Mask 56 may be formed from one or more materials; for example, a composite laminate layer of silicon nitride and silicon oxide (typically predominantly silicon dioxide). The choice of individual materials is based on several criteria. First, the mask materials or material must prevent the passage of, or "mask", impurities. Second, the mask material or materials must be electrically non-conductive at the interface with the semiconductor material. Third, the material or materials must resist etching in solutions used to etch compounds of semiconductor material formed by thermal oxidation. These mask materials need not be inert to the etching solution, but must only exhibit a substantially smaller etch rate than the oxide of the semiconductor material. Advantages provided by the mask 56 will be discussed in conjunction with Figure 3.

The base width of the transistor in Figure 2 is approximately equal to the difference in distance between the laterally diffused collector-base junction 58A and emitter-base junction 59A. This difference is a function of process parameters, and, in general, may be accurately controlled in a well known manner. The effective emitter-base junction area of the semiconductor device is proportional to (1) the depth of the emitter-base junction 59A, and (2) the length "e" (see Figure 3) of that portion of the mask edge 57 under which some of the emitter and base impurities travel, that is, the dimension perpendicular to the plane of the cross-section shown in Figure 2. A portion 521 (Figure 2) of P- type epitaxial layer 52 serves as the collector of the PNP lateral transistor. Electrical contact to the collector 521 of the transistor may be made at any suitable location and is shown at 522 in Figure 2. Emitter region 59 and base region 58 are terminated along isolation wall 541 which typically is formed at the same time isolation region 55 is formed.

Figure 3 shows a top view of the double-diffused, lateral, oxide-isolated transistor shown in Figure 2. The emitter region 59, base contact region 581, and collector contact region 522 are shown, surrounded at the surface of wafer 50 by field oxide insulation 55. Note that a portion of oxide 55 separates base contact 581 from emitter

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region 59. In one embodiment the self-aligning mask 56 is formed from several materials, including silicon nitride. A photoresist mask 61 is shown by a dashed line in Figure 3 in position for formation of emitter region 59 and collector contact region 522. For diffusion of the emitter region 59 and collector contact region 522, the area within dashed line 61 is exposed to a mild hydrofluoric acid etch. This removes silicon oxide films from the surface of the silicon within the opening of the photoresist mask 61 while not appreciably etching the self-aligning mask 56. The emitter region 59 and the collector contact region 522 are then formed in base region 58 and collector region 521, respectively (see Figure 2).

The particular self-aligning capability discussed above to make the opening in the photoresist mask 61 exposed both insulating material 55 and mask 56 effects that the locations of edges 57, 95 (Figure 3) of mask 56 determine the locations of the base region 58 (Figure 2), emitter region 59, and collector contact region 522. The dimensions and locations of these regions are not substantially dependent upon the position of the photoresist mask 61. Prior art devices typically depended upon accurate repositioning of photoresist masks to define the locations and sizes of the base and emitter regions. Unlike the prior art, mask 56 is not removed from the wafer 50 and then redeposited later in the manufacturing process. Thus it provides a self-aligning positional accuracy for formation of both the base and emitter regions of the transistor structure. When the base and emitter regions are formed, the positions of the collector-base junction 58A (Figure 2) and emitter-base junction 59A (Figure 2) are controlled by the impurity concentrations used in, and the duration of the processes used to form these regions. Mask 56 typically comprises silicon nitride, at least over its top surface.

Figure 4 shows a complementary PNP/NPN transistor structure formed within the same isolation area according to one embodiment of this invention. Both devices have graded base impurity concentrations. The PNP transistor structure includes emitter region 59, base region 58, and collector region 521. The NPN transistor structure includes emitter region 92, base regions 91, 521, and collector region 53. Note that the collector region 521 of the PNP transistor structure and base region 91 of the NPN transistor structure are common, as are the PNP base region 58 and the NPN collector region 53. Region 94 is the electrical contact for both the PNP base region 58 and the NPN collector region 53. Figure 5A shows the

transistor structure of Figure 4 schematically.

The complementary PNP/NPN transistor structure formed in accordance with this invention provides substantial advantages over the prior art. First, the complementary PNP/NPN structure allows very high packing densities because the addition of the NPN transistor consumes no extra space over that required for just the PNP transistor. This results directly from the formation of a part of the NPN base region 91 and formation of the NPN emitter region 92 approximately at the location which would be the PNP collector contact in a non-complementary embodiment of the invention. This advantage can readily be seen by comparing Figure 4 with Figure 2. Another advantage of the complementary PNP/NPN structure is that it may be formed very simply once the PNP transistor structure is fabricated. Once the PNP structure is formed only one extra manufacturing operation is necessary, that of forming the NPN emitter region 92 and NPN collector region-PNP base region contact 94. Note that the NPN base region 91 is formed at the same time the PNP emitter region 59 is formed. During formation of the NPN base region 91 and NPN emitter region 92 the edge 95 of mask 56 will perform a self-aligning function similar to that described above in conjunction with edge 57 of mask 56.

A further advantage of the complementary PNP/NPN transistor structure according to this invention is its compatibility for inclusion in semiconductor devices which utilize arrays of complementary transistors. The ease with which arrays of complementary PNP/NPN transistor structures may be formed is shown in Figure 5B. A portion of a wafer 400 is shown on which a plurality of complementary PNP/NPN transistor structures are formed. In Figure 5b, five pairs of complementary devices are shown for illustrative purposes only. Each of the devices shown in plan view in Figure 5B has the cross-section shown in Figure 4. A typical embodiment according to this invention employing an array of complementary PNP/NPN transistors may contain any number of such structures, for example, several thousand.

In Figure 5B the complementary transistor structures are formed at intersections of buried layers 53R-V with other regions formed in the wafer 400. Each of the buried layers 53R-V acts as a common PNP base-NPN collector. Also shown in Figure 5B are the self-aligned mask 56, PNP emitter region 59, a metal contact 403 to the PNP emitter region 59, NPN emitter region 92, and a metal contact

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405 to the NPN emitter region 92. Electrical contacts to other regions of the PNP/NPN complementary structure are not shown in Figure 5B; however, they could be made at any suitable location on wafer 400. The five pairs of complementary transistor structures are thus formed approximately at the intersections of emitter regions 59, 92 with the top surface of the semiconductor material. The PNP base region and the NPN base region are not shown, however, they separate the PNP emitter and collector regions and the NPN emitter and collector regions.

Figures 6A through 6F show one process which does not itself produce the transistor structure of this invention but which is included to facilitate understanding of the description relating to Figures 7A—7I. This process will be illustrated for a non-oxide isolated, lateral, double-diffused PNP transistor, although it should be noted the process may be used to form similar NPN structures.

1. Oxidize a P type silicon substrate wafer 51 to form a silicon dioxide impurity diffusion mask (Figure 6A, layer 101).

2. Form an opening 100 in the silicon dioxide layer 101 where the buried N-type layer is desired.

3. Form the buried layer 53 using an N+ predeposition.

4. Remove the oxide 101 from the surface of the substrate 51.

5. Grow a P type epitaxial layer (Figure 6B, layer 52).

6. Form a mask 104 on the surface of P type epitaxial layer 52. Mask 104 is comprised of material meeting the specifications set forth herein, and in one embodiment is silicon nitride.

7. Utilizing photo masking techniques, define openings in mask 104 which will be the emitter/base diffusion opening 105, the base contact opening 106, and the collector contact opening 107.

8. Oxidize the wafer to form a silicon dioxide film over the exposed silicon surface. This film will serve as an impurity diffusion mask (layers 108, 109, 110, Figure 6B).

9. Form the emitter/base mask 111 using well known photoresist material. Note this is an oversize mask, that is, the edges of the mask do not define the openings discussed in step 7 above. Remove oxide 110, 108 from emitter/base region 105 and base contact region 106 (Figure 6C).

10. Form the base region predeposition using N-type impurity (not shown).

11. Perform the base diffusion 112 (Figure 6D) at an elevated temperature, thereby causing the base impurity to contact the N+ buried layer 53 (Figure 6D).

During this operation silicon dioxide films 113, 115, 116 are formed.

12. Form the emitter and collector mask 114 using well-known photoresist material. Note this is also an oversized mask. Remove the silicon dioxide 115, 116 shown in Figure 6D.

13. Form the collector contact 117 and emitter 118 (Figure 6E) predepositions and oxidize the wafer (layers 119, 120, 121 in Figure 6E).

14. Remove oxide 119, 120, 121 to allow electric contact to be made to emitter region 118, base region 112A, and collector region 117.

15. Deposit and define metal contacts (122, Figure 6F).

The above-described process uses one masking layer 104 to form the collector, base and emitter regions 52A, 112B and 118, respectively, of a lateral, double-diffused PNP transistor with a graded base. Isolation is provided by backbiasing the PN junction between P regions 51, 52 and N type regions 112A, 112B and 53 (Figure 6E). Buried layer 53 serves as a low resistance contact to base region 112B. Of interest, if the cross-section shown in Figure 6F is rotated 360 degrees about a vertical line through the center of the emitter region, a circular structure is obtained with the emitter at the center, surrounded by the base region which in turn is surrounded by the collector region. The low resistivity buried N region underlies the structure and a circular base sink region surrounds the collector. In other words, the cross-section shown in Figure 6F to the left of a vertical centreline through the centre of the emitter region represents the cross-section of one half of a disk-shaped structure.

A second process, by which the transistor of this invention may be formed, utilizes, in part, the process of Peltzer, previously cited herein, to form the isolation regions. This process results in a double-diffused, lateral, oxide-isolated PNP structure. The steps of this process are as follows:

1. Follow steps 1—6 of the first process just discussed.

2. Remove mask 104 from everywhere on the surface of P-type epitaxial layer 52 except where the transistor structure of this invention is desired.

3. Oxidize the wafer to grow an impurity-diffusion masking layer 201 of silicon dioxide (Figure 7A).

4. Mask the base region using a photoresist mask 205 which overlaps the mask 104. Remove the exposed silicon dioxide.

5. Remove mask 205. Form the base region 206 N-type predeposition into the exposed silicon surface (Figures 7B, 7C).

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6. Remove the thermal oxide 201 (Figure 7C).

7. Deposit a second mask of a material with characteristics similar or identical to the material of mask 104, i.e., silicon nitride (Figure 7C, layer 207).

8. Using photomasking techniques, define mask 207 into islands as described in Peltzer (Figure 7D is a top view, while 7E is a cross-sectional view).

9. Etch the exposed silicon to a depth approximately equal to one-half the epitaxial layer 52 thickness using a solution which does not appreciably etch the mask 104 or mask 207 (see Figure 7F).

10. Oxidize the silicon to the extent that the upper surface of the silicon dioxide 208 corresponds substantially to the plane of the original silicon surface. The lower surface of the silicon dioxide film 208 should intersect the buried N⁺ layer 53. During this oxidation, N-type region 206 diffuses downward to meet the upward diffusing N⁺ buried layer 53 (Figure 7G).

11. Remove mask 207 leaving mask 104 intact.

12. Reoxidize the wafer to grow a thin protective oxide layer 209 (Figure 7H).

13. Use an oversized photoresist mask 212 to expose the silicon in emitter 210 and collector 211 contact regions. Etch through the layer 209 of the silicon dioxide (Figure 7H).

14. Form with a P-type impurity emitter region 213 and collector contact region 214. Remove the silicon dioxide 209 covering base contact region 206 (Figure 7I).

15. Form metal contacts 216A, 216B and 216C (or contacts of any other suitable conductive material) to the emitter, base, and collector regions, respectively.

The resulting structure shown in cross-section in Figure 7I, is similar to, and has the features and advantages of the structure shown in Figure 2.

A third process, for fabricating the transistor structure of this invention, utilizes ion implantation techniques. The steps of this process are as follows:

1. Follow steps 1—6 under the previously discussed first process. Figure 8 shows the mask 304 of silicon nitride, epitaxial layer 52, N⁺ buried layer 53 and substrate 51 as they will appear at the completion of this step.

2. Using chemical vapor deposition (CVD) deposit a silicon dioxide layer 301 (Figure 8) sufficiently thick to mask against the high energy ions which will later be used to implant impurities below the interface of mask 304 and silicon 52. (The CVD process is used as an example. Other processes utilizing other material could be used to form this layer).

3. Etch away the silicon dioxide layer 301

from everywhere except where the transistor structure is desired. The mask 304 is not etched at this time.

4. Form a photoresist mask 306 (Figure 8) over all regions of wafer 300 except those which are to receive the base impurity, that is, region 307. This layer is of sufficient thickness and density to prevent passage of impurity ions during ion implantation.

5. Implant the base N-type impurity into the wafer 300 surface. The implant energy is selected to make the peak of the impurity distribution fall below mask layer 304 in region 310 of silicon 52. The mask layer 304 is not appreciably altered by this step. The peak of the implanted impurity distribution is shown as lines of crosses 310 in Figure 8.

6. Remove photoresist layer 306.

7. Perform steps 8 through 15 of the second process (mask 304 of the third process functions as mask 207 of the second process, while mask 301 of the third process functions as mask 104 of the second process. Base region 310 of the third process is equivalent to base region 206 of the second process, except in the manner in which it is formed).

The invention can be equally well embodied in transistors and semiconductor devices of opposite conductivity types to those particular examples discussed herein. In other words, it should be understood that in Figure 3, for example, the conductivity type of each material could be reversed, thereby forming an NPN transistor, rather than a PNP transistor. It should also be noted that while this invention has been discussed in conjunction with silicon semiconductor device technology, it is equally applicable to semiconductor devices formed from other materials.

This invention has been described as using a mask of a material such as silicon nitride which etches at a different rate in a given etch than does silicon dioxide. However, instead of using silicon nitride for the mask such as mask 56 (Figure 2), silicon dioxide formed to a greater thickness than the adjacent layers of silicon dioxide formed on the device can be used as the mask. In this situation, mask 56 must be at least thick enough to allow the silicon dioxide on adjacent portions of the top surface of the wafer to be removed while still leaving a thick enough layer of silicon dioxide on the surface to mask the impurities to be diffused or otherwise placed in the underlying semiconductor material.

Attention is hereby drawn to our copending Patent Application No. 364414/76 (Serial No. 1,470,212) that is directed to a method of fabricating a semiconductor device such as hereinbefore described.

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WHAT WE CLAIM IS:—

1. A semiconductor device fabricated from semiconductor material having one surface which is substantially flat and having insulating material adjacent said surface, the top surface of said insulating material being formed substantially coplanar with said surface to produce an insulating border around the active regions of said semiconductor device, a collector region formed in a first portion of said semiconductor material emerging at said surface at a location within said insulating border, an emitter region formed in a second portion of said semiconductor material emerging at said surface at a location within said insulating border, with said emitter being laterally spaced from said collector, and a base region separating said emitter region from said collector region, said base region having a graded impurity concentration, and means for making electrical communication with said base region comprising a conducting channel which contacts said base region within said device and which provides electrical communication with said surface at a location exterior to said insulating border.

2. A semiconductor device as claimed in claim 1 in which the base region extends from said surface, between said emitter and collector and underneath said emitter to abut said insulating material.

3. A semiconductor device as claimed in claim 2 having additional insulating material formed adjacent said exterior location on said surface, the top surface of said additional insulating material being substantially coplanar with said surface to electrically isolate said exterior location at which said conducting channel contacts

said surface from other semiconductor devices fabricated in said semiconductor material.

4. A semiconductor device as claimed in claim 1, 2 or 3 in which said collector region is composed of P-conductivity type material, said base region is composed of N conductivity type material, and said emitter region is composed of P+ conductivity type material.

5. A semiconductor device as claimed in claim 1, 2 or 3 having an additional region of conductivity type opposite to the conductivity type of said collector region formed adjacent said collector region and emerging at said surface at a location within said insulating border, said additional region having a means for making electrical communication therewith.

6. A semiconductor device as claimed in claim 5 in which said emitter region is of P+ conductivity type, said base region is of N- conductivity type, said collector region is of P- conductivity type, and said additional region is of N+ conductivity type.

7. A semiconductor device as claimed in claim 1 and substantially as herein described with reference to Figures 1A and 1B, Figures 2 and 3, Figure 4, Figure 5, or Figure 7I of the accompanying drawings.

8. A method of fabricating a semiconductor device as claimed in claim 1 substantially as herein described with reference to Figures 7A to 7I or Figure 8 of the accompanying drawings.

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