

~~WHAT IS CLAIMED IS~~ CLAIMS:

1. A semiconductor wafer imaging system for imaging a semiconductor wafer, the system comprising:

shroud panels defining a black box;

a camera positioned in the black box for imaging the semiconductor wafer;

a flat mirror to reflect diffuse light to the camera; and

an illumination panel for directing the diffuse light to the semiconductor wafer, wherein a portion of the diffuse light is reflected off the semiconductor wafer and the camera images the semiconductor wafer by detecting the reflected diffuse light.

2. The system of claim 1, further comprising a controller for analyzing images generated by the camera, wherein the controller detects defects in the semiconductor wafer.

~~3. The system of claim 1, further comprising a flat mirror to reflect the diffuse light to the camera.~~

43. The system of claim ~~3~~2, wherein the shroud panels include black anodized aluminum panels to minimize reflections in the black box.

54. The system of claim 3, wherein the shroud panels define an upper chamber and a lower chamber, a support plate separates the upper chamber from the lower chamber, a bottom shroud panel at least partially defines the lower chamber and defines a wafer opening, the support plate defines a camera opening, wherein the diffuse light is transmitted to the semiconductor wafer through the wafer

opening, and wherein the reflected diffuse light is transmitted from the semiconductor wafer to the camera through the wafer opening and the camera opening.

65. The system of claim 54, wherein the illumination panel is positioned in the lower chamber.

76. The system of claim 5, further comprising an end effector to position the semiconductor wafer in the wafer opening.

87. The system of claim 76, further comprising an end effector positioner attached to the black box for calibrating a position of the end effector, wherein the end effector positioner is detachable from the black box after the position of the end effector has been calibrated.

98. The system of claim 54, wherein the camera and the flat mirror are positioned in the upper chamber.

109. The system of claim 98, further comprising a slide lock attached to the camera for positioning the camera in the upper chamber.

110. The system of claim 98, further comprising a mirror positioning system attached to the flat mirror for positioning the flat mirror in the upper chamber.

1211. The system of claim 910, wherein a filter is positioned in the upper chamber and covers the camera opening.

1312. The system of claim 98, wherein a filter is attached to the camera and covers a lens of the camera.

~~14~~13. The system of claim 1, further comprising a locating plate attached to the black box for positioning the black box.

~~15~~14. A black box for imaging a semiconductor wafer, the black box comprising:

shroud panels defining an upper chamber and a lower chamber, a support plate separates the upper chamber from the lower chamber, a bottom shroud panel at least partially defines the lower chamber and defines a wafer opening, the support plate defines a camera opening;

a camera positioned in the upper chamber for imaging the semiconductor wafer; and

an illumination panel for directing diffuse light to the semiconductor wafer, wherein the diffuse light is transmitted to the semiconductor wafer through the wafer opening, and wherein a portion of the diffuse light is reflected off the semiconductor wafer through the wafer opening and the camera opening and the camera images the semiconductor wafer by detecting the reflected diffuse light.

~~16~~15. The black box of claim ~~15~~14, wherein the diffuse light is transmitted to the semiconductor wafer through the wafer opening, and wherein the reflected diffuse light is transmitted from the semiconductor wafer to the camera through the wafer opening and the camera opening.

~~17~~16. The black box of claim ~~15~~14, wherein the illumination panel is positioned in the lower chamber.

~~18~~17. The black box of claim ~~15~~14, wherein the camera and a flat mirror are positioned in the upper chamber.

~~19~~18. The black box of claim ~~18~~17, further comprising a slide lock attached to the camera for positioning the camera in the upper chamber.

~~20~~19. The black box of claim ~~18~~17, further comprising a mirror positioning system attached to the flat mirror for positioning the flat mirror in the upper chamber.

20. The black box of claim 14, wherein a filter is attached to the camera and covers a lens of the camera.

~~21. A semiconductor wafer processing system for processing a semiconductor wafer, the system comprising:~~

~~a semiconductor wafer processing station for processing the semiconductor wafer; and~~

~~a semiconductor wafer imaging system for imaging a semiconductor wafer, wherein the semiconductor wafer imaging system images the semiconductor wafer after the semiconductor wafer processing station processes the semiconductor wafer, the system comprising:~~

~~shroud panels defining a black box;~~

~~a camera positioned in the black box for imaging the semiconductor wafer; and~~

~~an illumination panel for directing diffuse light to the semiconductor wafer, wherein a portion of the diffuse light is reflected off the semiconductor~~

~~wafer and the camera images the semiconductor wafer by detecting the reflected diffuse light.~~

~~22. The system of claim 21, wherein the semiconductor wafer processing station includes a cleaving station and the semiconductor wafer imaging system is positioned above the cleaving station.~~

~~23. The system of claim 22, wherein the cleaving station is positioned upstream of the semiconductor wafer imaging system.~~

~~24. The system of claim 21 further comprising a semiconductor wafer imaging station, wherein the semiconductor wafer imaging system is positioned in the semiconductor wafer imaging station.~~

~~25. The system of claim 21 further comprising a frame and a locating plate attached to the frame, wherein the semiconductor wafer imaging system is attached to the locating plate.~~

~~26. The system of claim 25, wherein the semiconductor wafer imaging system is movably attached to the locating plate and a position of the semiconductor wafer imaging system is adjusted by adjusting the position of the semiconductor wafer imaging system on the locating plate.~~

~~27. The system of claim 25, further comprising an end effector attached to the frame for position the semiconductor wafer within a field of view of the camera.~~

~~28. The system of claim 27, wherein the end effector receives the semiconductor wafer from the semiconductor wafer processing station.~~

~~29. A semiconductor wafer processing system for processing a semiconductor wafer, the system comprising:~~

~~a first manufacturing line for processing a first semiconductor wafer and including a first semiconductor wafer processing station for processing the first semiconductor wafer;~~

~~a second manufacturing line for processing a second semiconductor wafer and including a second semiconductor wafer processing station for processing the second semiconductor wafer, the second manufacturing line intersects the first manufacturing line at a common location;~~

~~a semiconductor wafer imaging system for imaging the first and second semiconductor wafers and positioned within the common location where the first and second manufacturing lines intersect, wherein the semiconductor wafer imaging system images the first and second semiconductor wafers after the first and second semiconductor wafer processing stations process the first and second semiconductor wafers, the system comprising:~~

~~shroud panels defining a black box;~~

~~a camera positioned in the black box for imaging the semiconductor wafer; and~~

~~an illumination panel for directing diffuse light to the semiconductor wafer, wherein a portion of the diffuse light is reflected off the semiconductor wafer and the camera images the semiconductor wafer by detecting the reflected diffuse light.~~

~~30. The system of claim 29, wherein at least one of the first and second semiconductor wafer processing stations includes a cleaving station.~~

~~31. The system of claim 30, wherein the cleaving station is positioned upstream of the semiconductor wafer imaging system.~~

~~32. The system of claim 29 further comprising a semiconductor wafer imaging station positioned within the common location where the first and second manufacturing lines intersect, wherein the semiconductor wafer imaging system is positioned in the semiconductor wafer imaging station.~~

~~33. The system of claim 29 further comprising a frame and a locating plate attached to the frame, wherein the semiconductor wafer imaging system is attached to the locating plate.~~

~~34. The system of claim 33, wherein the semiconductor wafer imaging system is movably attached to the locating plate and a position of the semiconductor wafer imaging system is adjusted by adjusting the position of the semiconductor wafer imaging system on the locating plate.~~

~~35. The system of claim 33, further comprising an end effector attached to the frame for positioning the first and second semiconductor wafers within a field of view of the camera.~~

~~36. The system of claim 35, wherein the end effector receives the semiconductor wafer from at least one of the first and second semiconductor wafer processing stations.~~

~~37. The system of claim 29, wherein the semiconductor wafer imaging system is positioned downstream of the first and second semiconductor wafer processing~~

~~stations and alternates between imaging the first and second semiconductor wafers from the first and second manufacturing lines.~~

~~38. A semiconductor wafer imaging station of a semiconductor wafer processing system for imaging a semiconductor wafer, the station comprising:~~

~~a frame;~~

~~a locating plate attached to the frame;~~

~~a black box movably attached to the locating plate, the black box comprising:~~

~~shroud panels defining the black box;~~

~~a camera positioned in the black box for imaging the semiconductor wafer; and~~

~~an illumination panel for directing diffuse light to the semiconductor wafer, wherein a portion of the diffuse light is reflected off the semiconductor wafer and the camera images the semiconductor wafer by detecting the reflected diffuse light; and~~

~~an end effector for positioning the semiconductor wafer within a field of view of the camera.~~

~~39. The station of claim 38, wherein a position of the black box is adjusted by adjusting the position of the black box on the locating plate.~~

~~40. The station of claim 38, wherein the end effector is attached to the frame and positions the semiconductor wafer within a field of view of the camera.~~

~~41. A method of detecting defects on a semiconductor wafer, the method comprising:~~

~~directing diffuse light to the semiconductor wafer;~~

~~reflecting the diffuse light off of the semiconductor wafer;~~

~~detecting the diffuse light with a camera to generate an image of the semiconductor wafer; and~~

~~analyzing the image to detect defects on the semiconductor wafer.~~

~~42. The method of claim 41, wherein analyzing the image to detect defects on the semiconductor wafer comprises:~~

~~detecting a wafer boundary of the semiconductor wafer by segmenting and isolating the wafer boundary in the image; and~~

~~detecting a transfer layer boundary of a transfer layer on the semiconductor wafer by segmenting and isolating the transfer layer boundary in the image.~~

~~43. The method of claim 42, wherein analyzing the image to detect defects on the semiconductor wafer further comprises:~~

~~analyzing the transfer layer of the semiconductor wafer in the image; and~~

~~detecting defects in the transfer layer of the semiconductor wafer.~~

~~44. The method of claim 42, wherein the wafer boundary and the transfer layer boundary define a terrace width therebetween, and wherein analyzing the image to detect defects on the semiconductor wafer further comprises~~

~~analyzing the terrace width to generate terrace width statistics.~~

~~45. The method of claim 42, wherein analyzing the image to detect defects on the semiconductor wafer further comprises quantifying the detected defects into quantified metrics.~~

~~46. A method of processing a semiconductor wafer, the method comprising:~~

~~cleaving the semiconductor wafer in a cleaving station;~~

~~positioning the semiconductor wafer within a field of view of a camera;~~

~~directing diffuse light to the semiconductor wafer;~~

~~reflecting the diffuse light off of the semiconductor wafer;~~

~~detecting the diffuse light with the camera to generate an image of the semiconductor wafer; and~~

~~analyzing the image to detect defects on the semiconductor wafer.~~

~~47. The method of claim 46, wherein analyzing the image to detect defects on the semiconductor wafer comprises:~~

~~detecting a wafer boundary of the semiconductor wafer by segmenting and isolating the wafer boundary in the image; and~~

~~detecting a transfer layer boundary of a transfer layer on the semiconductor wafer by segmenting and isolating the transfer layer boundary in the image.~~

~~48. The method of claim 47, wherein analyzing the image to detect defects on the semiconductor wafer further comprises:~~

~~analyzing the transfer layer of the semiconductor wafer in the image; and~~

~~detecting defects in the transfer layer of the semiconductor wafer.~~

~~49. The method of claim 47, wherein the wafer boundary and the transfer layer boundary define a terrace width therebetween, and wherein analyzing the image to detect defects on the semiconductor wafer further comprises analyzing the terrace width to generate terrace width statistics.~~

~~50. The method of claim 47, wherein analyzing the image to detect defects on the semiconductor wafer further comprises quantifying the detected defects into quantified metrics.~~

~~51. A method of processing a semiconductor wafer using a semiconductor wafer processing system, the semiconductor wafer processing system includes a processing station and a semiconductor wafer imaging station, the method comprising:~~

~~processing the semiconductor wafer in the processing station;~~

~~positioning the semiconductor wafer within a field of view of a camera of the semiconductor wafer imaging station;~~

~~directing diffuse light to the semiconductor wafer;~~

~~reflecting the diffuse light off of the semiconductor wafer;~~

~~detecting the diffuse light with the camera to generate an image of the semiconductor wafer; and~~

~~analyzing the image to detect defect on the semiconductor wafer.~~

~~52. The method of claim 51, wherein analyzing the image to detect defect on the semiconductor wafer comprises:~~

~~detecting a wafer boundary of the semiconductor wafer by segmenting and isolating the wafer boundary in the image; and~~

~~detecting a transfer layer boundary of a transfer layer on the semiconductor wafer by segmenting and isolating the transfer layer boundary in the image.~~

~~53. The method of claim 52, wherein analyzing the image to detect defect on the semiconductor wafer further comprises:~~

~~analyzing the transfer layer of the semiconductor wafer in the image; and~~

~~detecting defect in the transfer layer of the semiconductor wafer.~~

~~54. The method of claim 52, wherein the wafer boundary and the transfer layer boundary define a terrace width therebetween, and wherein analyzing the image to detect defect on the semiconductor wafer further comprises analyzing the terrace width to generate terrace width statistics.~~

~~55. The method of claim 52, wherein analyzing the image to detect defect on the semiconductor wafer further comprises quantifying the detected defect into quantified metrics.~~

~~56. A method of processing a semiconductor wafer using a semiconductor wafer processing system, the semiconductor wafer processing system includes a first manufacturing line, a second manufacturing line, and a semiconductor wafer imaging station positioned within a common location where the first and second manufacturing lines intersect, the first and second manufacturing lines each include processing stations for processing the semiconductor wafer, the method comprising:~~

~~i) processing a first semiconductor wafer in the processing station of the first manufacturing line;~~

~~ii) positioning the first semiconductor wafer within a field of view of a camera of the semiconductor wafer imaging station;~~

~~iii) directing diffuse light to the first semiconductor wafer;~~

~~iv) reflecting the diffuse light off of the first semiconductor wafer;~~

~~v) detecting the diffuse light with the camera to generate an image of the first semiconductor wafer; and~~

~~vi) analyzing the image to detect defect on the first semiconductor wafer;~~

~~vii) processing a second semiconductor wafer in the processing station of the second manufacturing line;~~
~~and~~

~~viii) repeating steps ii through vi to image the second semiconductor wafer.~~

~~57. The method of claim 56, wherein analyzing the image to detect defect on the semiconductor wafer comprises:~~

~~detecting a wafer boundary of the semiconductor wafer by segmenting and isolating the wafer boundary in the image; and~~

~~detecting a transfer layer boundary of a transfer layer on the semiconductor wafer by segmenting and isolating the transfer layer boundary in the image.~~

~~58. The method of claim 57, wherein analyzing the image to detect defect on the semiconductor wafer further comprises:~~

~~analyzing the transfer layer of the semiconductor wafer in the image; and~~

~~detecting defect in the transfer layer of the semiconductor wafer.~~

~~59. The method of claim 57, wherein the wafer boundary and the transfer layer boundary define a terrace width therebetween, and wherein analyzing the image to detect defect on the semiconductor wafer further comprises analyzing the terrace width to generate terrace width statistics.~~

~~60. The method of claim 57, wherein analyzing the image to detect defect on the semiconductor wafer further comprises quantifying the detected defect into quantified metrics.~~