CLAIM

What is claimed is:

1. A circuit package comprising:

an electronic integrated circuit comprising a plurality of processing elements, each processing element comprising a message router including photonic-channel interfaces; and

a plurality of bidirectional photonic channels connecting the processing elements into an electro-photonic network, each bidirectional photonic channel interfacing at a first end with a photonic-channel interface of the message router of a first one of the processing elements and at a second end with a photonic-channel interface of the message router of a second one of the processing elements and being configured to optically transfer a packet between the message routers of the first and second processing elements,

wherein each bidirectional photonic channel comprises one or more unidirectional photonic links in both directions, and

wherein each unidirectional photonic link comprises an optical modulator at an input end, a photodetector at an output end, and an optical waveguide connecting the optical modulator to the photodetector, and wherein each photonic-channel interface comprises a modulator driver for each unidirectional photonic link with which it interfaces at the input end and a transimpedance amplifier for each unidirectional photonic link with which it interfaces at the output end.

~~2. The circuit package of claim 1, wherein each bidirectional photonic channel comprises one or more unidirectional photonic links in both directions.~~

~~3~~2. The circuit package of claim ~~2~~1, wherein each bidirectional photonic channel comprises multiple unidirectional photonic links in both directions, and wherein the multiple unidirectional photonic links in each direction are bonded together.

~~4. The circuit package of claim 2, wherein each unidirectional photonic link comprises an optical modulator at an input end, a photodetector at an output end, and an optical waveguide connecting the optical modulator to the photodetector, and wherein each photonic channel interface comprises a modulator driver for each unidirectional photonic link with which it interfaces at the input end and a transimpedance amplifier for each unidirectional photonic link with which it interfaces at the output end.~~

~~5~~3. The circuit package of claim ~~4~~1, wherein the optical modulators are electro-absorption modulators (EAMs).

~~6~~4. The circuit package of claim ~~4~~1, wherein the optical modulators comprise at least one of a ring modulator, Mach-Zehnder modulator, quantum-confined Stark effect (QCSE) electro-absorption modulator.

~~7~~5. The circuit package of claim ~~4~~1, wherein the electronic integrated circuit is implemented in an electronic circuit layer and the plurality of bidirectional photonic channels are implemented in a photonic circuit layer.

~~8~~6. The circuit package of claim ~~7~~5, wherein the electronic circuit layer is implemented in a first semiconductor chip and the photonic circuit layer is implemented in a second semiconductor chip.

~~9~~7. The circuit package of claim ~~7~~5, wherein each modulator driver is placed directly above or below the optical modulator with which it is associated and each transimpedance amplifier is placed directly above or below the photodetector with which it is associated.

~~10~~8. The circuit package of claim ~~8~~6, wherein distances between the optical modulators and their associated modulator drivers and between the photodetectors and their associated transimpedance amplifiers are smaller than 200 μm.

~~11~~9. The circuit package of claim ~~8~~6, further comprising, in the photonic circuit layer of the semiconductor chip, optical input waveguides supplying optical carrier signals provided by one or more laser light sources to the optical modulators of the photonic links, the optical carrier signals being modulated by the optical modulators in accordance with drive signals applied by the associated modulator drivers to generate modulated optical signals carrying the packet.

~~12~~10. The circuit package of claim ~~11~~9, further comprising the one or more laser light sources integrated into the circuit package.

~~13~~11. The circuit package of claim ~~12~~10, wherein the one or more laser light sources are integrated with the optical input waveguides in one or more photonic integrated circuits (PICs) in the photonic circuit layer.

~~14~~12. The circuit package of claim ~~12~~10, wherein the one or more laser light sources are implemented in an interposer co-packaged with the semiconductor chips and are edge-coupled with one or more PICs in the photonic circuit layer that include the optical input waveguides.

~~15~~13. The circuit package of claim ~~11~~9, wherein the one or more laser light sources are implemented externally to the circuit package and optically coupled via one or more optical fibers to one or more PICs in the circuit package.

~~16~~14. The circuit package of claim ~~15~~13, wherein the one or more optical fibers are coupled to the one or more PICs via one or more fiber attach units (FAUs) located over grating couplers implemented in the PICs.

~~17~~15. The circuit package of claim ~~15~~13, wherein the one or more optical fibers are edge-coupled to the one or more PICs.

~~18~~16. The circuit package of claim ~~15~~13, further comprising, in the photonic circuit layer of the semiconductor chip, one or more optical splitters each splitting an input optical carrier signal received from an associated one of the

one or more laser light sources between multiple of the input optical waveguides.

~~19~~17. The circuit package of claim 1, wherein the electronic integrated circuit is an application-specific integrated circuit (ASIC).

~~20~~18. The circuit package of claim ~~19~~17, wherein the ASIC comprises digital and mixed-signal electronic circuitry.

~~21~~19. The circuit package of claim ~~19~~17, wherein each processing element further comprises a dot product engine implementing a combinatorial tree of multipliers and adders for computing dot products between vectors.

~~22~~20. The circuit package of claim ~~21~~19, wherein each processing element further comprises a tensor engine for obtaining and processing vectors computed as output of the dot product engine.

~~23~~21. The circuit package of claim ~~21~~19, wherein each processing element further comprises a memory system.

~~24~~22. The circuit package of claim ~~19~~17, further comprising at least one of a peripheral component interconnect express (PCIE) interface, an advanced RISC machine core, an image processor, or an external memory controller.

~~25~~23. The circuit package of claim ~~19~~17, further comprising high bandwidth memory (HBM), the ASIC further comprising a RAM controller communicatively coupling the processing elements to the HBM.

~~26~~24. The circuit package of claim 1, wherein the message routers of the processing elements are configured to route a packet -having routing information in a portion of the packet, wherein a path through the electro-photonic network is determined by using the routing information.

~~27~~25. The circuit package of claim ~~26~~ 24 wherein the message router of each processing element is configured to determine, based on the routing information in the packet received on one of its photonic-channel interfaces, a destination of the packet, and to route the packet either to a local port if the destination is a local memory or a processing engine within the processing element or to another one of the photonic-channel interfaces if the destination is not the local memory or processing engine within the processing element.

~~28~~26. The circuit package of claim ~~26~~24, wherein the processing elements are arranged in a regular grid, and wherein the routing information in the packet specifies relative locations in first and second dimensions along the grid to a processing element that is a destination of the packet.

~~29~~27. The circuit package of claim ~~28~~26, wherein each bidirectional photonic channels connects a pair of immediately adjacent processing elements in the grid in one of the first dimension or the second dimension, and wherein the message router of each processing element is configured to decrement a value in the routing information associated with the relative location in the first dimension when routing the packet to an immediately adjacent processing element along the first dimension and to decrement a value in the routing information associated with the relative location in the second dimension when routing the packet to an immediately adjacent processing element along the second dimension.

~~30~~28. The circuit package of claim ~~26~~24, wherein the plurality of bidirectional photonic channels are configured to connect the processing elements into an electro-photonic network having a grid topology defining at least two dimensions, wherein the routing information in the packet specifies coordinates in the at least two dimensions relative to a processing element that is a destination of the packet, and wherein the message router of each processing element, when routing the packet to a topologically immediately adjacent processing element along one of the at least two dimensions, modifies the routing information in the packet by decrementing a value associated with one of the at least two dimensions.

~~31~~29. The circuit package of claim 1, wherein the electronic circuit is configured as an arrangement of tiles each corresponding to one of the processing elements .

~~32~~30. The circuit package of claim ~~31~~29, wherein the tiles are rectangular tiles arranged in a rectangular grid.

~~33~~31. The circuit package of claim ~~32~~30, wherein the plurality of bidirectional photonic channels is configured to directly connect each pair of immediately adjacent tiles in the rectangular grid to result in a quadrilateral mesh topology of the electro-photonic network.

~~34~~32. The circuit package of claim ~~33~~31, wherein the plurality of bidirectional photonic channels is configured to further directly connect one or more pairs of non-adjacent tiles in the rectangular grid.

~~35~~33. The circuit package of claim ~~33~~31, further comprising bidirectional photonic channels configured to directly connect pairs of tiles on opposite edges of the rectangular grid to result in a wrapped toroidal mesh topology of the electro-photonic network.

~~36~~34. The circuit package of claim 1, wherein the bidirectional photonic channels are configured to connect the processing elements into an electro-photonic network having a cubic grid topology.

~~37. A method comprising:~~

~~at a first electronic processing element of an electro-photonic network, generating an electronic packet having a header and a payload, the header or a portion of the payload comprising routing information associated with a destination electronic processing element of the electro-photonic network;~~

~~determining, based on the routing information, a path from the first electronic processing element to the destination electronic processing element via one or more intermediate electronic processing elements of the electro-~~

photonic network, wherein the first, destination, and intermediate processing elements are connected by associated photonic channels;

at the first processing element, routing the packet to a port connected via one of the photonic channels to a first intermediate processing element along the path, and transforming the packet from an electronic signal to an optical signal for transmission to the first intermediate processing element;

at each of the one or more intermediate processing elements, transforming the optical signal back into an electronic signal, routing the electronic signal to a port connected via one of the photonic channels to a processing element, among the intermediate processing elements and the destination processing elements, that is next along the path, and transforming the electronic signal into an optical signal for transmission to the processing element that is next along the path; and

at the destination processing element, transforming the optical signal back into an electronic signal.

38. The method of claim 37, wherein transforming each electronic signal into an optical signal comprises operating a modulator driver of the respective electronic processing element to cause an associated modulator of the photonic channel to modulate the optical signal in accordance with the packet, and wherein transforming the optical signal back into an electronic signal comprises measuring the optical signal by a photodetector of the photonic channel.

39. The method of claim 37, wherein each of the first, intermediate, and destination electronic processing elements comprises a router, and wherein the path through the electro-photonic network is determined collectively by the routers of the first, intermediate, and destination electronic processing elements.

40. The method of claim 39, wherein the routing information specifies the destination in terms of relative locations in first and second dimensions to the destination electronic processing element, the method further comprising, responsive to transmission of the packet from any of the first or intermediate

~~electronic processing elements to the next electronic processing element along the path, modifying the routing information in the packet.~~

~~41. The method of claim 39, wherein the routers of the first, intermediate, and destination electronic processing elements each comprise a local port and ports associated with multiple photonic channels connecting the respective electronic processing element to multiple other electronic processing elements within the electro-photonic network, wherein the routers of the first and the intermediate electronic processing elements each direct the packet to the port associated with the photonic channel connected to the electronic processing element that is next along the path, and wherein the router of the destination electronic processing element directs the packet to its local port.~~

~~42. A system comprising:~~

~~a first circuit package and a second circuit package each comprising~~

~~an electronic integrated circuit (EIC) comprising a plurality of processing elements and a plurality of message routers capable of transmitting and receiving a message, and~~

~~a plurality of intra-chip bidirectional photonic channels connecting the message routers into an intra-chip electro-photonic network that can operate on the message; and~~

~~a plurality of inter-chip bidirectional photonic channels connecting the message routers of the first and the second circuit packages into an inter-chip electro-photonic network that can transmit the message from an EIC in the first circuit package to an EIC in the second circuit package.~~

~~43. The system of claim 42, wherein each circuit package includes an electronic circuit layer in which the EIC is implemented and a photonic circuit layer in which the intra-chip bidirectional photonic channels are implemented.~~

~~44. The system of claim 43, wherein each circuit package includes a first semiconductor chip implementing the electronic circuit layer and a second semiconductor chip implementing the photonic circuit layer.~~

45. The system of claim 42, wherein the plurality of intra-chip bidirectional photonic channels of each of the circuit packages are implemented using optical waveguides in a photonic integrated circuit (PIC) of the circuit package.

46. The system of claim 42, wherein the intra-chip bidirectional photonic channels each comprise one or more photonic links in each direction, each photonic link comprising, in the PIC, an optical modulator at an input end of the photonic link, a photodetector at an output end of the photonic link, and an optical waveguide connecting the optical modulator to the photodetector.

47. The system of claim 46, wherein the message routers include photonic-circuit interfaces each for interfacing with one of the bidirectional photonic channels, each photonic-circuit interface comprising a modulator driver for each photonic link with which it interfaces at the input end of the photonic link and a transimpedance amplifier for each photonic link with which it interfaces at the output end of the photonic link.

48. The system of claim 46, wherein the plurality of inter-chip bidirectional photonic channels are implemented with optical fiber.

49. The system of claim 48, wherein the first and second circuit packages each include one or more optical coupling structures for coupling the electro-photonic network of the first circuit package via the optical fiber to the electro-photonic network of the second circuit package.

50. The system of claim 49, wherein the optical coupling structures include edge couplers in the PICs.

51. The system of claim 49, wherein the optical coupling structures include fiber attach units (FAUs) located over grating couplers in the PICs.

52. The system of claim 48, wherein the inter-chip bidirectional photonic channels are configured to transmit multiplexed optical signals.

~~53. The system of claim 52, wherein the inter-chip bidirectional photonic channels each comprise directional photonic channels in each direction, each directional photonic channel between a first PIC of a first circuit package and a second PIC of a second circuit package comprising:~~

~~in the first PIC, multiple optical modulators to create modulated optical signals at multiple respective wavelengths, a multiplexer to combine the modulated optical signals at the multiple wavelengths into a single multiplexed optical signal, and an optical coupling structure to couple the multiplexed optical signal into the optical fiber; and~~

~~in the second PIC, an optical coupling structure to couple the multiplexed optical signal from the optical fiber into the second PIC, a demultiplexer to demultiplex the multiplexed optical signal into modulated optical signals at the multiple wavelengths, and multiple respective photodetectors to measure the modulated optical signals at the multiple wavelengths.~~

~~54. The system of claim 42, further comprising at least one single-wavelength light source for supplying an optical carrier signal to modulators of the intra-chip bidirectional photonic channels, and at least one multiple-wavelength light source for supplying optical carrier signals at multiple wavelengths to groups of modulators of the inter-chip bidirectional photonic channels.~~

~~55. The system of claim 54, where the at least one single-wavelength light source and the at least one multiple-wavelength light sources comprise light sources integrated into the circuit packages.~~

~~56. The system of claim 54, where the at least one single-wavelength light source and the at least one multiple-wavelength light sources comprise light sources provided externally to the circuit packages and optically couple via one or more optical fibers to one or more PICs in the circuit packages.~~

~~57. The system of claim 42, further comprising a plurality of additional circuit packages having an associated EIC with a plurality of associated~~

~~processing elements, the first, second, and additional circuit packages arranged in a quadrilateral grid.~~

~~58. The system of claim 57, wherein each of the intra-chip and inter-chip bidirectional photonic channel connects a pair of immediately adjacent processing elements in the quadrilateral grid to result in a quadrilateral mesh topology of the inter-chip electro-photonic network.~~

~~59. The system of claim 58, wherein the plurality of inter-chip bidirectional photonic channels are further configured to directly connect pairs of processing elements on opposite edges of the quadrilateral grid to form an electro-photonic network having an extensible wrapped toroidal mesh topology.~~

~~60. The system of claim 42, wherein the message routers are configured to route the messages through the inter-chip and the intra-chip electro-photonic network, wherein when the message is sent from a first processing element to a second processing element that is not directly connected with the first processing element via a bidirectional photonic channel, the electronic is routed to the second processing element along a path through one or more third processing elements, wherein the message is at each of the third processing elements converted from an optical domain to an electronic domain and back into the optical domain at a message router associated with the respective third processing element.~~

~~61. The system of claim 60, wherein the message routers are configured to determine a path through the electro-photonic network for each message based in part on a portion of the message associated with routing information.~~

~~62. A processing device implementing an artificial neural network (ANN) comprising a plurality of neural nodes having associated sets of weights, the processing device comprising:~~

~~an electro-photonic network comprising a plurality of electronic processing elements connected by bidirectional photonic channels, each processing element comprising one or more processing engines, memory~~

communicatively coupled to the one or more processing engines, and a message router interfacing with two or more of the bidirectional photonic channels and communicatively coupled to the memory, wherein:

each neural node of the ANN is implemented by one or more of the processing elements;

the set of weights associated with each neural node is stored in the memory of the one or more processing elements implementing that neural node;

the message routers are configured, based on a predetermined flow of activations between the neural nodes, to stream a plurality of activations between the processing elements implementing the respective neural nodes during execution of the ANN; and

the one or more processing engines within each processing element are configured to perform, for each neural node implemented by the processing element, computations on the associated set of weights stored in the memory of the processing element and input activations to that node streamed to the processing element to generate an output activation for the node during the execution of the ANN.

63. The processing device of claim 62, wherein each processing element implements one or more of the neural nodes.

64. The processing device of claim 62, wherein at least one of the neural nodes is implemented by multiple of the processing elements jointly.

65. The processing device of claim 62, wherein activations between neural nodes implemented by the same processing element are exchanged via the memory of the processing element, and wherein activations between neural nodes implemented by different processing elements are exchanged via associated ones of the bidirectional photonic channels.

66. The processing device of claim 62, wherein the one or more processing engines comprise a dot product engine implementing a combinatorial tree of

multipliers and adders configured to perform multiply-accumulate (MAC) operations.

67. The processing device of claim 66, wherein the one or more processing engines further comprise a tensor engine configured to compute non-linear activations.

68. The processing device of claim 62, wherein the plurality of electronic processing elements is implemented on one or more electronic integrated circuits (EICs) each comprising multiple of the electronic processing elements, and wherein the bidirectional photonic channels connecting the electronic processing elements with each EIC are implemented as optical waveguides in an associated photonic integrated circuit (PIC) stacked with the EIC.

69. The processing device of claim 68, wherein each EIC and its associated PIC are packaged together as a system-in-package (SIP).

70. The processing device of claim 68, wherein the plurality of electronic processing elements are implemented on multiple EICs, and wherein the bidirectional photonic channels connecting electronic processing elements on different ones of the multiple EICs are implemented with optical fiber.

71. The processing device of claim 68, wherein the plurality of electronic processing elements are arranged in a quadrilateral grid, and wherein the bidirectional photonic channels are collectively configured to connect pairs of immediately adjacent processing elements in the grid to result in a quadrilateral mesh topology of the electro-photonic network.

72. A method of implementing an artificial neural network (ANN) comprising a plurality of neural nodes with associated predetermined weights, the method comprising:

connecting to an electro-photonic network comprising a plurality of processing elements connected by bidirectional photonic channels, each processing element comprising one or more processing engines, memory

~~communicatively coupled to the one or more processing engines, and a message router including two or more photonic-channel interfaces and a communicative coupling to the memory;~~

~~loading prior to runtime, based on an assignment between the neural nodes and the processing elements, the predetermined weights associated with each neural node into the memory of one or more processing elements assigned to implement the neural node; and~~

~~using the message routers at runtime, based on the assignments and on a predetermined flow of activations between the neural nodes within the ANN, to route the activations between the neural nodes implemented by the processing elements, wherein activations routed between nodes implemented by different source and destination elements among the processing elements are transformed, at the source element and at any intermediate processing element along a path from the source element to the destination element, from an electrical form to an optical form for transmission via the bidirectional photonic channels, and are transformed, at the destination element and any intermediate processing elements along the path, from an optical form to an electrical form.~~

~~73. The method of claim 72, wherein the weights are loaded from memory external to the electro-photonic network into the memory of the processing elements via a PCIE interface.~~

~~74. The method of claim 72, wherein activations between neural nodes implemented by a shared processing element are transferred electronically within the processing element.~~

~~75. The method of claim 72, wherein the assignment between the neural nodes and the processing elements is determined at compile time.~~

~~76. The method of claim 72, further comprising operating the electro-photonic network to:~~

~~stream activations between the processing elements in accordance with routing decisions made by the configured routers; and~~

for each node, perform computations on the associated weights and input activations streamed to the node using the one or more processing engines of the one or more processing elements assigned to implement the node.

77. The method of claim 72, further comprising selectively activating photonic links within the bidirectional optical channels based on the flow of activations for reduced power consumption.

78. The method of claim 77, wherein each bidirectional photonic channel comprises multiple photonic links, and wherein one of the links in each channel is kept active to serve as a master link.

79. The method of claim 72, wherein each bidirectional photonic channel comprises multiple photonic links in each direction, the method further comprising, during initialization of the electro-photonic network, establishing logical channels over at least some of the bidirectional photonic channels, wherein establishing a logical channel over a bidirectional photonic channel comprises bonding photonic links in each direction within that bidirectional photonic channel together to form a bonding group of links.

80. The method of claim 79, wherein photonic links that are nonfunctioning are omitted from the bonding groups.

81. The method of claim 79, wherein a number of photonic links in the bonding group is determined based on bandwidth requirements associated with implementing the ANN.

82. A hardware circuit comprising:

a combinatorial tree having a plurality of rows and a plurality of columns, the combinatorial tree using a plurality of hardware units to generate one or more dot product values based on input values received at a first column the combinatorial tree;

a first memory device for storing the input values;

a sequencer configured to obtain the input values from the first memory device and reorganize the input values in a switch fabric;

a clock configured to control a time for when a portion of the reorganized input values is provided to the first column of the combinatorial tree from the switch fabric; and

a plurality of hardware units where each hardware unit comprises an accumulator configured to accumulate the one or more dot product values, wherein during one or more subsequent time periods defined by the clock, additional portions of the reorganized input values are provided to accumulators of hardware units associated with the first column, and wherein during one or more additional time periods controlled by the clock, a value associated with each of the accumulators of the hardware units in the first column is written to the first memory device.

83. The hardware circuit of claim 82, wherein the hardware units comprise at least one fused multiple-accumulate (FMA) unit.

84. The hardware circuit of claim 82, wherein the combinatorial tree comprises an array of dot product units configured to receive the input values, and to generate the one or more dot product values based on the input values as received by the first column, a single dot product unit of the array comprising two or more of the hardware units.

85. The hardware circuit of claim 84, further comprising a control circuit, the array of dot product units comprising data paths, the control circuit being configured to use the data paths to cause at least two weight values to swap between two neighboring columns of the array or to propagate a weight value from a first row of the array to a second row of the array.

86. The hardware circuit of claim 82, wherein the sequencer includes the switch fabric that operatively couples the combinatorial tree to the first memory device.

87. The hardware circuit of claim 82, wherein the sequencer determines a sequence of input vectors provided to the first column based on a set of parameters, the set of parameters comprising at least one of a stride value, a dilation value, or a kernel size value.

88. The hardware circuit of claim 82, wherein the sequencer is configured to generate an individual input vector of the sequence of input vectors by reading a plurality of weight values and a plurality of operand values read from the first memory device during one or more clock cycles, the individual input vector comprising the plurality of the weight values and the plurality of the operand values.

89. The hardware circuit of claim 88, wherein the first memory device comprises memory banks, and wherein the plurality of weight values and the plurality of operand values read by the sequencer during the one or more clock cycles are selected for the reading such that:

the plurality of weight values and the plurality of operand values are permuted by the sequencer in the switch fabric after receipt from the memory bank, and each of the weight values and the operand valued are read by the sequencer in a single pass.

90. The hardware circuit of claim 88, wherein the first memory devices comprise memory banks, and wherein the plurality of weight values and the plurality of operand values read by the sequencer during one or more clock cycles are selected for the reading such that:

the plurality of weight values and the plurality of operand values are permuted by the sequencer in the switch fabric after receipt from the memory bank, and each of the weight values and the operand values are read by the sequencer in a single pass; and

data is read from each of the memory banks, wherein a number of rows of the memory banks is substantially equivalent to a number of rows in the first column of the combinatorial tree.

~~91. The hardware circuit of claim 88, wherein each successive read of the first memory device, by the sequencer, results in reading of new weight values and new operand values from the first memory device not read by the sequencer during a previous clock cycle.~~

~~92. The hardware circuit of claim 82, wherein a single hardware unit is operatively coupled to at least two adjacent hardware units such that an output value generated by the single hardware unit is shared as an input value to each of the at least two adjacent hardware units.~~

~~93. The hardware circuit of claim 82, wherein the accumulator comprises a plurality of accumulators configured to accumulate partial dot product values generated by a single hardware unit as values flow through the single hardware unit.~~

~~94. The hardware circuit of claim 82, wherein the combinatorial tree comprises registers associated with the hardware units configured to maintain clock alignment of values flowing through the hardware units.~~

~~95. The hardware circuit of claim 82, comprising logic that is configured to generate a set of final dot product values for the input values after all of a sequence of input vectors have been inputted to the combinatorial tree, the set of final dot product values being constructed from values stored in accumulators of the hardware units of the combinatorial tree.~~

~~96. The hardware circuit of claim 95, wherein the logic is configured to store the set of final dot product values to the first memory device.~~

~~97. The hardware circuit of claim 82, wherein the input values comprise at least one weight value and at least one operand value.~~

~~98. The hardware circuit of claim 82, wherein the hardware circuit is part of a photonic integrated circuit (PIC).~~

99. A method comprising:

reading, by a sequencer, a first plurality of weight values and a first plurality of operand values from a set of memory devices operatively coupled to the sequencer;

receiving, at a first column of a combinatorial tree, a plurality of first input vectors from the sequencer, the first plurality of input vectors comprising the first plurality of weight values and the first plurality of operand values;

processing the first plurality of input vectors by math units at the first column of the combinatorial tree, the math units being associated with each of the input vectors, each of the math units having at least one accumulator, the combinatorial tree being configured to generate a dot product value in an accumulator of each of the math unit based on values received by the math units at the first column of the combinatorial tree;

reading, by the sequencer, a second plurality of weight values and a second plurality of operand values from the set of memory devices;

receiving, at the first column of the combinatorial tree, a second plurality of input vectors from the sequencer, the second plurality of input vectors comprising the second plurality of weight values and the second plurality of operand values;

processing the second plurality of input vectors by the math units at the first column of the combinatorial tree, the first plurality of input vectors and the second plurality of inputs vector being part of a sequence of input vectors to be received by the math units in the first column of the combinatorial tree; and

after all of the sequence of input vectors has been received by the first column of the combinatorial tree and processed by associated math units, providing a set of final dot product values by retrieving a value from each accumulator in each of the math units residing in every row of the first column of the combinatorial tree.

100. The method of claim 99, wherein the at least one accumulator comprises a plurality of accumulators in each of the math units, the plurality of accumulators being configured to accumulate partial dot product values generated by individual math units as values flow through the individual math units.

~~101. A hardware circuit comprising:~~

~~an array of dot product units organized as a combinatorial tree that generates dot product values based on weight values and activation values received as input by the array of dot product units, the array of dot product units comprises 64 rows by 32 columns of dot product units, each dot product unit being configured to receive as input two 8-bit values and having an accumulator; and~~

~~a switch fabric operatively coupling the array to a set of memory devices, the set of memory devices storing a plurality of weight values and a plurality of activation values, the switch fabric being configured to provide 64 input vectors as input to a first column of the array, during a first clock sequence comprising one or more clock cycles,~~

~~wherein one or more additional clock sequences cause the switch fabric to provide a plurality of additional sets of 64 input vectors to the first column of the array, and wherein when each of the accumulators in the first column of the array has 32 bits, writing each value from each accumulator back into the set of memory devices.~~

~~102. The hardware circuit of claim 101, wherein the dot product units comprise a plurality of FMA units.~~

~~103. The hardware circuit of claim 101, wherein the dot product units are configured to receive a 32-byte input.~~

~~104. The hardware circuit of claim 101, wherein the set of memory devices comprises 64 banks of 32-byte wide memory devices.~~

~~105. A circuit package comprising:~~

~~an application-specific integrated circuit (ASIC) comprising a plurality of processing elements that include photonic-channel interfaces; and~~

~~a plurality of photonic channels connecting the plurality of processing elements via the photonic-channel interfaces to form at least part of an electro-photonic network, a sub-plurality of the plurality of photonic channels being~~

connected to an individual processing element of the plurality of processing elements, the individual processing element being configured to:

select, for the individual processing element, a master photonic channel from the sub-plurality of photonic channels;

select, for the individual processing element, a set of slave photonic channels from the sub-plurality of photonic channels;

extract a received clock signal from the master photonic channel;

generate, based on the received clock signal, a local clock signal used by the individual processing element to perform one or more local operations on the individual processing element; and

transmit, over the set of slave photonic channels, a distributed clock signal to a set of the plurality of processing elements connected to the individual processing element, the transmitting the distributed clock signal comprising transforming the distributed clock signal from an electrical form to an optical form using the photonic-channel interface of the individual processing element, the transmitting the distributed clock signal further comprising transforming the distributed clock signal from the optical form to the electrical form at the set of the plurality of processing elements, the distributed clock signal being suitable for transmission across the set of slave photonic channels and for use as associated local clock signals by the set of the plurality of processing elements, the distributed clock signal being generated based on the received clock signal.

106. The circuit package of claim 105, wherein the individual processing element comprises a jitter-attenuating phase-lock loop (PLL), wherein the individual processing element uses the jitter-attenuating PLL to generate a low jitter clock signal based on the received clock signal, and wherein the generating of the local clock signal based on the received clock signal comprises generating the local clock signal based on the low jitter clock signal.

107. The circuit package of claim 105, wherein the individual processing element selects the master photonic channel during boot time of the individual processing element.

~~108. The circuit package of claim 105, wherein the individual processing element selects the set of slave photonic channels during boot time of the individual processing element.~~

~~109. The circuit package of claim 105, wherein the individual processing element is configured to:~~

~~perform a channel alignment operation on the master photonic channel, the channel alignment operation being configured to adjust one or more settings of the individual processing element to compensate for clock skew.~~

~~110. The circuit package of claim 105, wherein the individual processing element extracts the received clock signal from the master photonic channel by performing clock data recovery on an incoming bit stream received over the master photonic channel.~~

~~111. The circuit package of claim 105, wherein the individual processing element transmits the distributed clock signal to the set of processing elements by transmitting one or more outgoing bit streams to the set of processing elements, the one or more outgoing bit streams being generated based on the distributed clock signal.~~

~~112. The circuit package of claim 105, wherein the individual processing element comprises a tensor processor and a DNN, wherein each of the tensor processor and the DNN is configured to operate based on the local clock signal, and wherein a packet is capable of being transferred between the DNN and the tensor processor using the local clock signal.~~

~~113. The circuit package of claim 105, wherein the individual processing element comprises a message router that includes the photonic channel interface, the message router being configured to operate based on the local clock signal.~~

~~114. The circuit package of claim 105, wherein the individual processing element comprises a hardware circuit for computing one or more dot products~~

between at least two vectors, the hardware circuit being configured to operate based on the local clock signal.

115. The circuit package of claim 105,

wherein the individual processing element is a first processing element, the sub-plurality of photonic channels is a first sub-plurality of photonic channels, the master photonic channel is a first master photonic channel, the set of slave photonic channels is a first set of slave photonic channels, the received clock signal is a first received clock signal, the local clock signal is a first local clock signal, and the distributed clock signal is a first distributed clock signal; and

wherein a second sub-plurality of the plurality of photonic channels being connected to a second processing element, the second processing element being included in the set of processing elements connected to the first processing element, the second sub-plurality of the plurality of photonic channels including an individual photonic channel of the set of slave photonic channels that connects the first processing element to the second processing element, the second processing element being configured to:

select, for the second processing element, a second master photonic channel from the individual photonic channel;

select, for the second processing element, a second set of slave photonic channels from the second sub-plurality of photonic channels;

extract a second received clock signal from the second master photonic channel;

generate, based on the second received clock signal, a second local clock signal used by the second processing element to perform one or more local operations on the second processing element; and

transmit, over the second set of slave photonic channels, a second distributed clock signal to a second set of the plurality of processing elements connected to the second processing element, the transmitting the second distributed clock signal comprising transforming the second distributed clock signal from the electrical form to the optical form using the photonic-channel interface of the individual processing element, the transmitting the second distributed clock signal further comprising

transforming the second distributed clock signal from the optical form to the electrical form at the second set of the plurality of processing elements, the second distributed clock signal being suitable for transmission across the second set of slave photonic channels and for use as associated local clock signals by the second set of the plurality of processing elements, the second distributed clock signal being generated based on the second received clock signal.

116. The circuit package of claim 115, wherein the first processing element comprises a first set of components, the second processing element comprises a second set of components, the first set of components comprising at least one of a first tensor processor, a first message router that includes a photonic-channel interface, or a first hardware circuit for computing one or more first dot products between at least two vectors, the second set of components comprising at least one of a second tensor processor, a second message router that includes a photonic-channel interface, or a second hardware circuit for computing one or more second dot products between at least two vectors, the first set of components being configured to operate based on the first local clock signal, and the second set of components being configured to operate based on the second local clock signal.

117. A method comprising:

selecting, by an individual processing element of a plurality of processing elements, a master photonic channel from a plurality of photonic channels, the master photonic channel being selected for the individual processing element, the plurality of processing elements being part of an application-specific integrated circuit (ASIC) of a circuit package, the plurality of processing elements being connected together by a plurality of photonic channels to form at least part of an electro-photonic network within the circuit package;

selecting, by the individual processing element, a set of slave photonic channels from the plurality of photonic channels, the set of slave photonic channels being selected for the individual processing element;

~~extracting, by the individual processing element, a received clock signal from the master photonic channel in a digital format;~~

~~based on the received clock signal in the digital format, generating, by the individual processing element, a local clock signal used by the individual processing element to perform one or more local operations on the individual processing element using a digital portion of the ASIC; and~~

~~transmitting, by the individual processing element and over the set of slave photonic channels, a distributed clock signal to a set of the plurality of processing elements connected to the individual processing element, the distributed clock signal being generated based on the received clock signal in the digital format, the transmitting comprising:~~

~~transforming the distributed clock signal from a digital format to an optical format;~~

~~routing the distributed clock signal in the optical format across the set of slave photonic channels;~~

~~receiving the distributed clock signal in the optical format at photonic interfaces of the set of the plurality of processing elements; and~~

~~transforming the distributed clock signal to the digital format in the set of the plurality of processing elements using associated photonic channel interfaces.~~

~~118. The method of claim 117, wherein the individual processing element comprises a jitter-attenuating phase-lock loop (PLL), wherein the individual processing element uses the jitter-attenuating PLL to generate a low jitter clock signal based on the received clock signal, and wherein the generating of the local clock signal based on the received clock signal comprises generating the local clock signal based on the low jitter clock signal.~~

~~119. The method of claim 117, wherein the selecting of the master photonic channel is performed during boot time of the individual processing element.~~

~~120. The method of claim 117, wherein the selecting of the set of slave photonic channels during boot time of the individual processing element.~~

~~121. The method of claim 117, comprising:~~

~~performing, by the individual processing element, a channel alignment operation on the master photonic channel, the channel alignment operation being configured to adjust one or more settings of the individual processing element to compensate for clock skew.~~

~~122. The method of claim 117, wherein the extracting of the received clock signal from the master photonic channel comprises performing clock data recovery on an incoming bit stream received over the master photonic channel.~~

~~123. The method of claim 117, wherein the transmitting of the distributed clock signal to the set of processing elements comprises transmitting one or more outgoing bit streams to the set of processing elements, the one or more outgoing bit streams being generated based on the distributed clock signal.~~

~~124. The method of claim 117, wherein the individual processing element comprises a set of components, the set of components comprising at least one of a tensor processor, a message router that includes photonic-channel interfaces, or a hardware circuit for computing a dot product between at least two vectors, the set of components being configured to operate based on the local clock signal.~~