PROCESS FOR MANUFACTURE OF MOS GATED DEVICE WITH REDUCED MASK COUNT

ABSTRACT OF THE DISCLOSURE

A reduced mask process for forming a MOS gated device such as a power MOSFET uses a first mask to sequentially form a cell body and a source region within the cell body, and a second mask step to form, by a silicon etch, a central opening in the silicon surface at each cell and to subsequently undercut the oxide surrounding the central opening. A contact layer then fills the openings of each cell to connect together the body and source regions. Only one critical mask alignment step is used in the process.

This Sheet Has Been Replaced

