

DESCRIPTION

TITLE OF THE INVENTION: SEMICONDUCTOR STRUCTURE BASED ON SILICON CARBIDE FOR POWER APPLICATIONS AND ASSOCIATED MANUFACTURING METHOD

FIELD OF THE INVENTION

[0001] The present invention is aimed at the field of microelectronics and more particularly power electronics. It relates in particular to a structure comprising a semiconductor layer made of high-quality monocrystalline silicon carbide and a carrier substrate made of polycrystalline silicon carbide, assembled at an electrically conductive interface zone. The invention also relates to a method for manufacturing such a structure.

[0002] TECHNOLOGICAL BACKGROUND OF THE INVENTION

[0003] It is usual to form a semiconductor structure by transferring a working semiconductor layer, of low thickness and of high crystalline quality, onto a semiconductor carrier substrate of a lower crystalline quality. A well-known thin-film transfer solution is the Smart Cut™ process, based on an implantation of light ions into a donor substrate and on a direct bonding assembly at a bonding interface between said donor substrate and a carrier substrate; a separation takes place along a buried fragile plane defined by the implantation, leading to the transfer of a working layer from the donor substrate, onto the carrier substrate. In addition to economic advantages related to the streamlining of the high-quality material of the working layer, the semiconductor structure can also provide advantageous properties, for example related to the thermal or electrical conductivity or mechanical compatibility of the carrier substrate.

- [0004] In the field of power electronics for example, it is advantageous to establish electrical conduction between the working layer and the carrier substrate, so as to form vertical components. For example, in the case of a structure comprising a working layer made of monocrystalline silicon carbide (SiC) and a carrier substrate made of lower quality silicon carbide (SiC) (monocrystalline or polycrystalline), the bonding interface must have a resistivity that is as low as possible, less than 0.1 mohm.cm^2 , or even preferentially less than 0.01 mohm.cm^2 .
- [0005] Certain solutions of the state of the art propose achieving direct semiconductor-on-semiconductor bonding between the working layer and the carrier substrate to establish vertical electrical conduction. However, it is difficult to achieve a good interface quality with this type of bonding.
- [0006] F. Mu et al. (ECS Transactions, 86 (5) 3-21, 2018) implement direct bonding, after activation of the surfaces to be assembled by argon bombardment (SAB for "surface activation bonding"): such treatment prior to bonding generates a very high density of dangling bonds, which promote the formation of covalent bonds at the assembly interface, and therefore a high bonding energy. This method nevertheless has the shortcoming of generating an amorphous layer, at the assembled surfaces, which adversely affects the vertical electrical conduction between the thin layer and the carrier substrate. To overcome this problem, heavy doping of said surfaces is proposed in particular in document EP3168862, by shallow implantation. In addition to the fact that shallow implantation doses cannot be increased indefinitely, high introductions of dopant atoms tend to damage the crystalline quality of the working layer and/or reduce the bonding energy of the structure.
- [0007] Other solutions of the state of the art propose conductive bonding using different types of layers deposited on the surfaces to be assembled, in order to avoid massive implantation of dopants prior to assembly.

[0008] Document WO2022/008809 proposes to form an interface zone from a very thin layer of a metal material, such as tungsten, in a SiC/SiC semiconductor structure. Considering a working layer and a carrier substrate made of monocrystalline SiC with a resistivity of 20 mohm.cm, and a tungsten layer of 1 nm to 3 nm (W) sandwiched between the working layer and the carrier substrate, it is possible to achieve an resistivity of the interface zone of less than or equal to 0.1 mohm.cm², after applying an appropriate heat treatment and formation of very fine nodules largely consisting of metal (W), responsible for good vertical conduction of the interface zone.

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[0009] Document WO2022/129726 proposes to form an interface zone, in a SiC/SiC semiconductor structure, comprising regions of direct contact between the working layer and the carrier substrate, and agglomerates comprising a semiconductor material different from that or those of the working layer and the carrier substrate, and having a thickness less than or equal to 250 nm. The semiconductor material is chosen for its particular affinity with oxygen. Thus, the agglomerates are able to effectively trap the oxygen that may be present in the bonding interface; the regions of direct contact between the working layer and the carrier substrate, devoid of native oxide residues in particular, allow electrical conduction and/or a vertical semi-conductor/semi-conductor contact that is effective and of good quality. Considering a working layer with a resistivity of 20 mohm.cm, a carrier substrate with a resistivity of 20 mohm.cm and a silicon semiconductor material, it is possible to obtain a resistivity of the interface zone of less than or equal to 0.1 mohm.cm², for example 0.032 mohm.cm² (after annealing the structure at 1370°C) or 0.0076 mohm.cm² (after annealing at very high temperature, namely 1900°C).

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[0010] **OBJECT OF THE INVENTION**

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[0011] The present invention offers a solution that meets the need for very low resistivity (less than or equal to 0.01 mohm.cm²) in the interface zone of a semiconductor structure based on silicon carbide, and simplifies the fabrication

of the structure. It relates to a semiconductor structure and a method of manufacturing such a structure.

[0012] **BRIEF DESCRIPTION OF THE INVENTION**

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[0013] The present invention relates to a semiconductor structure based on silicon carbide comprising:

[0014] - a working layer made of monocrystalline silicon carbide having a first dopant concentration that is uniform over its thickness,

10 [0015] - a carrier substrate made of polycrystalline silicon carbide having a second dopant concentration that is uniform over its thickness, the second concentration being related to the first concentration by the following relationship:

[0016] $C_2 > N_2 \times \exp(-C_1/N_1)$ with

15 [0017] C_1 is the first concentration, C_2 the second concentration, $N_1 = 2.85 \cdot 10^{18} \text{ cm}^{-3}$ and $N_2 = 5.40 \cdot 10^{20} \text{ cm}^{-3}$,

[0018] - an interface zone, between the carrier substrate and the working layer, comprising nodules and regions of direct contact between the working layer and the carrier substrate, the nodules comprising a metal or semiconductor
20 material other than silicon carbide, the interface zone having an average resistivity of less than or equal to 0.01 mohm.cm^2 .

[0019] The dopant concentration profile along a thickness of the semiconductor structure:

[0020] - is in the form of a step, and

25 [0021] - is devoid of a doping peak in the interface zone, or

[0022] - exhibits a doping peak in the interface zone, the extremum of which corresponds to a third dopant concentration equal to the second dopant concentration to within plus or minus 10%.

30 [0023] According to advantageous features of the invention, taken alone or in any feasible combination:

- the resistivity of the carrier substrate is less than or equal to 10 mohm.cm, 5 mohm.cm, even 3 mohm.cm or even 2 mohm.cm;
 - the interface zone has a thickness of less than or equal to 200 nm;
 - the metal material of the nodules is selected from tungsten, titanium, nickel,
- 5 aluminum, molybdenum, niobium, tantalum, cobalt and copper, or the semiconductor material of the nodules is selected from silicon, germanium, carbon, III-V compounds such as gallium nitride or other compounds formed from these materials.
- 10 [0024] The invention also relates to a method for manufacturing a semiconductor structure based on silicon carbide comprising the following steps:
- [0025] a) providing a working layer made of monocrystalline silicon carbide having a free face to be assembled and a first dopant concentration that is uniform over its thickness,
- 15 [0026] b) providing a carrier substrate made of polycrystalline silicon carbide having a free face to be assembled, a second dopant concentration that is uniform over its thickness, the second concentration being related to the first concentration by the following relationship:
- [0027] $C_2 > N_2 \times \exp(-C_1/N_1)$ with
- 20 [0028] C_1 is the first concentration, C_2 the second concentration, $N_1 = 2.85 \cdot 10^{18} \text{ cm}^{-3}$ and $N_2 = 5.40 \cdot 10^{20} \text{ cm}^{-3}$,
- [0029] c) depositing a film of a metal or semiconductor material other than silicon carbide having a thickness of less than or equal to 20 nm, on the free face of the working layer to be assembled and/or on the free face of the carrier
- 25 substrate to be assembled,
- [0030] d) forming an intermediate structure, comprising direct assembly of the free faces to be assembled of the working layer and of the carrier substrate, respectively, the intermediate structure including an encapsulated film originating from the one or more film(s) deposited during step c),
- 30 [0031] e) annealing the intermediate structure at a temperature of between 1200°C and 2000°C, to form the semiconductor structure comprising an interface zone which includes nodules resulting from the segmentation of the

encapsulated film and regions of direct contact between the thin layer and the carrier substrate.

5 [0032] The interface zone has an average resistivity of less than or equal to 0.01 mohm.cm²; the dopant concentration profile along one thickness of the semiconductor structure is in the form of a step, and is devoid of a doping peak in the interface zone or exhibits a doping peak in the interface zone, the extremum of which corresponds to a third dopant concentration equal to the second dopant concentration to within plus or minus 10%.

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[0033] According to advantageous features of the invention, taken alone or in any feasible combination:

- 15 • step a) comprises an implantation of light species in a donor substrate of monocrystalline silicon carbide, to form a buried fragile plane which delimits, with a front face of the donor substrate, the working layer;
- 20 • step d) comprises, after the direct assembly giving rise to a bonded assembly comprising the donor substrate and the carrier substrate, a separation at the buried fragile plane, in order to form, on the one hand, the intermediate structure comprising the working layer, the encapsulated film and the carrier substrate, and on the other hand, the remainder of the donor substrate;
- 25 • prior to step c), the free face of the thin film to be assembled has a monocrystalline surface, devoid of zones amorphized or damaged by doping or bombardment activation, and the free face of the carrier substrate to be assembled has a polycrystalline surface, devoid of zones amorphized or modified by doping or bombardment activation;
- the method comprises a step of epitaxial growth of an additional layer of monocrystalline silicon carbide on the working layer of the semiconductor structure.

30 **BRIEF DESCRIPTION OF THE DRAWINGS**

[0034] Other features and advantages of the invention will emerge from the following detailed description of the invention with reference to the appended figures, in which:

5 [0035] [Fig. 1] [Fig. 1] shows a semiconductor structure in accordance with the present invention;

[0036] [Fig. 2a]

[0037] [Fig. 2b]

[0038] [Fig. 2c]

[0039] [Fig. 2d]

10 [0040] [Fig. 2e] Figures 2a to 2e show steps of a manufacturing method in accordance with the present invention;

[0041] [Fig. 3a]

[0042] [Fig. 3b]

[0043] [Fig. 3c]

15 [0044] [Fig. 3d] Figures 3a to 3d show steps of a manufacturing method in accordance with the present invention;

[0045] [Fig. 4] [Fig. 4] shows a dopant concentration profile (A) along the thickness of a semiconductor structure in accordance with the present invention, from other dopant concentration profiles (B, C, D) of structures of
20 the state of the art

[0046] [Fig. 5] [Fig. 5] shows a curve expressing the relationship between the second concentration C_2 and the first concentration C_1 , so as to obtain an average resistivity of the interface zone (denoted ρ_{int} in the figure), less than or equal to 0.01 mohm.cm^2 ; the first concentration C_1 and the second concentration C_2 being
25 respectively the dopant concentration of the working layer made of monocrystalline silicon carbide and the dopant concentration of the carrier substrate in a semiconductor structure in accordance with the invention.

[0047] Some figures are schematic depictions which, for the sake of readability,
30 are not to scale. In particular, the thicknesses of the layers along the z-axis are not to scale with respect to the lateral dimensions along the x- and y-axes. The same references in the figures may be used for elements of the same type.

DETAILED DESCRIPTION OF THE INVENTION

[0048] The invention relates to a semiconductor structure 100 comprising a
5 working layer 10 made of monocrystalline silicon carbide, typically of polytype
4H, a carrier substrate 30 made of polycrystalline silicon carbide, typically of
polytype 3C, and an interface zone 20 between the working layer 10 and the
carrier substrate 30 ([Fig.1]). Like the working layer 10, the interface zone 20
extends in parallel to the main plane (x,y).

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[0049] Advantageously, and as is usually the case in the field of
microelectronics, the semiconductor structure 100 is in the form of a circular
wafer with a diameter of between 100 mm and 450 mm. It is understood that,
in this case, the carrier substrate 30 and the working layer 10 also have such
15 a circular shape. The front 100a and rear 100b (circular) faces of the wafer
extend in parallel to the main plane (x,y).

[0050] The semiconductor structure 100 has a total thickness typically
comprised between 300 microns and 1000 microns. The thickness of the
20 carrier substrate 30 forms the major part of this total thickness, with the
working layer 10 typically having a thickness of less than a few microns, or
even less than 1 μm .

[0051] According to the invention, the carrier substrate 30 has a dopant
25 concentration (hereinafter referred to as the second concentration C_2) that is
uniform over its thickness. By uniform, we mean a dopant concentration that
is constant over the thickness to within +/- 10%. For N-type doping, nitrogen,
phosphorus or arsenic atoms will be present in the polycrystalline matrix of
the carrier substrate 30, whereas boron or aluminum atoms will be present
30 for P-type doping.

[0052] Advantageously, the resistivity of the carrier substrate 30 is less than or equal to 10 mohm.cm (i.e. a dopant concentration typically greater than or equal to $1 \cdot 10^{20} \text{ cm}^{-3}$), 5 mohm.cm (i.e. a dopant concentration typically greater than or equal to $2 \cdot 10^{20} \text{ cm}^{-3}$), or even 3 mohm.cm, or even 2 mohm.cm (i.e. a
5 dopant concentration greater than or equal to $4 \cdot 10^{20} \text{ cm}^{-3}$).

[0053] The working layer 10 also has a dopant concentration (known as the first concentration C_1) that is uniform over its thickness (to within +/- 10%). The doping type of the working layer 10 is usually the same as that of the carrier substrate 30.
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[0054] In addition, the second concentration C_2 is related to the first concentration C_1 by the following relationship: $C_2 > N_2 \times \exp(-C_1/N_1)$ with $N_1 = 2.85 \cdot 10^{18} \text{ cm}^{-3}$ and $N_2 = 5.40 \cdot 10^{20} \text{ cm}^{-3}$, as shown in [Fig.5]. Note that this curve is defined for an N-type doped, monocrystalline 4H-SiC working layer 10 and
15 an N-type doped, polycrystalline 3C-SiC carrier substrate 30.

[0055] The range of first C_1 and second C_2 concentrations according to the invention is therefore located above the curve of [Fig.5], said curve reflecting an average resistivity ρ_{int} of the interface zone 20 equal to 0.01 mohm.cm²,
20 and less than this value when moving above the curve.

[0056] A wide range of resistivities can thus be used for the working layer 10, in the semiconductor structure 100 in accordance with the invention: a resistivity of between a few ohms and 10 mohm.cm for example (i.e. typically
25 a first concentration C_1 of dopants of between a few $1 \cdot 10^{17} \text{ cm}^{-3}$ and $1 \cdot 10^{19} \text{ cm}^{-3}$) can be used. By selecting the second concentration C_2 of the carrier substrate 30 within the defined range (above the ρ_{int} curve), excellent electrical conduction between the working layer 10 and the carrier substrate 30 will be achieved via the interface zone 20.

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[0057] The interface zone 20 comprises nodules 21 and regions of direct contact 22 between the working layer 10 and the carrier substrate 30. The

nodules 21 are composed of a metal or semiconductor material other than silicon carbide. Without limitation, the metal material of the nodules 21 can be selected from tungsten, titanium, nickel, aluminum, molybdenum, niobium, tantalum, cobalt and copper; the semiconductor material of the nodules 21 can
5 be selected from silicon, germanium, carbon, III-V compounds such as gallium nitride, or other compounds formed from these materials (SiGe, SiGeC, etc.).

[0058] The interface zone 20 has a thickness, along a z axis normal to the main plane (x,y), typically less than or equal to 200 nm, or even less than or equal to
10 100 nm. In particular, its maximum thickness is defined by the maximum thickness of the nodules 21. The nodules 21, distributed over the interface zone 20, are either disjoint or adjacent to one another; the disjoint nodules are mostly separated from one another by the regions of direct contact 22 wherein the working layer 10 is in direct contact with the carrier substrate 30, in other words,
15 wherein there is a direct bond between the monocrystalline silicon carbide of the working layer 10 and the polycrystalline silicon carbide of the carrier substrate 30.

[0059] On a median plane P of the interface zone 20, the degree of coverage of the regions of direct contact 22 is typically between 30% and 80%.

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[0060] In some cases of semiconductor structures 100, nanometer-thick cavities may optionally exist in these regions of direct contact 22, but said cavities typically occupy less than 10% or even less than 5% of the surface area along the main (x,y) plane occupied by the regions of direct contact 22.
25 Their thickness is also less than that of the nodules 21.

[0061] According to the present invention, the interface zone 20 has a resistivity of less than or equal to 0.01 mohm.cm². We are talking herein about a "surface" resistivity in ohm.cm² for the interface zone 20 due to its very low
30 thickness. By average resistivity, we mean the resistivity of the interface zone 20 as a whole, i.e. including its various regions, namely the regions of direct contact 22, the nodules 21 and the cavities (if present). Indeed, the

resistivity of the interface zone 20 is obtained from a measurement of I(V) (current as a function of voltage) taken at two electrodes formed on the structure 100, between which the current path passes through the interface zone 20, due to the presence of trenches 40 crossing said zone 20, between
5 said electrodes. Naturally, the resistive contributions of other layers and interfaces involved in the current path are taken into account.

[0062] As shown in [Fig.4], a dopant concentration profile A, along a thickness of the semiconductor structure 100, is in the form of a step, between the working
10 layer 10 and the carrier substrate 30. In other words, starting from the free face of the working layer 10, crossing the interface zone 20 and penetrating the carrier substrate 30 to a depth of more than 1 μm (parallel to the z axis), the dopant concentration profile defines a clear step between the thin layer 10, which is less doped than the carrier substrate 30, and the latter, whose doping
15 level is higher (in particular, of the order of $5.10^{18} \text{ cm}^{-3}$ for the first concentration C_1 and of the order of $5.10^{20} \text{ cm}^{-3}$ for the second concentration C_2 , in the example of [Fig.4]). There is no dopant diffusion profile to increase or modify the uniform doping level of the thin film 10 in the vicinity of the interface zone 20.

20 [0063] Furthermore, the interface zone 20 has an average doping level identical to or very close to that of the carrier substrate 30. The interface zone 20 is devoid of any doping peaks associated with extrinsic introduction of dopants on the side of the working layer 10 or the carrier substrate 30 (for example by implantation); said interface zone 20 has a dopant concentration
25 identical to within plus or minus 10% of the second concentration.

[0064] Optionally, the interface zone 20 may exhibit a doping peak, but whose extremum corresponds to a dopant concentration (so-called third concentration) slightly greater or less than the second concentration: the third
30 dopant concentration is equal to the second dopant concentration C_2 to within plus or minus 10%. This doping peak is therefore also much lower than a peak

associated with extrinsic introduction of dopants, as can be seen in profiles B, C and D in [Fig.4], taken from structures of the state of the art.

[0065] The semiconductor structure 100 thus guarantees good electrical conductivity between the working layer 10 and the carrier substrate 30, via its interface zone 20. In particular, the regions of direct contact 22 benefit from a high concentration of dopants, similar to that of the carrier substrate 30, due to the diffusion and trapping of dopants from the carrier substrate 30 at the interface between the working layer 10 and carrier substrate 30. The nodules 21 can also participate in vertical electrical conduction; the presence of a large quantity of dopants at the interface between the nodules 21 and the highly-doped carrier substrate 30 is conducive to this electrical conduction.

[0066] The interface zone 20, with a resistivity of less than or equal to 0.01 mohm.cm², can be considered "transparent" in the semiconductor structure 100, providing no parasitic increase in resistance in vertical electrical conduction.

[0067] In addition to its excellent electrical conduction, the interface zone 20 ensures physical continuity between the working layer 10 and the carrier substrate 30, and provides excellent mechanical strength for the semiconductor structure 100. The quality of the working layer 10 is therefore not affected by any holes or interface defects; it should be noted that the above-mentioned cavities, when they are present, have dimensions and a density which do not negatively impact the quality and the mechanical resistance of the working layer 10.

[0068] Power components can be produced on and/or in the working layer 10 of a semiconductor structure 100 according to the invention. There is no need to thin the carrier substrate 30 to thicknesses of less than 200 µm, or even less than 150 µm, as the high doping of the carrier substrate 30 ensures excellent vertical electrical conductivity. It is usually necessary to thicken the working

layer 10, for example by forming an additional layer by epitaxy, to produce the power components.

5 [0069] These components can notably comprise at least one electrical contact on and/or in the carrier substrate 30, in the region of a rear face 100b of the semiconductor structure 100. By way of non-limiting examples, these power components may include transistors, diodes, thyristors or passive components (capacitors, inductors, etc.) etc.

10 [0070] The invention also relates to a method for manufacturing a semiconductor structure 100 as previously described.

[0071] The production method firstly comprises a step a) of providing the working layer 10 made of monocrystalline silicon carbide ([Fig. 2a]). In this step a), the
15 working layer 10 has a free face 10a intended to be assembled, during a subsequent step of the method, also called front face 10a; it also has a rear face 10b opposite its front face 10a. The thin film 10 has a dopant concentration (first concentration C_1) that is uniform over its thickness. As previously mentioned, a resistivity for example of between a few ohms and 10 mohm.cm (i.e. a first
20 dopant concentration C_1 of between a few $1.10^{17} \text{ cm}^{-3}$ and $1.10^{19} \text{ cm}^{-3}$) can be used.

[0072] According to an advantageous embodiment, the working layer 10 is derived from the transfer of a surface layer of a donor substrate 1, in particular
25 a layer transfer based on the Smart Cut™ method.

[0073] Step a) can thus comprise an implantation of light species, for example hydrogen, helium or a combination of these two species, into a donor substrate 1 (typically 4H-SiC), to form a buried fragile plane 11 which delimits,
30 with a front face 10a of the donor substrate 1, the working layer 10 ([Fig. 3a]).

[0074] According to a variant of this embodiment, step a) comprises the formation of the donor substrate 1 by epitaxy of a donor layer 1' on an initial substrate, prior to the implantation of the light species ([Fig. 3b]). This variant makes it possible to form a donor layer 1' having the structural and electrical characteristics required for the intended application. In particular, an excellent crystal quality can be obtained by epitaxy, and in situ doping of the donor layer 1' can be precisely controlled. The implantation of light species, to form the buried fragile plane 11, is then carried out in the donor layer 1'.

10 [0075] Alternatively, the working layer 10, provided in step a) may of course be formed from other known thin-film transfer techniques.

[0076] The manufacturing method according to the invention then comprises a step b) of providing a carrier substrate 30 made of polycrystalline silicon carbide ([Fig. 2b]). The carrier substrate 30 has a free face 30a intended to be assembled during a subsequent step of the method, also called front face 30a; it also has a rear face 30b.

[0077] According to the invention, the dopant concentration (second concentration C_2) of the carrier substrate 30 is uniform over its thickness and is related to the first concentration C_1 by the following relationship:

[0078] $C_2 > N_2 \times \exp(-C_1/N_1)$ with $N_1 = 2.85.10^{18} \text{ cm}^{-3}$ and $N_2 = 5.40.10^{20} \text{ cm}^{-3}$, particularly in the case of N-type doping for the working layer 10 and for the carrier substrate 30.

[0079] Advantageously, the resistivity of the carrier substrate 30 is less than or equal to 10 mohm.cm, or even 5 mohm.cm, 3 mohm.cm or else 2 mohm.cm.

30 [0080] The manufacturing method then comprises a step c) of depositing a film 2 made of a metal or semiconductor material other than silicon carbide, on the free face to be assembled 10a of the working layer 10 or on the free face

to be assembled 30a of the carrier substrate 30 or else, as shown in [Fig. 2c], on the two free faces to be assembled 10a, 30a.

5 [0081] Note that the free face 10a of the working layer 10 has a perfectly monocrystalline surface; neither implantation doping nor bombardment activation has damaged or amorphized its crystalline quality. Similarly, the free face 30a of the carrier substrate 30 has a polycrystalline surface, unmodified or amorphized by any implantation doping or atomic bombardment activation.

10 [0082] The metal material can be selected from the following non-limiting list of materials: tungsten, titanium, nickel, aluminum, molybdenum, niobium, tantalum, cobalt, copper; the semiconductor material can be selected from the following non-limiting list: silicon, germanium, carbon, III-V compounds such as gallium nitride, or other compounds formed from these materials (SiGe, SiGeC, etc.).

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[0083] The film 2 has a thickness of less than or equal to 20 nm, preferentially less than or equal to 10 nm, or even less than or equal to 5 nm. For example, the deposited film 2 may have a thickness of the order of 0.5 nm, 1 nm, 2 nm, 3 nm, 4 nm, 5 nm, 8 nm, 10 nm or 15 nm.

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[0084] Note that when a film 2 is deposited on the two free faces 10a, 30a, the total deposited thickness, i.e. the sum of the thicknesses of the film 2 deposited on one and the other free faces 10a, 30a is preferentially less than or equal to 20 nm, or even less than or equal to 10 nm. The total thickness of
25 deposited film 2 is always kept low, so as to allow a segmentation of the film in the form of nodules 21, in a subsequent step of the method.

[0085] The film 2 is deposited under a non-oxidizing controlled atmosphere. It is important that the film 2 does not undergo oxidation or is not degraded by
30 pollution from the surrounding atmosphere. Typically, the deposition in step c) is carried out under a high vacuum, of the order of 10^{-6} Pa or less.

[0086] Depending on the nature of the deposited film 2, step c) is carried out at room temperature or at low temperature, advantageously by a sputter deposition technique using, to bombard the metal target, an element which is neutral or whose residual presence in the deposited metal is not
5 troublesome (Ar, Si, N, etc.).

[0087] According to a particular embodiment, the manufacturing method according to the invention comprises, prior to the deposition step c), a deoxidation step c') of the free face to be assembled 10a of the working
10 layer 10 and/or of the free face to be assembled 30a of the carrier substrate 30. Such a step removes the native oxide potential present on the surface of the working layer 10 and/or of the carrier substrate 30. Deoxidation can be carried out by wet chemical treatment (for example HF etching) or dry treatment (dry etching or annealing in a reducing atmosphere).

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[0088] The manufacturing method then comprises a step d) of forming an intermediate structure 150, said step comprises a direct assembly of the free faces to be assembled 10a, 30a respectively of the working layer 10 and of the carrier substrate 30, at an assembly interface 15 ([Fig. 2d]).

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[0089] This direct assembly is preferentially carried out by molecular-adhesion bonding, consisting of bringing the faces to be assembled 10a, 30a into contact, under a non-oxidizing controlled atmosphere. This could be direct bonding between the working layer 10 and the film 2, when the latter has only
25 been deposited on the carrier substrate 30, or direct bonding between the carrier substrate 30 and the film 2, when the latter has only been deposited on the working layer 10, or direct bonding between two films 2, when they have been deposited on the working layer 10 and on the carrier substrate 30.

30 [0090] Direct bonding is preferentially carried out under a high vacuum, of the order of 10^{-6} Pa or less.

[0091] Advantageously, the deposition of step c) and the direct bonding of step d) are linked without breaking the vacuum, in situ or in a multi-chamber apparatus. By way of example, mention will be made of Atomic Diffusion Bonding BV7000 from the company Canon, wherein it is possible to
5 successively carry out the deposition of the film 2' and direct bonding, by maintaining a controlled atmosphere.

[0092] Referring to the advantageous embodiment shown in Figures 3a to 3d, step d) comprising the direct assembly of the free face to be assembled 10a
10 of the working layer 10 on the free face to be assembled 30a of the carrier substrate 30, gives rise to a bonded assembly 200 that includes the donor substrate 1, the carrier substrate 30, and the assembly interface 15 ([Fig. 3c]). Step d) further comprises a separation at the buried fragile plane 11 in order to form, on the one hand, the intermediate structure 150 comprising the
15 working layer 10, the film(s) 2 and the carrier substrate 30 and, on the other hand, the rest of the donor substrate 1" ([Fig. 3d]). Such a separation can be carried out during a heat treatment capable of growing cavities and microcracks, induced by the implanted species, in the buried fragile plane 11. The separation can also be carried out by applying mechanical stress, or else
20 by the combination of thermal and mechanical stresses, as is well known in reference to the Smart Cut™ method.

[0093] Sequences for cleaning, smoothing, polishing or etching the separate face 10b of the working layer 10 and/or of the separate face 1" a of the rest of
25 the donor substrate 1" may be able to be carried out so as to restore a good surface quality, notably in terms of roughness, defectivity and other contaminations.

[0094] Regardless of the embodiment of the method, at the end of step d), the
30 intermediate structure 150 has a front face 10b on the side of the working layer 10, a rear face 30b on the side of the carrier substrate 30, and an encapsulated film 2' between the working layer 10 and the carrier substrate 30.

It should be noted that the encapsulated film 2' corresponds to the film 2 when the latter has only been deposited on one of the free faces 10a, 30a to be assembled, or corresponds to the two films 2 deposited on the working layer 10 and on the carrier substrate 30, respectively.

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[0095] The manufacturing method according to the invention then comprises a step e) of annealing the intermediate structure 150 at a temperature of between 1200°C and 2000°C, preferentially around 1700°C, so as to cause segmentation of the encapsulated film 2' in the form of nodules 21 and diffusion of the dopants from the carrier substrate 30 (very heavily doped) into the regions of direct contact 22 and optionally into the nodules 21. Step e) results in the formation of the semiconductor structure 100 with its interface zone 20 between the carrier substrate 30 and the working layer 10, said interface zone 20 including said nodules 21 and said regions of direct contact 22 ([Fig. 2e]).

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[0096] The annealing temperature of step e) is selected such that the system including the encapsulated film 2' and the semiconductor surfaces of the working layer 10 and of the carrier substrate 30 in contact with said film 2' will optimize its surface energy by agglomerating the encapsulated film 2' in the form of nodules 21 and by creating regions of direct contact 22 between the semiconductor surfaces respectively of the working layer 10 and of the carrier substrate 30. This temperature is also set to enable the closure of a bonding interface in the regions of direct contact 22, between the monocrystalline silicon carbide of the working layer 10 and the polycrystalline silicon carbide of the carrier substrate 30. Moreover, the annealing temperature is capable of diffusing the dopants from the carrier substrate 30 into the regions of direct contact 22 and potentially into the nodules 21 (particularly when these are made of semiconductor material).

30 [0097] Given the steep gradient in dopant concentration between the working layer 10 and the carrier substrate 30 (which results from the relationship between the first C_1 and second C_2 concentrations, shown on the curve in

[Fig.5), the dopants diffuse very efficiently towards the working layer 10, and segregation occurs at the interfaces present in the interface zone 20, namely the interface between the monocrystalline SiC and the polycrystalline SiC, at each region of direct contact 22, and the interface between the material of the nodules 21 and the polycrystalline SiC. The quantity of dopants able to segregate at these interfaces is far greater than the quantity of dopants able to diffuse into the working layer (related to the solubility of the dopant in monocrystalline SiC). Notably, the interface between mono-SiC and poly-SiC in the regions of direct contact 22 can be considered as a very extensive grain boundary on which dopants are concentrated, preferentially at the SiC volume. As this interface has a certain roughness (related notably to the presence of poly-SiC grains), the dopants are distributed over a thickness of up to 5 nm on both sides of the mono-SiC/poly-SiC interface.

[0098] The material making up the nodules 21 may also have a solubility of dopants greater than their solubility in SiC; this is the case, for example, when the material is silicon, at temperatures greater than its melting point.

[0099] A dopant concentration profile along a thickness of the semiconductor structure 100 can be measured using a known technique, for example SIMS (secondary ion mass spectrometry). The measurement point, in the plane of the interface zone 20, is sufficiently large to integrate and average the profile measurement over the various elements making up the interface zone 20 (namely, mainly the nodules 21 and the regions of direct contact 22).

[0100] The dopant concentration profile of the semiconductor structure 100 takes the form of a steep step, the transition of which coincides with the interface zone 20. The abruptness reflects the fact that there is no significant diffusion of dopants from the carrier substrate 30 into the working layer 10, which is highly advantageous in terms of the properties and stability of said layer 10. The profile is also devoid of doping peaks in the interface zone 20 or exhibits a doping peak in the interface zone 20, the extremum of which

corresponds to a third dopant concentration, equal to the second dopant concentration to within plus or minus 10%.

5 [0101] The regions of direct contact 22 are doped to a level similar to that of the carrier substrate 30 and have a resistivity of less than or equal to 0.01 mohm.cm², giving the interface zone a similar average resistivity overall.

10 [0102] The manufacturing method as described therefore produces a semiconductor structure 100 providing excellent vertical electrical conduction between the working layer 10 and the carrier substrate 30, via an interface zone 20 mainly composed of nodules 21 and regions of direct contact 22. The diffusion of dopants from the carrier substrate 30 (due to the strong dopant concentration gradient between the working layer 10 and the carrier substrate 30) and their segregation at the various interfaces of the interface zone 20 give the latter a very low resistivity.

[0103] Example embodiment:

20 [0104] The donor substrate 1 is made of high-quality, monocrystalline 4H SiC with a diameter of 150 mm. The donor substrate 1 is N-doped, with a resistivity of the order of 20 mohm.cm (first concentration of C₁ dopants: 4.10¹⁸ cm⁻³). It is implanted through its front face 1a, a "C" type face, with hydrogen ions at a dose of 5.10¹⁶ cm⁻² and an energy of 95 keV. Around the implantation depth, a buried fragile plane 11 is thus defined, delimiting, with the front face 10a of the donor substrate 1, the working layer 10.

[0105] The carrier substrate 30 is made of polycrystalline 3C SiC, of the same diameter as the donor substrate 1. It is N-doped, with a resistivity of the order of 3 mohm.cm (i.e. a second C₂ dopant concentration of 5.10²⁰ cm⁻³).

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[0106] Both the substrates 1, 30 undergo cleaning sequences in order to remove the particles and other surface contaminations. The sequences are

preferentially selected so that the surfaces of substrates 1, 30 do not undergo oxidation (absence of native oxide).

5 [0107] The substrates 1, 30 are introduced into a first deposition chamber, integrated into direct bonding equipment. A silicon film 2 having a thickness of 10 nm is deposited on each of the front faces 10a, 30a (free faces to be assembled) of the substrates 1, 30 under a vacuum, at 10^{-6} Pa and room temperature, by sputtering. The substrates 1, 30 are then introduced into a second bonding chamber in order to be assembled at their front faces 10a, 10 30a by bringing the films 2 deposited on the donor substrate 1 and on the carrier substrate 30, respectively, into direct contact. The atmosphere in the bonding chamber is the same as that in the deposition chamber, which avoids any oxidation or passivation of the surface of the films 2.

15 [0108] After assembly, the bonded assembly 200 comprises the donor substrate 1 connected to the carrier substrate 30 via a bonding interface 15, and the encapsulated film 2' formed of the two films 2 deposited and buried between the two substrates 1, 30. The encapsulated film 2' has a thickness of the order of 20 nm.

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[0109] The bonded assembly 200 is subjected to a heat treatment to cause separation at the buried fragile plane 11, at a temperature between 800°C and 1000°C for a few minutes to a few hours. The intermediate structure 150 including a working layer 10 having a thickness of 500 nm is then obtained, 25 arranged on the encapsulated film 2', itself arranged on the carrier substrate 30. Cleaning and polishing sequences are applied so as to restore the right level of defectiveness and roughness to the surface 10b of the working layer 10.

[0110] Finally, annealing at 1700°C for 30 minutes is applied to the 30 intermediate structure 150, which was previously provided with a protective layer on its front face 10b (also free face 10b of the working layer 10 in the intermediate structure 150). At the end of this annealing, the structure 100

according to the invention is obtained: the interface zone 20 formed of silicon nodules 21 and regions of direct contact 22, between the working layer 10 and carrier substrate 30, gives the structure 100 an excellent vertical electrical conductivity (average resistivity of the interface zone of the order of 5 0.01 mohm.cm²) due to the segregation of dopants from the carrier substrate 30 at the various interfaces of the interface zone 20.

[0111] The nodules 21 in this structure 100 have a thickness of the order of 200 nm and an average diameter of the order of 100 nm to 1 µm. The degree 10 of coverage of the regions of direct contact 22 in a median plane of the interface zone 20 is of the order of 80%. The dopant concentration profile according to the thickness of the semiconductor structure 100 takes the form of a steep step, with no significant change in the uniform concentration profile of the working layer 10.

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[0112] Of course, the invention is not limited to the embodiments described and it is possible to add alternative embodiments thereto without departing from the scope of the invention as defined by the claims.

Claims

[Claim 1] A semiconductor structure (100) based on silicon carbide-based comprising:

- 5 - a working layer (10) made of monocrystalline silicon carbide having a first dopant concentration (C_1) that is uniform over its thickness,
- a carrier substrate (30) made of polycrystalline silicon carbide having a second dopant concentration (C_2) that is uniform over its thickness, the second concentration (C_2) being related to the first concentration (C_1) by the
- 10 following relationship: $C_2 > N_2 \times \exp(-C_1/N_1)$ with $N_1 = 2.85.10^{18} \text{ cm}^{-3}$ and $N_2 = 5.40.10^{20} \text{ cm}^{-3}$,
- an interface zone (20), between the carrier substrate (30) and the working layer (10), comprising nodules (21) and regions of direct contact (22) between the working layer (10) and the carrier substrate (30), the nodules (21)
- 15 comprising a metal or semiconductor material other than silicon carbide, the interface zone (20) having an average resistivity of less than or equal to 0.01 mohm.cm^2 ,
- a dopant concentration profile along a thickness of the semiconductor structure (100):
- 20 - in the form of a step, and
- being devoid of a doping peak in the interface zone (20), or
- exhibiting a doping peak in the interface zone (20), the extremum of which corresponds to a third dopant concentration equal to the second dopant concentration to within plus or minus 10%.

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[Claim 2] The semiconductor structure (100) according to one of the preceding claims, wherein the resistivity of the carrier substrate is less than or equal to 10 mohm.cm , 5 mohm.cm , even 3 mohm.cm or even 2 mohm.cm .

- 30 [Claim 3] The semiconductor structure (100) according to one of the preceding claims, wherein the interface zone has a thickness of less than or equal to 200 nm .

[Claim 4] The semiconductor structure (100) according to one of the preceding claims, wherein:

- the metal material of the nodules (21) is selected from tungsten, titanium,
5 nickel, aluminum, molybdenum, niobium, tantalum, cobalt and copper, or
- the semiconductor material of the nodules (21) is selected from silicon, germanium, carbon, III-V compounds such as gallium nitride or other compounds formed from these materials.

10 [Claim 5] A method for manufacturing a semiconductor structure (100) based on silicon carbide comprising the following steps:

- a) providing a working layer (10) made of monocrystalline silicon carbide having a free face to be assembled and a first dopant concentration (C_1) that is uniform over its thickness,
- 15 b) providing a carrier substrate (30) made of polycrystalline silicon carbide having a free face to be assembled, a second dopant concentration (C_2) that is uniform over its thickness, the second concentration (C_2) being related to the first concentration (C_1) by the following relationship: $C_2 > N_2 \times \exp(-C_1/N_1)$ with $N_1 = 2.85 \cdot 10^{18} \text{ cm}^{-3}$ and $N_2 = 5.40 \cdot 10^{20} \text{ cm}^{-3}$,
- 20 c) depositing a film (2) of a metal or semiconductor material other than silicon carbide, having a thickness of 20 nm or less, on the free face of the working layer (10) to be assembled and/or on the free face of the carrier substrate (30) to be assembled,
- d) forming an intermediate structure (150), comprising direct assembly
25 of the free faces to be assembled of the working layer (10) and of the carrier substrate (30) respectively, the intermediate structure (150) including an encapsulated film (2') originating from the one or more film(s) (2) deposited during step c),
- e) annealing the intermediate structure (150) at a temperature of
30 between 1200°C and 2000°C, to form the semiconductor structure (100) comprising an interface zone (20) which includes nodules (21) resulting from

the segmentation of the encapsulated film (2') and regions of direct contact (22) between the thin layer (10) and the carrier substrate (30),

- the interface zone (20) having an average resistivity of less than or equal to 0.01 mohm.cm²,

- 5 - a dopant concentration profile along a thickness of the semiconductor structure (100) in the form of a step, and being devoid of a doping peak in the interface zone (20) or exhibiting a doping peak in the interface zone (20), the extremum of which corresponds to a third dopant concentration equal to the second dopant concentration (C₂) to within plus or minus 10%.

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[Claim 6] The manufacturing method according to claim 5, wherein step a) comprises an implantation of light species in a donor substrate (1) made of monocrystalline silicon carbide, to form a buried fragile plane (11) which delimits, with a front face of the donor substrate (1), the working layer (10).

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[Claim 7] The manufacturing method according to one of claims 5 and 6, wherein step d) comprises, after the direct assembly giving rise to a bonded assembly (200) comprising the donor substrate (1) and the carrier substrate (30), a separation at the buried fragile plane (11) in order to form, on the one

20 hand, the intermediate structure (150) comprising the working layer (10), the encapsulated film (2') and the carrier substrate (30) and, on the other hand, the rest of the donor substrate (1").

[Claim 8] The manufacturing method according to one of claims 5 to 7,

25 wherein, prior to step c), the free face to be assembled of the thin film (10) has a monocrystalline surface, devoid of zones amorphized or damaged by doping or bombardment activation, and the free face to be assembled of the carrier substrate (30) has a polycrystalline surface, devoid of zones amorphized or modified by doping or bombardment activation.

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[Claim 9] The manufacturing method according to one of claims 5 to 8, comprising a step of epitaxial growth of an additional layer of monocrystalline silicon carbide on the working layer (10) of the semiconductor structure (100).