WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a memory comprising

a memory stack,

a memory cell interconnection comprising a plurality of upper conductive patterns configured to be electrically connectable to the memory stack, and

a memory cell insulation surrounding the memory stack and the memory cell interconnection;

a peripheral circuit comprising

a peripheral circuit board,

a peripheral circuit region on the peripheral circuit board, and

a peripheral circuit interconnection comprising a plurality of lower conductive patterns between the peripheral circuit region and the memory and bonded to the memory cell interconnection;

a plurality of conductive bonding structures on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in a vertical direction, the plurality of conductive bonding structures being a bonded resultant of a plurality of first upper conductive patterns selected from among the plurality of upper conductive patterns and a respective plurality of first lower conductive patterns selected from among the plurality of lower conductive patterns; and

a through electrode penetrating one of the memory cell insulation and the peripheral circuit board and extended to a second lower conductive pattern selected from among the plurality of lower conductive patterns in the vertical direction, in a second region, the second region overlapping the memory cell insulation in the vertical direction.

2. The integrated circuit device of claim 1, wherein

the through electrode penetrates the memory cell insulation and extends to the second lower conductive pattern.

3. The integrated circuit device of claim 1, wherein

the through electrode penetrates the peripheral circuit board and the peripheral circuit region and extends to the second lower conductive pattern.

4. The integrated circuit device of any one of claims 1 to 3, wherein

the first lower conductive pattern and the second lower conductive pattern are at different levels.

5. The integrated circuit device of any one of claims 1 to 3, wherein

the first lower conductive pattern and the second lower conductive pattern are at the same level.

6. The integrated circuit device of any one of claims 1 to 5, wherein

the first lower conductive pattern and the second lower conductive pattern comprise different metals.

7. The integrated circuit device of any one of claims 1 to 5, wherein

the first lower conductive pattern and the second lower conductive pattern comprise the same metal.

8. The integrated circuit device of any one of claims 1 to 7, wherein

each of the first lower conductive pattern and the second lower conductive pattern has a shape in which a width in a horizontal direction increases as the first lower conductive pattern and the second lower conductive pattern respectively becomes closer toward the memory.

9. The integrated circuit device of any one of claims 1 to 7, wherein

the first lower conductive pattern has a shape in which a width in a horizontal direction increases as the first lower conductive pattern becomes closer toward the memory, and

the second lower conductive pattern has a shape in which a width in the horizontal direction decreases as the second lower conductive pattern becomes closer toward the memory.

10. The integrated circuit device of any one of claims 1 to 9, further comprising

a conductive pad in contact with the through electrode and extending in a horizontal direction outside of the memory,

wherein the conductive pad comprises a portion overlapping the memory stack in the vertical direction.

11. The integrated circuit device of any one of claims 1 to 9, further comprising

a conductive pad in contact with the through electrode and extending in a horizontal direction outside of the peripheral circuit, wherein the conductive pad is spaced apart from the peripheral circuit region with the peripheral circuit board therebetween.

12. An integrated circuit device comprising:

a memory comprising

a memory stack comprising

a plurality of bit lines extending in a first horizontal direction,

a memory cell interconnection comprising a plurality of upper conductive patterns configured to be electrically connectable to the plurality of bit lines, and

a memory cell insulation surrounding the memory stack and the memory cell interconnection;

a peripheral circuit comprising

a peripheral circuit board,

a peripheral circuit region on the peripheral circuit board, and

a peripheral circuit interconnection comprising a plurality of lower conductive patterns between the peripheral circuit region and the memory and bonded to the memory cell interconnection;

a conductive bonding on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in a vertical direction, the conductive bonding being a bonded resultant of a first upper conductive pattern selected from among the plurality of upper conductive patterns and a first lower conductive pattern selected from among the plurality of lower conductive patterns; and

a plurality of through electrodes extended in the vertical direction through one of the memory cell insulation and the peripheral circuit board, in a second region spaced apart from the first region in a horizontal direction,

wherein the plurality of through electrodes comprise a plurality of first through electrodes arranged in a line along the first horizontal direction in the second region.

13. The integrated circuit device of claim 12, wherein

the plurality of through electrodes further comprise a plurality of second through electrodes arranged in a line along a second horizontal direction perpendicular to the first horizontal direction in the second region.

14. The integrated circuit device of claim 12 or claim 13, wherein

the plurality of through electrodes comprise one through electrode in contact with a second lower conductive pattern selected from among the plurality of lower conductive patterns, and

the one through electrode extends to the second lower conductive pattern through the memory cell insulation.

15. The integrated circuit device of claim 12 or claim 13, wherein

the plurality of through electrodes comprise one through electrode in contact with a second lower conductive pattern selected from among the plurality of lower conductive patterns, and

the one through electrode extends to the second lower conductive pattern through the peripheral circuit board and the peripheral circuit region.

16. The integrated circuit device of claim 15, wherein

a first shortest distance from the peripheral circuit board to the first lower conductive pattern is greater than a second shortest distance from the peripheral circuit board to the second lower conductive pattern.

17. The integrated circuit device of claim 15, wherein

a first shortest distance from the peripheral circuit board to the first lower conductive pattern is the same as a second shortest distance from the peripheral circuit board to the second lower conductive pattern.

18. The integrated circuit device of any one of claims 15 to 17, wherein

the first lower conductive pattern and the second lower conductive pattern comprise different metals.

19. An integrated circuit device comprising:

a memory comprising

a semiconductor layer,

a memory stack on the semiconductor layer,

a memory cell interconnection comprising a plurality of upper conductive patterns overlapping the memory stack in a vertical direction and configured to be electrically connectable to the memory stack, and

a memory cell insulation surrounding the semiconductor layer, the memory stack, and the memory cell interconnection;

a peripheral circuit comprising

a peripheral circuit board,

a peripheral circuit region on the peripheral circuit board, and

a peripheral circuit interconnection between the peripheral circuit region and the memory and bonded to the memory cell interconnection;

a plurality of conductive bonding structures comprising Cu and on a boundary between the memory cell interconnection and the peripheral circuit interconnection in a first region, the first region overlapping the memory stack in the vertical direction;

a plurality of lower conductive patterns comprising at least one metal selected from among Al, W, and Cu and in the peripheral circuit interconnection in a second region, the second region overlapping the memory cell insulation in the vertical direction; and

a through electrode penetrating one of the memory cell insulation and the peripheral circuit board in the second region and contacting one lower conductive pattern among the plurality of lower conductive patterns.

20. The integrated circuit device of claim 19, wherein

the plurality of lower conductive patterns comprise a first lower conductive pattern constituting the plurality of conductive bonding structures and a second lower conductive pattern in contact with the through electrode,

the first lower conductive pattern has a shape in which a width in a horizontal direction increases as the first lower conductive pattern becomes closer toward the memory, and

the second lower conductive pattern has a shape in which a width in the horizontal direction decreases as the second lower conductive pattern becomes closer toward the memory.