METHODS OF FORMING FIELD EFFECT TRANSISTORS HAVING STRESS-INDUCING SIDEWALL INSULATING SPACERS THEREON

Abstract of the Disclosure

Methods of forming integrated circuit devices include forming a field effect transistor having a gate electrode, a sacrificial spacer on a sidewall of the gate electrode and silicided source/drain regions. The sacrificial spacer is used as an implantation mask when forming highly doped portions of the source/drain regions. The sacrificial spacer is then removed from the sidewall of the gate electrode. A stress-inducing electrically insulating layer, which is configured to induce a net tensile stress (for NMOS transistors) or compressive stress (for PMOS transistors) in a channel region of the field effect transistor, is then formed on the sidewall of the gate electrode.

Figure 10