CIRCUIT FOR RECEIVING DATA, SYSTEM FOR RECEIVING DATA, AND MEMORY DEVICE

Technical Field

Embodiments of the present application relate to the technical field of semiconductors, and in particular, to a circuit for receiving data, a system for receiving data, and a memory device.

Background

In memory applications, as a signal transmission rate becomes increasingly fast, a channel loss has a greater impact on signal quality, which easily leads to intersymbol interference. In addition, a difference in level between a data signal received by a circuit for receiving data in a memory and a reference signal affects judgment of the circuit for receiving data on the data signal, thereby affecting accuracy of a signal outputted by the circuit for receiving data.

At present, an equalization circuit is usually configured to compensate for a channel, and the equalization circuit may select a continuous time linear equalizer (CTLE) or a decision feedback equalizer (DFE). However, the accuracy of the signal outputted by the equalization circuit currently used needs to be improved, receiving performance of the equalization circuit needs to be enhanced, and the processing speed of the equalization circuit to the data signal needs to be accelerated.