PATENT SPECIFICATION (11) 1343473

1343473

(21) Application No. 16888/71 (22) Filed 25 May 1971

(31) Convention Application No. 44391 (32) Filed 8 June 1970 in

(33) United States of America (US)

(44) Complete Specification published 9 Jan. 1974

(51) International Classification H01L 7/10

(52) Index at acceptance

H1K 211 217 225 312 38Y 412 413 417 41Y 421 422 424 469 491 52Y 593

(19)



(54) IMPROVEMENTS IN CERAMIC PASSIVATED SEMICONDUCTOR DEVICE AND PROCESS FOR ITS MANUFACTURE

(71) We, GENERAL ELECTRIC COMPANY, a corporation organised and existing under the laws of the State of New York, United States of America, residing at 1 River Road, Schenectady 12305, State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the manufacture of semi-conductor devices.

Silicon semi-conductor devices are known to the art which utilise glass both as a junction passivant and as an entire insulative hermetic housing for the silicon semi-conductive element: A typical example is the A14 rectifier sold by the General Electric Company. While this hermetic encapsulation approach is highly successful for relatively low hermetic housing for the silicon semi-contive element devices, the differences in the thermal coefficients of expansion of the silicon and glass passivant preclude this approach from being applied to the manufacture of devices where the silicon semi-conductive element approaches 150 mils in width, since larger elements produce much larger stresses in the glass.

Typically the otherwise suitable soft glasses—i.e., those having a firing or softening temperature below 700°C—exhibit a thermal coefficient of expansion that is too high for larger silicon semiconductive elements. While a number of glasses have been identified which have a thermal coefficient of expansion which sufficiently matches that of silicon, these glasses have proven generally unsuitable for direct bonding to silicon either because of extremely high fusion temperatures—typically above 900°C, or because of degradation of the electronic properties of the silicon semi-conductive elements at their junctions.

According to the present invention there is provided a semi-conductor device including a silicon semi-conductive element having a junction which intersects a face of said element, a protective body over-lying said face and comprising a fired aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially 45×10^{-7}/°C, and discrete metal oxide particles substantially free from mobile alkali atoms and having a thermal coefficient of expansion below that of silicon and present in an amount sufficient to reduce the thermal coefficient of expansion of said aggregate below that of said glass passivant, said metal oxide particles being suspended throughout the glass passivant and being non-reactive with said glass.

In another aspect the invention provides a semi-conductive device including a silicon semi-conductive element having a junction which intersects a face of said element, and a protective body overlying said face and comprising an alkali migration barrier associated with said face and, overlying said barrier a fired aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially 45×10^{-7}/°C, and discrete metal oxide particles having an alkali content of less than substantially 5% by weight and having a thermal coefficient of expansion below that of silicon, said metal oxide particles being suspended throughout the glass passivant and being non-reactive with said glass.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawing, in which:—

Figure 1 is a schematic vertical section of one embodiment of the invention, and

Figure 2 is a schematic vertical section of a second embodiment of the invention.

For ease of illustration, in both of the figures, the thickness of the semiconductive elements is exaggerated as compared to their

width. Additionally, sectioning is omitted from the semiconductive elements to avoid unduly cluttering the drawings.

Noting Figure 1, a semiconductor device 100 is shown including a silicon semiconductive element 102. The semiconductive element is provided with first and second opposed major surfaces 104 and 106, respectively. A junction 108 is located within the semiconductive element which intersects a peripheral edge 118. The portion of the semiconductive element lying between the junction and the first major surface may be of one conductivity type while the remainder of the semiconductive element is of an opposite conductivity type. A first electrode 110 is conductively associated with the first major surface by a contact 112 while a second electrode 114 is similarly conductively associated with the second major surface by a contact 116. The electrodes and contacts may be of any conventional construction and may be each formed of one or a plurality of elements or layer. In the preferred form the electrodes are refractory metal back up plates having a thermal coefficient of expansion of less than 55×10^{-7}/°C e.g. molybdenum or tungsten. This minimizes the thermally induced stresses transmitted from the electrodes to the semiconductive element and also facilitates passivant bonding, as is explained below. The contacts may include either a hard or soft solder for the refractory back up plates. In the preferred form the peripheral edge 118 is beveled to spread the surface field associated with the junction. The peripheral edge may be either positively or negatively beveled, as is well understood in the art. The advantages of beveling the peripheral surface are fully discussed, for example, in Davies et al United States Patent No. 3,491,272, issued January 20, 1970, the disclosure of which is here incorporated by reference. It is, of course, not essential that the peripheral edge be either positively or negatively beveled.

A dielectric protective body 120 is bonded to the peripheral edge of the silicon semiconductive element. The protective body preferably exhibits a dielectric strength of at least 100 volts/mil and a resistivity of at least 10^{10} ohm-cm. The protective body exhibits a thermal coefficient of expansion which is lower than that obtainable with conventional soft glass passivants. Preferably the protective body is formed with a thermal coefficient of expansion which approximates that of the silicon semiconductive element. In this regard it is to be noted that the thermal coefficient of expansion of monocrystalline silicon has been measured within the range of from $30—37\times10^{-7}$/°C, depending on the crystallographic plane chosen. An exact match of the thermal coefficients of expansion of the protective body and the silicon element is not necessary to achieve the advantages of the invention and in most instances is not practical.

The protective body may be formed according to the invention by mixing together in particulate form a conventional soft glass passivant such as a zinc borosilicate glass and a substantially mobile alkali free metal oxide. Exemplary conventional soft glass passivants are disclosed in Claypoole United States Patent No. 2,889,952, Martin United States Patent No. 3,420,685, and Graff United States Patent No. 3,441,422, the disclosures of which are here incorporated by reference. The term "soft glass" as herein employed refers to a glass that has a firing (or softening) temperature below 700°C. Such glasses can be fired to the edge of the silicon semiconductive elements without degradation of the physical or electrical characteristics of these elements. While all available soft glass passivants have thermal coefficients of expansion well in excess of that of silicon, some have very high thermal coefficients of expansion. Accordingly, it is preferred to utilize in the practice of the present invention only those glass passivants having thermal coefficients of expansion of 45×10^{-7}/°C or less. As employed throughout this specificaiton the "thermal coefficient of expansion" refers to the average linear thermal coefficient of expansion and, like other parameters given, is taken over the normal range of device operating temperatures—i.e., from 0 to 300°C.

In a preferred form the metal oxide particles are amorphous silica particles. Amorphous silica particles are particularly advantageous, since they exhibit an extremely low thermal coefficient of expansion—less than 15×10^{-7}/°C. Instead of silica particles, particles of conventional substantially mobile alkali free glasses having thermal coefficients of expansion less than silicon may be utilized. A variety of such glasses are commercially available. Examplary suitable glasses are set out in Table I. The ingredients not listed are metal oxide impurities.

TABLE I

Commercial Name	Thermal Coefficient $\times10^{-7}$/°C	Principal Ingredients—wt % Al_2O_3	B_2O_3	SiO_2
GE-GSC1	12.8	5.4	11.3	82.6
GE-GSC2	16.8	4.8	10.5	83.5
GE-GSC3	13.3	5.1	12.1	81.9
GE-GSC4	22.4	1.1	17.6	79.9

These glasses all have firing temperatures above 700°C and are defined in this application as hard glasses. While it is preferred to utilize substantially alkali free glasses, it is recognized that alkali atoms are detrimental only to the extent that they are mobile. Alkali may be incorporated within the hard glasses where it is present in a chemically bound form that obviates alkali atom or ion migration. It is preferred to utilize hard glasses having less than about 5% by weight total alkali content.

In order to form the protective body we comminute and mix the soft glass passivant and metal oxide particles. While particle size is not critical, we prefer to utilize particles that pass through 100 mesh screen, preferably 300 mesh screen. It is preferred that the soft glass particles be sized below the metal oxide particles in order to facilitate bonding. It is also recognized that the available surface to weight relationship of the metal oxide and glass particles can be adjusted by controlling the particle sizes. The proportion of metal oxide particles to soft glass particles can be varied widely. It is generally preferred to incorporate the minimum amount of metal oxide particles necessary to achieve the desired thermal coefficient of expansion for the protective body. Generally the soft glass and metal oxide particles are utilized in a weight ratio of 8:1 or greater. It is appreciated that the advantages of the invention can be realized in reducing the thermal coefficient of expansion of the protective body below that of the soft glass merely by incorporating very small amounts of metal oxide particles.

In a preferred form the mixed aggregate of soft glass and metal oxide particles is positioned on a junction intersected edge of a monocrystalline silicon element and fired to the softening temperature of the soft glass or slightly thereabove. A volatilizable carrier, such as deionized water or a conventional organic liquid carrier, can be utilized to form the aggregate of particles into an easily positionable slurry. The carrier can be removed by drying or baking to leave the aggregate in the desired location on the semiconductive element. The aggregate is then heated to the firing temperature of the soft glass passivant to form the protective body. The aggregate can be fired in the same manner in which glass frit is conventionally fired.

In working with metal oxide particles having low but significant alkali contents—up to 5% by weight—which may be incidentally included either in material formation or in subsequent comminution or handling, we have observed that such alkali contaminated particles may be successfully utilized to form semiconductor devices according to the invention, if steps are taken to provide a barrier to alkali migration into the semiconductive element. According to one approach the semiconductive element may be preliminarily oxidized to produce an oxide layer on the edge adjacent the junction to be passivated. For example, the semiconductive element may be placed in boiling nitric acid. Other techniques are known to the art for laying down silicon oxide layers and may be utilized. The oxide layer acts as a barrier to alkali migration into the semiconductive element. As an alternative to forming an oxide layer on the edge of the semiconductive element prior to positioning of the aggregate, it has also been discovered that a decomposable compound of a metal, such as lead or arsenic, capable of stimulating oxide formation at the edge of the silicon element may be utilized. For example, by saturating the deionized water used as a carrier with a material, such as a lead or arsenic halide, an alkali migration barrier may be formed, since the metal halide will thermally decompose below the firing temperature of the soft glass and react with the silicon at the edge of the semiconductive element to accelerate oxidation thereof. The result is the same in that an alkali migration barrier is formed prior to reaching temperatures above about 500°C at which alkali would migrate rapidly into the silicon. The approach of preliminarly forming the oxide layer as a migration barrier prior to application of the aggregate has the advantage of giving the best electrical performance. We have observed that the use of an alkali migration barrier can be relied upon to completely eliminate junction downgrading in the process of applying the protective body and, surprisingly, we have even observed significant improvements in junction voltage blocking characteristics. However, preliminary formation of the barrier layer adds an additional process step, which may not in all cases be economically acceptable. Further, where an oxide formation technique is utilized, such as exposure to nitric acid, it is necessary that the protective body processing be undertaken before contacts are applied to the silicon element. Where the alkali migration barrier is formed during the firing step as the result of incorporating an oxidation accelerating material, we have observed some downgrading of junction blocking characteristics, typically less than 10%, but the extent of downgrading has been significantly reduced below that observed for devices formed without alkali migration barriers, but with comparable alkali contents. The alkali migration barrier is in most instances taken into solution by the soft glass passivant at its firing temperature, so that it is not present as a distinct element in the fired protective body.

In the device configuration shown in Figure 1 the protective body is not only bonded

to the edge of the semiconductive element, but is also bonded to the periphery of the refractory back up plates. Thus, the electrodes and protective body together hermetically encase the semiconductive element. This obviates any necessity of further packaging the device. It is, of course, recognized that other packaging or protective layers could be added to the device, if desired. For example, the device shown could be mounted in a hermetically sealed case or potted in a plastic dielectric according to techniques well understood in the art. When additional protective packaging is contemplated, it is appreciated that mechanical irregularities may be permitted in the protective body rendering it less than entirely fluid impervious.

Where the protective body contains mechanical irregularities rendering it unsuitable to act as a hermetic barrier (or where doubts exist), it may be desirable to modify the construction of our semiconductor device as shown in Fig. 2. Elements of the semiconductor device 200 identical to those of the semiconductor device 100 are assigned like reference numerals and are not redescribed. The protective body 220 may be identical to protective body 120 or differ therefrom in the manner above noted. The layer 222 in the preferred form of my invention is a glaze formed of a soft glass passivant. The glaze may be applied according to conventional techniques after the protective body is formed by firing. Since it is not necessary to heat the entire device to the firing temperature of the glaze, the protective body does not necessarily receive a second firing. Normally the glaze is chosen to have a thermal coefficient of expansion of 45×10^{-7}/°C or less, similarly as the soft glass passivant utilized in the protective body, but it is appreciated that where the thermal coefficient of expansion of the protective body exceeds that of the semiconductive element a higher thermal coefficient of expansion may be tolerated for the glaze. Instead of utilizing a conventional soft glass passivant to form the glaze it is appreciated that a variety of other glasses having a firing temperature at or below that of the soft glass passivant incorporated in the protective body may be utilized. Since the glaze is separated from the semiconductive element by the protective body, the junction of the semiconductive element is much less sensitive to alkali contained within the glaze. It is accordingly contemplated that alkali contents of up to 5% by weight in the glaze may be tolerated whether or not an alkali migration barrier was originally present. In applying the glaze a portion of the protective body and/or glaze may devitrify to form a crystalline ceramic barrier at their interface. The devitrified layer lends additional mechanical strength to the composite structure.

While we have disclosed the invention with reference to certain preferred embodiments, it is appreciated that numerous variations will readily occur to those skilled in the art. For example, while for clarity we have discussed the invention with reference to a single junction device, a rectifier, it is appreciated that the invention could be readily applied to the construction of transistors, thyristors, and other single and multi-junction semiconductor devices requiring passivation of a junction at its intersection with an edge of a silicon element. It is accordingly intended that the scope of my invention be determined by reference to the following claims.

WHAT WE CLAIM IS:—

1. A semiconductor device including a silicon semiconductive element having a junction which intersects a face of said element, a protective body over-lying said face and comprising a fired aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially 45×10^{-7}/°C, and discrete metal oxide particles substantially free from mobile alkali atoms and having a thermal coefficient of expansion below that of silicon, said metal oxide particles being suspended throughout the glass passivant and being non-reactive with said glass.

2. A semiconductive device including a silicon semiconductive element having a junction which intersects a face of said element, and a protective body overlying said face and comprising an alkali migration barrier associated with said face and, overlying said barrier, a fired aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially 45×10^{-7}/°C, and discrete metal oxide particles having an alkali content of less than substantially 5% by weight and having a thermal coefficient of expansion below that of silicon, said metal oxide particles being suspended throughout the glass passivant and being non-reactive with said glass.

3. A semiconductor device as claimed in Claim 1 or Claim 2 including a pair of electrodes conductively associated with said element, said protective body being sealingly associated with said electrodes.

4. A semiconductor device as claimed in Claim 3 in which said protective body and said electrodes hermetically encapsulate said semiconductive element.

5. A semiconductor device as claimed in any one of Claims 1 to 4 in which said soft glass passivant is a zinc borosilicate glass.

6. A semiconductor device as claimed in any one of Claims 1 to 5 in which said metal oxide particles comprise amorphous silica particles.

7. A semiconductor device as claimed in

to the edge of the semiconductive element, but is also bonded to the periphery of the refractory back up plates. Thus, the electrodes and protective body together hermetically encase the semiconductive element. This obviates any necessity of further packaging the device. It is, of course, recognized that other packaging or protective layers could be added to the device, if desired. For example, the device shown could be mounted in a hermetically sealed case or potted in a plastic dielectric according to techniques well understood in the art. When additional protective packaging is contemplated, it is appreciated that mechanical irregularities may be permitted in the protective body rendering it less than entirely fluid impervious.

Where the protective body contains mechanical irregularities rendering it unsuitable to act as a hermetic barrier (or where doubts exist), it may be desirable to modify the construction of our semiconductor device as shown in Fig. 2. Elements of the semiconductor device 200 identical to those of the semiconductor device 100 are assigned like reference numerals and are not redescribed. The protective body 220 may be identical to protective body 120 or differ therefrom in the manner above noted. The layer 222 in the preferred form of my invention is a glaze formed of a soft glass passivant. The glaze may be applied according to conventional techniques after the protective body is formed by firing. Since it is not necessary to heat the entire device to the firing temperature of the glaze, the protective body does not necessarily receive a second firing. Normally the glaze is chosen to have a thermal coefficient of expansion of $45\times10^{-7}/°C$ or less, similarly as the soft glass passivant utilized in the protective body, but it is appreciated that where the thermal coefficient of expansion of the protective body exceeds that of the semiconductive element a higher thermal coefficient of expansion may be tolerated for the glaze. Instead of utilizing a conventional soft glass passivant to form the glaze it is appreciated that a variety of other glasses having a firing temperature at or below that of the soft glass passivant incorporated in the protective body may be utilized. Since the glaze is separated from the semiconductive element by the protective body, the junction of the semiconductive element is much less sensitive to alkali contained within the glaze. It is accordingly contemplated that alkali contents of up to 5% by weight in the glaze may be tolerated whether or not an alkali migration barrier was originally present. In applying the glaze a portion of the protective body and/or glaze may devitrify to form a crystalline ceramic barrier at their interface. The devitrified layer lends additional mechanical strength to the composite structure.

While we have disclosed the invention with reference to certain preferred embodiments, it is appreciated that numerous variations will readily occur to those skilled in the art. For example, while for clarity we have discussed the invention with reference to a single junction device, a rectifier, it is appreciated that the invention could be readily applied to the construction of transistors, thyristors, and other single and multi-junction semiconductor devices requiring passivation of a junction at its intersection with an edge of a silicon element. It is accordingly intended that the scope of my invention be determined by reference to the following claims.

WHAT WE CLAIM IS:—

1. A semiconductor device including a silicon semiconductive element having a junction which intersects a face of said element, a protective body over-lying said face and comprising a fired aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially $45\times10^{-7}/°C$, and discrete metal oxide particles substantially free from mobile alkali atoms and having a thermal coefficient of expansion below that of silicon, said metal oxide particles being suspended throughout the glass passivant and being non-reactive with said glass.

2. A semiconductive device including a silicon semiconductive element having a junction which intersects a face of said element, and a protective body overlying said face and comprising an alkali migration barrier associated with said face and, overlying said barrier, a fired aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially $45\times10^{-7}/°C$, and discrete metal oxide particles having an alkali content of less than substantially 5% by weight and having a thermal coefficient of expansion below that of silicon, said metal oxide particles being suspended throughout the glass passivant and being non-reactive with said glass.

3. A semiconductor device as claimed in Claim 1 or Claim 2 including a pair of electrodes conductively associated with said element, said protective body being sealingly associated with said electrodes.

4. A semiconductor device as claimed in Claim 3 in which said protective body and said electrodes hermetically encapsulate said semiconductive element.

5. A semiconductor device as claimed in any one of Claims 1 to 4 in which said soft glass passivant is a zinc borosilicate glass.

6. A semiconductor device as claimed in any one of Claims 1 to 5 in which said metal oxide particles comprise amorphous silica particles.

7. A semiconductor device as claimed in

* C L M S *

any one of Claims 1 to 5 in which said metal oxide particles comprise particles of a hard glass.

8. A semiconductor device as claimed in any one of Claims 1 to 7 in which said protective body exhibits a thermal coefficient of expansion substantially the same as that of silicon.

9. A semiconductor device as claimed in any one of Claims 1 to 8 including a glaze overlying said protective body.

10. A semiconductor device as claimed in Claim 9 wherein said glaze comprises a soft glass passivant.

11. A semiconductor device as claimed in Claim 9 or Claim 10 including a devitrified ceramic layer interposed between said glaze and said protective body.

12. A semiconductor device as claimed in Claim 2 or in any one of Claims 3 to 11 when dependent on Claim 2 in which said alkali migration barrier is a silica layer.

13. A method of making a semiconductor device comprising providing a semiconductive element having a junction which intersects a face of the element, disposing on said face an aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially 45×10^{-7}/°C and metal oxide particles substantially free from mobile alkali atoms and having a thermal coefficient of expansion below that of silicon, and heating the aggregate to the firing temperature of the glass passivant, said metal oxide particles, upon firing of said protective body, substantially retaining their identity and being suspended throughout the glass passivant and being non-reactive with said glass.

14. A method of making a semiconductor device comprising providing a semiconductive element having a junction which intersects a face of the element, providing on said face an alkali migration barrier, and providing over said barrier an aggregate comprising a soft glass passivant having a thermal coefficient of expansion in excess of that of silicon and below substantially 45×10^{-7}/°C, and metal oxide particles having an alkali content of less than substantially 5% by weight and having a thermal coefficient of expansion below that of silicon, and heating the aggregate to the firing temperature of the glass passivant, said metal oxide particles, upon firing of said protective body, substantially retaining their identity and being suspended throughout the glass passivant and being non-reactive with said glass.

15. A method as claimed in Claim 14 wherein the barrier is formed by oxidizing said face of the element.

16. A method as claimed in Claim 14 wherein the barrier is formed by mixing with the aggregate prior to firing a thermally decomposable compound of a metal capable of accelerating the oxidation of silicon.

17. A method as claimed in any one of Claims 13 to 16 including the step of securing electrodes to said element.

18. A method as claimed in any one of Claims 13 to 17 including the step of depositing a glaze onto the fired surface of said appregate.

19. A semiconductor device substantially as described herein with reference to Figure 1 or Figure 2 of the accompanying drawings.

20. A method as claimed in Claim 13 or Claim 14 and substantially as described herein.

BROOKES & MARTIN,
High Holborn House,
52/54 High Holborn,
London, WC1V 6SE.
Agents for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1974.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

