WHAT IS CLAIMED IS:

1. A vertical memory device comprising:

gate electrode structures each including gate electrodes spaced apart from one another on a substrate in a first direction substantially perpendicular to an upper surface of the substrate, wherein each of the gate electrodes extends in a second direction substantially parallel to the upper surface of the substrate, and the gate electrode structures are spaced apart from one another in a third direction substantially parallel to the upper surface of the substrate and crossing the second direction;

channels each extending through one of the gate electrode structures in the first direction;

a first division pattern extending in the second direction between first ones of the gate electrode structures neighboring in the third direction;

second and third division patterns alternately disposed in the second direction between second ones of the gate electrode structures neighboring in the third direction; and

a first support layer on the gate electrode structures, wherein the first support layer is at substantially a same height as upper portions of the first and second division patterns and contacting the upper portions of the first and second division patterns,

wherein the upper portions of the first division patterns and the upper portions of the second division patterns are arranged in a zigzag pattern in the second direction in a plan view,

wherein the first division pattern includes a lower portion extending in the second direction, and

wherein a distance of an upper surface of the lower portion of the first division pattern from the substrate is greater than a distance of an upper surface of the third division pattern from the substrate.

2. The vertical memory device of claim 1, wherein each of the upper portions of the first division patterns partially overlaps the upper portions of the second division patterns in the third direction.

3. The vertical memory device of claim 1 or claim 2, wherein the first division pattern is one of a plurality of first division patterns spaced apart from one another in the third direction, and

wherein the second division pattern is disposed between neighboring first division patterns of the plurality of first division patterns neighboring in the third direction.

4. The vertical memory device of claim 3, wherein the second division pattern is one of a plurality of second division patterns spaced apart from one another in the second direction, and

wherein the second division pattern is disposed between the neighboring first division patterns in the third direction.

5. The vertical memory device of any one of claims 1 to 4, wherein the upper portions of the first division pattern are spaced apart from one another in the second direction, and each of the upper portions of the first division pattern contact the upper surface of the lower portion of the first division pattern.

6. The vertical memory device of claim 5, wherein a width in the third direction of each of the upper portions of the first division pattern is greater than that of the lower portion thereof.

7. The vertical memory device of claim 5 or claim 6, further comprising a metal oxide pattern covering a sidewall of each of the upper portions of the first division pattern.

8. The vertical memory device of claim 7, further comprising a blocking pattern covering lower and upper surfaces and a sidewall of each of the gate electrodes,

wherein the blocking pattern includes a material substantially same as that of the metal oxide pattern.

9. The vertical memory device of claim 1, wherein the second division pattern includes lower portions spaced apart from one another in the second direction and connected to the third division patterns, and

wherein the upper portion of the second division pattern commonly contacts upper surfaces of neighboring lower portions of the lower portions neighboring in the second direction.

10. The vertical memory device of claim 9, wherein the third division pattern overlaps the upper portion of the second division pattern in the first direction.

11. The vertical memory device of claim 9 or claim 10, wherein a width in the third direction of the upper portion of the second division pattern is greater than that of the lower portions thereof.

12. The vertical memory device of any one of claims 9 to 11, wherein a distance of upper surfaces of the lower portions of the second division pattern from the substrate is

greater than the distance of the upper surface of the third division pattern from the substrate.

13. The vertical memory device of claim 1, wherein the second division pattern includes lower portions spaced apart from one another in the second direction and connected to the third division patterns, and

wherein the upper portions of the second division pattern contact upper surfaces of the lower portions, respectively.

14. The vertical memory device of claim 1, wherein the second division pattern includes lower portions spaced apart from one another in the second direction and connected to the third division patterns, and

wherein the upper portions of the second division pattern are spaced apart from one another on each of the lower portions, and each contact an upper surface of a corresponding one of the lower portions.

15. A vertical memory device comprising:

gate electrode structures each including gate electrodes spaced apart from one another on a substrate in a first direction substantially perpendicular to an upper surface of the substrate, wherein each of the gate electrodes extends in a second direction substantially parallel to the upper surface of the substrate, and the gate electrode structures are spaced apart from one another in a third direction substantially parallel to the upper surface of the substrate and crossing the second direction;

channels each extending through one of the gate electrode structures in the first direction;

a first division pattern including:

a first lower portion extending in the second direction between first ones of the gate electrode structures neighboring in the third direction to separate the first ones of the gate electrode structures from one another; and

first upper portions spaced apart from one another in the second direction, and contacting an upper surface of the first lower portion;

a second division pattern including:

second lower portions spaced apart from one another in the second direction and disposed between second ones of the gate electrode structures; and

second upper portions contacting upper surfaces of the second lower portions;

third division patterns disposed between the second lower portions of the second division pattern; and

a support layer on the gate electrode structures, and facing sidewalls of a first and second upper portions of the first and second division patterns, respectively,

wherein a distance of the upper surface of the first lower portion of the first division pattern from the substrate is greater than a distance of an upper surface of the third division pattern from the substrate.

16. The vertical memory device of claim 15, wherein the first and second upper portions of the first and second division patterns, respectively, are at substantially the same height.

17. The vertical memory device of claim 15 or claim 16, wherein widths in the third direction of the first and second upper portions of the first and second division patterns, respectively, are greater than widths in the third direction of a first and second lower

portions of the first and second division patterns, respectively.

18. A vertical memory device comprising:

a common source plate (CSP) on a substrate;

a channel connection pattern and a first support layer sequentially stacked on the CSP in a first direction substantially perpendicular to an upper surface of the substrate;

gate electrode structures each including gate electrodes spaced apart from one another on the first support layer in the first direction, wherein each of the gate electrodes extends in a second direction substantially parallel to the upper surface of the substrate, and the gate electrode structures are spaced apart from one another in a third direction substantially parallel to the upper surface of the substrate and crossing the second direction;

channels each extending in the first direction through one of the gate electrode structures, the first support layer, and the channel connection pattern on the CSP, wherein the channels are electrically connected to one another;

a first division pattern extending in the second direction between first ones of the gate electrode structures neighboring in the third direction to separate the first ones of the gate electrode structures from one another;

second and third division patterns alternately disposed in the second direction between second ones of the gate electrode structures neighboring in the third direction to separate the second ones of the gate electrode structures from one another; and

a second support layer on the gate electrode structures, wherein the second support layer is at substantially a same height as upper portions of the first and second division patterns,

wherein the upper portions of the first division pattern and the upper portions of the second division patterns are arranged in a zigzag pattern in the second direction,

wherein the first division pattern includes a lower portion extending in the second direction, and

wherein a distance of an upper surface of the lower portion of the first division pattern from the substrate is greater than a distance of an upper surface of the third division pattern from the substrate.

19. The vertical memory device of claim 18, further comprising a charge storage structure covering an outer sidewall of each of the channels.