

Description

The invention relates to an electric circuit for an A/D converter, having a first and a second pair of inputs and at least three pairs of outputs, each pair of inputs serving to receive two input signals which are substantially complementary to one another, each of at least two pairs of outputs for supplying two substantially complementary output signals, the first pair of outputs being connected to the first pair of inputs and the second pair of outputs being connected to the second pair of inputs, and a first output of the third pair of outputs being connected to a node in the circuit which is not one of the inputs of the first pair of inputs. Such a circuit is known from the published European patent Application no. 227,165 (PHA 1137) and is used, for example, as an interpolation circuit in analog-to-digital (A/D) converters. Important considerations in developing an A/D converter are the conversion speed, the dissipation, which is directly related to the number of components in the A/D converter, and the resolution.

So-called "flash" converters provide the highest conversion speed. In a fully parallel version of such a converter the input voltage is applied to $2^n - 1$ comparators, which each compare this voltage with one of $2^n - 1$ reference values to generate an n-bit digital signal, see for example J. Peterson, "A monolithic video A/D converter", IEEE JSSC, Dec. 1979, pp. 932-937.

The principal disadvantage of this fully parallel version is the large number of components, which is due *inter alia* to the large number of comparators required.

Many proposals have been made to reduce the number of comparators in an A/D converter, see for example United States Patent Specifications 2,70,118 and 4,386,339. Generally these proposals lead to a reduction in conversion speed.

A "folding" system is one of the more promising techniques for reducing the number of components. In a "folding" A/D converter a number of "folding" amplifiers respond to an input voltage and a corresponding number of reference voltages in such a way that each amplifier generates two substantially complementary signals which each have recurring trapezoidal shape as a function of the input voltage level.

European patent Application no. 227,165 describes an improvement to an A/D converter equipped with folding amplifiers and proposes an interpolation system which interpolates between at least two pairs of said complementary signals which vary with a parameter to generate further pairs of complementary signals representing one said parameter.

An input circuit generates at least two pairs of substantially complementary signals. In general these signals are generated in response to an analog input voltage, in such a way that the voltages of at least one of the signal pairs vary in a non-insubstantial manner as a function of the input voltage for each value of the input voltage as this voltage varies over a certain input voltage range.

Interpolation is performed with an interpolation circuit comprising two strings each comprising a specific number of series-connected impedance elements, preferably resistors, arranged between two pairs of inputs. To each pair of inputs an associated pair of complementary input signals is applied. Pairs of nodes between two consecutive impedance elements in the two strings, which are moreover located at similar positions along the strings, constitute outputs from which pairs of complementary interpolated signals can be taken. Moreover, the two pairs of complementary input signals also constitute two pairs of output signals of the interpolations circuit.

Sampling comparators (sample latches), corresponding in number to the number of pairs of output signals, generate a sequence of digital bits by comparing the voltages of each pair of output signals.

Only the "zero crossings" - that is the signs of the voltage differences - are material. For the rest the magnitude of the signal difference is irrelevant. The result of the steps proposed in said European Application is a reduction of the number of components without loss in conversion speed and accuracy.

It is the object of the invention to provide a circuit which enables the number of components to be reduced even further and, in some embodiments, the output impedance of the circuit to be reduced. To this end the electric circuit is characterized in that the second output of the third pair of outputs is connected to a first input of the first pair of inputs. This means that the third pair of output signals is non-complementary.

The invention is based on the recognition of the fact that a smaller number of impedance elements is needed to generate the same number of output-signal pairs. This can be achieved because it is no longer necessary to take these output signals from nodes situated at like positions along the two strings. In some cases it is even found that one string may be wholly dispensed with.

The simplest known circuit is that in which only one pair of signals is derived from the first and the second pair of input signals. This means that such a circuit has three pairs of outputs. To replace such a known circuit the circuit in accordance with the invention is characterized in that the first output of the third pair of outputs is connected to a first input

of the second pair of inputs. The known circuit is an interpolation circuit having three pairs of outputs, a third pair of complementary output signals being available on the third pair of outputs. This third pair of output signals is obtained from the first and the second pair of input signals after interpolation. For this purpose the known circuit requires four impedance elements. The circuit in accordance with the invention which can replace the known circuit in fact needs no impedance elements at all. Moreover, this circuit cannot be referred to as an interpolation circuit, because the third pair of output signals is now derived directly from the two pairs of input signals, instead of via interpolation. Further, the pair of output signals appearing on the third pair of outputs is not complementary. Nevertheless, these signals enable the same information, necessary for deriving a digital signal in the A/D converter, as would have been obtained by means of the known circuit to be obtained from the sample latch connected to the third pair of outputs.

Hereinafter, it will also appear that in many cases pairs of outputs in circuits in accordance with the invention supply pairs of signals which are non-complementary to one another.

The electric circuit comprising a string of at least two series connected impedance elements between the second input of the first pair of inputs and the first input of the second pair of inputs is characterized in that the first output of the third pair of outputs is connected to one end of the impedance element which has its other end connected to the second input of the first pair of inputs. If the string in this circuit comprises exactly two impedance elements and five pairs of outputs are provided, then five pairs of output signals can be generated, by an appropriate coupling of these five pairs of outputs to nodes in the circuit, in such a way that the sample latches connected to said five pairs of outputs are capable of supplying the same information for A/D conversion as if they were connected to the five pairs of outputs of the known interpolation circuit. This can be achieved in that a first output of the fourth pair of outputs is connected to one end of the impedance element which has its other end connected to the first input of the second pair of inputs and in that a first output of the fifth pair of outputs is connected to the first input of the first pair of inputs and the second output of the fifth pair of outputs is connected to the first input of the second pair of inputs.

Some embodiments of the invention will now be described in more detail, by way of example, with reference to the accompanying drawings. In the drawings

Figure 1 shows an electric circuit comprising a known interpolation circuit,

Figure 2 shows a first embodiment, and

Figure 3 shows a second embodiment of the electric circuit in accordance with the invention which can replace the known circuit of Figure 1, Figure 4 shows a number of signal waveforms appearing on various points in the circuits of Figures 1, 2 and 3,

Figure 5 shows another known interpolation circuit,

Figure 6 shows an embodiment which can replace the known interpolation circuit of Figure 5, Figure 7 shows a number of signal waveforms appearing on various points in the circuits of Figures 5 and 6,

Figure 8 shows yet another known interpolation circuit,

Figure 9 shows an embodiment which can replace the known circuit of Figure 8,

Figure 10 shows a number of signals appearing on various points of in the circuits of Figures 8 and 9,

Figure 11 shows still another known interpolation circuit,

Figure 12 shows an embodiment which can replace the known circuit of Figure 11, and

Figure 13 shows a number of signals appearing on various points in the circuits of Figures 11 and 12.

Elements in different Figures bearing the same reference numerals are identical.

Figure 1 shows a known electric circuit comprising an interpolation circuit 1. The interpolation comprises two pairs of inputs 2, 2' and 3, 3'. Two signals V_1 and V_{1c} which are substantially complementary to one another can be applied to the first pair of inputs 2, 2'. Similarly two signals V_3 and V_{3c} which are substantially complementary to each other can be applied to the second pair of inputs 3, 3'. For this purpose two signal sources 4 and 5, each having two outputs 6, 6' and 7, 7' respectively, for supplying two pairs of substantially complementary signals, are connected to said inputs 2, 2' and 3, 3' respectively. An input signal V_{in} is applied to the inputs 8 and 9.

The signal sources 4 and 5 may be arbitrary signal sources, provided that they can each generate two mutually complementary output signals. Examples of such signal sources are a signal source having a differential output or a folding amplifier as described in for example the aforementioned European Patent Application 227,165.

Herein "substantially complementary" is to be understood to mean that at least the variable components of two signals are substantially complementary to one another. As will be described hereinafter with reference to Figure 4, for example the signals V_1 and V_2 are complementary to each other. This means that their waveforms vary in a complementary manner about a DC component V_0 .

which is not necessarily zero.

The known interpolation circuit 1 comprises two strings of impedance elements. One string 10 is arranged between the inputs 2' and 3' and comprises four series connected identical impedance elements, preferably resistors, 11 to 14. The second string 15 is arranged between the inputs 2 and 3 and comprises four series connected impedance elements of the same impedance value, preferably resistors, 16 to 19. The interpolation circuit comprises five pairs of outputs 20, 20'; 21, 21'; 22, 22'; 23, 23' and 24, 24'. The pair 20, 20' is connected to the pair of inputs 2, 2'. The pair 24, 24' is connected to the pair of inputs 3, 3'. The pair of outputs 21, 21' is connected to the nodes between the impedances 16, 17 and 11, 12 respectively. The pair of outputs 22, 22' is connected to the nodes between the impedances 17, 18 and 12, 13 respectively. The pair of outputs 23, 23' is connected to the nodes between the impedances 18, 19 and 13, 14 respectively.

Figure 4 shows the output signals V_1 , V_{1c} , V_5 , V_{5c} of the two signal sources 4 and 5 as a function of the input signal V_{in} . If the signal source 4 is a folding amplifier it has a number of reference signals with which the input signal V_{in} is compared. If the input signal V_{in} changes from a value slightly smaller than V_{r1} to a value slightly larger than V_{r1} the signal V_1 and hence its complementary signal V_{1c} is subject to a change. Around the value of the reference signal V_{r1} the output signal V_1 changes from a value V_H to a value V_L , whilst at the same time the output signal V_{1c} changes from a value V_L to the value V_H . For other reference values in the folding amplifier larger than V_{r1} a similar change occurs. For the next reference value above V_{r1} the value of V_1 changes from V_L to V_H , whilst V_{1c} changes from V_H to V_L etc.

Similarly the folding amplifier 5 has a number of reference signals, of which one signal, V_{r2} is shown in Figure 4. This means that around the value of V_{r2} the signal V_5 changes from V_H to V_L , whilst the signal V_{5c} changes from V_L to V_H . The behaviour of the folding amplifier 5 is identical to the behaviour of the folding amplifier 4, except that the transitions are shifted by a value $V_{r2}-V_{r1}$ along the V_{in} axis.

The interpolated signals V_2 and V_{2c} appear on the outputs 21 and 21'. The interpolated signals V_3 and V_{3c} appear on the outputs 22 and 22' and the interpolated signals V_4 and V_{4c} are available on the outputs 23 and 23'. In Figure 4 these signals are shown in broken lines as a function of the input signal V_{in} .

For converting the analog input signal V_{in} into a digital signal the pairs of complementary signals V_1 , V_{1c} ; V_2 , V_{2c} ; V_3 , V_{3c} ; V_4 , V_{4c} and V_5 , V_{5c} appearing on the pairs of outputs 20, 20'; 21, 21';

22, 22'; 23, 23' and 24, 24' in Figure 1 which are applied to the sample latches. Only one sample latch 26 is shown. The sample latch 26, as well as the sample latches connected to the other pairs of outputs, respond(s) to the crossing of signals applied to the two inputs of the sample latch(es). In fact, the outputs of these sample latches detect the intersections P_1 to P_5 of the complementary signals in Figure 4. For that value of V_{in} for which the intersections P_1 to P_5 occur, the outputs of the sample latches "change over", i.e. the output of a sample comparator goes from "high" to "low" or vice versa.

A further coding of the signals appearing on the outputs of the sample latches may yield a digital signal which is a digital replica of the analog input signal V_{in} .

Figure 2 shows an embodiment of the circuit 31 in accordance with the invention which can replace the known circuit of Figure 1. The circuit 31 again comprises two strings 30 and 35 of impedance elements. The string 30 comprises a series arrangement of two identical impedance elements 32 and 33. The string 35 comprises a series arrangement of two identical impedance elements 34 and 36. Preferably, all the impedance elements are resistors. The circuit 31 now generates only the signals V_3 and V_{3c} and not the signals V_2 , V_{2c} , V_4 and V_{4c} of Figure 4. The signals V_3 and V_{3c} are complementary to one another and appear on the nodes between the impedance elements 34, 36 and 32, 33, respectively. These nodes constitute the outputs 22 and 22'. The pairs of outputs 20, 20' and 24, 24' are thus obtained in the same way as in the known circuit 1 in Figure 1 and are consequently connected to the pairs of inputs 2, 2' and 3, 3' respectively.

The pairs of outputs 21, 21' and 23, 23' are obtained in another way. The output 21 is connected to the input 2. The output 21' is connected to the node between the impedances 32 and 33. The output 23 is connected to the node between the impedances 34 and 36, and the output 23' is connected to the input 3'.

Sample latches (not shown) connected to the pairs of outputs 20, 20'; 22, 22' and 24, 24' again detect the value for V_{in} for which the signals V_1 and V_{1c} ; V_3 and V_{3c} , and V_5 and V_{5c} intersect one another. Thus, the intersections P_1 , P_3 and P_5 are defined, see Figure 4. Since the interpolation circuit 31 does not derive the signals V_2 , V_{2c} , V_4 and V_{4c} the intersections P_2 and P_4 cannot be determined.

Instead of these intersections the sample latches (not shown) connected to the pairs of outputs 21, 21' and 23, 23' determine the intersections P_2' (the intersection of the signals V_3 and V_{5c}). In Figure 4 these intersections are represented as open circles. These intersection coincide with the

same value of the input signal V_{in} as the intersections P_2 and P_4 and may therefore also be used in the subsequent incoding step. From the foregoing it is obvious that each of the pairs of outputs 21, 21' and 23, 23' in Figure 2 supplies a pair of output signals which are not complementary to one another. Nevertheless, A/D conversion is performed correctly.

The circuit of Figure 2 has several advantages over the interpolation circuit shown in Figure 1. The number of tapplings of the interpolation resistors in the circuit of Figure 2 is smaller so that the overall stray capacitance in the circuit, if realized in integrated form, is substantially lower. Moreover, the output impedances of the output 21, 21'; 22, 22' and 23, 23' are substantially lower. This applies in the case of the practical assumption that the impedance values of the elements 32, 33 34 and 36 are equal to each other and are equal to the impedance value of each of the impedances 11 to 14 and 16 to 19.

It is evident from Figure 4 that instead of the intersection P_4' between the signals V_3 and V_{5c} the intersection between the signals V_{3c} and V_5 could have been determined. This would have meant that the output 23 had to be connected to the input 3 and the output 23' to the node point between the impedances 32 and 33.

Figure 3 shows an embodiment 31' of the circuit which bears much resemblance to the circuit of Figure 2 and which can also replace the known interpolation circuit of Figure 1. As in the alternative given above, the outputs 23 and 23' are connected respectively to the input 3 and to the node between the impedances 32 and 33, respectively. Moreover, the outputs 22 and 22' are connected to the inputs 2 and 3' respectively.

The following intersections in Figure 4 are now determined: P_1 , P_2 , P_3 , P_4' and P_5 . The circuit of Figure 3 has a minimal number of tapplings on the impedance elements and moreover the output impedance of the outputs 22, 22' is substantially lower than that of the corresponding outputs in the circuit shown in Figure 2. Moreover, it is to be noted that no tapping is needed from the node between the impedance elements 34 and 36. Thus, in this case the two impedance elements 34 and 36 may be dispensed with. Therefore the string 35 of impedance elements is shown in broken lines. Thus the circuit 31 requires only a minimal number of components to obtain the three intermediate intersections P_2' , P_3' and P_4' .

Figure 5 shows a known interpolation circuit 40 comprising two pairs of inputs 2, 2' and 3, 3', to which pairs of complementary signals V_1 , V_{1c} and V_3 , V_{3c} , respectively can be applied. The known circuit comprises nine pairs of outputs 20, 20'; 24, 24' and 43, 43' to 49, 49'.

The two strings 41 and 42 each comprising 8 series-connected impedance elements having the same impedance values are arranged between the inputs 2', 3' and 2, 3 respectively.

Figure 7 shows the input signals V_1 and V_3 which are applied to the inputs 2 and 3 and which can be taken from the outputs 20 and 24, and the complementary signals V_{1c} and V_{3c} which are applied to the inputs 2' and 3' and which appear on the outputs 20' and 24'. The signal pairs V_2 , V_{2c} to V_8 , V_{8c} are signals which are generated by means of the known interpolation circuit and which appear on the outputs 43, 43' to 49, 49'.

By means of sample latches (not shown) connected to the outputs of the interpolation circuit 40 it is possible to determine the intersections P_1 to P_8 in Figure 7 between the various pairs of complementary signals.

Figure 6 shows a circuit 40' in accordance with the invention which can be replace the known interpolation circuit 40 of Figure 5. By means of sample latches (not shown) connected to the pairs of outputs 20, 20' and 24, 24' it is again possible to detect the intersections P_1 and P_3 of Figure 7. The sample latches (not shown) connected to the pairs of outputs 43, 43' to 49, 49' now detect the intersections P_2' to P_8' indicated as open circles in Figure 7.

The intersections P_2' to P_5' take the place of the intersections P_2 to P_5 and represent the intersections of the signal V_1 with the respective signals V_{3c} , V_{5c} , V_{7c} and V_{9c} . This means that the outputs 43, 44 45 and 47 should be connected to the input 2, that the outputs 43', 44' and 45' should be connected to the respective nodes 50, 51 and 52 and that the output 46' should be connected to the input 3'. For this purpose a string 53 of four series connected identical impedance elements 54 to 57 is arranged between the inputs 2' and 3'.

The intersections P_6' , P_7' and P_8' take the place of the intersections P_6 , P_7 and P_8 and represent the intersections of the signal V_3 with the respective signals V_{3c} , V_{5c} and V_{7c} . This means that the outputs 47, 48 and 49 should be connected to the input 3' and that the outputs 47', 48' and 49' are connected to the respective nodes 50, 51 and 52. Again the pairs of outputs 20, 20' and 24, 24' are connected to the pairs of inputs 2, 2' and 3, 3' respectively.

Again it is obvious that no (second) string 58 of four impedance elements is needed between the inputs 2 and 3. Therefore, this string 58 is indicated in broken lines.

Figure 8 shows the simplest known interpolation circuit 60 comprising two strings 62 and 63 of two series connected identical impedance elements each. A pair of complementary signals V_2 , V_{2c} is supplied to the pair of outputs 61, 61'. The various

signals in the known interpolation circuit of Figure 8 are indicated in Figure 10. From this it is evident that only one pair of complementary signals is derived by interpolation from the two pairs of input signals V_1 , V_{1c} and V_3 , V_{3c} . The intersections P_1 , P_2 and P_3 in Figure 10 can be determined by means of three sample latches (not shown) connected to the three pairs of outputs.

Figure 9 shows the circuit in accordance with the invention, which can replace the known interpolation circuit of Figure 8. The output 61 is now connected to the input 2 and the output 61' is connected to the input 3'. The sample latch (not shown) connected to the pair of outputs 61, 61' thus detects the intersection P_2' between the signals V_1 and V_{3c} . The circuit of Figure 9 with the following sample latches thus enables the intersections P_1 , P_2' and P_3 to be determined.

So far only circuits comprising an odd number of output pairs have been described. However, the invention can also be applied to circuits having an even number of output pairs. Figures 11 and 12 show examples of such circuits.

Figure 11 shows a known interpolation circuit having four pairs of outputs 20, 20'; 71, 71'; 72, 72'; 24, 24'. The known circuit which comprises two strings of three series connected impedance elements each (resistors having equal resistance values R) supplies two pairs of output signals V_2 , V_{2c} and V_3 , V_{3c} , which are derived from the two pairs of input signals V_1 , V_{1c} and V_4 , V_{4c} by interpolation. Figure 13 shows the four pairs of signals appearing in the known circuit. Sample latches (not shown) connected to the pairs of outputs 20, 20'; 71, 71'; 72, 72' and 24, 24' detect the intersections P_1 to P_4 between the respective pairs of output signals V_1 , V_{1c} ; V_2 , V_{2c} ; V_3 , V_{3c} and V_4 , V_{4c} .

Figure 12 shows the circuit 70' in accordance with the invention which can replace the circuit 70. The circuit 70' again comprises two strings of impedance elements. Both strings 73 and 74 each comprise a series arrangement of two impedance elements R , $2R$. The impedance value ($2R$) of one impedance element 75, 76 in each string 73 or 74 is equal to twice the impedance value (R) of the other element 77 or 78 in the respective string 73 or 74. The two impedance elements 75 and 76 may obviously comprise a series arrangement of two impedance elements of the value R . Such a construction is preferred if the circuit 70' is integrated. Sample latches (not shown) connected to the pairs of outputs of the circuit 70' now detect the intersections P_1 , P_2' , P_3 and P_4 . This circuit 70' has the advantage that although its overall impedance value is equal to that of the circuit 70 in Figure 11 the number ofappings on the impedance string can be reduced.

If desired, other intersections in Figures 4, 7, 10 and 13 can be determined than the intersections detected by means of the embodiments described.

Claims

1. An electric circuit (Fig 9; Figs 2, 3, 12) for use in an A/D converter, having a first and a second pair of inputs (2,2'; 3',3) and at least three pairs of outputs (20,20'; 24',24; 61',61), each pair of inputs serving to receive two input signals (V_1 , V_{1c} ; V_{3c} ; V_3) which are substantially complementary to one another, each of at least two pairs of outputs (20,20'; 24',24) serving to supply two output signals which are substantially complementary to one another, the first pair of outputs (20,20') being connected to the first pair of inputs (2,2') and the second pair of outputs (24',24) being connected to the second pair of inputs (3',3), and a first output (61') of the third pair of outputs (61',61) being connected to a node in the circuit which is not one of the inputs of the first pair of inputs, characterized in that the second output (61) of the third pair of outputs is connected to a first input (2) of the first pair of inputs.
2. An electric circuit (Fig 9; 60') as claimed in Claim 1, characterized in that the first output (61') of the third pair of outputs is connected to a first (3') input of the second pair of inputs.
3. An electric circuit (Fig 12; 70') as claimed in Claim 1, comprising at least four pairs of outputs (20,20'; ... 24',24), a string of at least two series-connected impedance elements (75,77) being arranged between the second input (2') of the first pair of inputs and a first input (3') of the second pair of inputs, characterized in that the first output (71') of the third pair of outputs (71',71) is connected to one end of the impedance element (75) which has its other end connected to the second input (2') of the first pair of inputs.
4. An electric circuit (Fig 3; 31') as claimed in Claim 3, comprising at least five pairs of outputs (20,20'; 24',24), a first output (23') of the fourth pair of outputs (23'; 23) being connected to one end of the impedance element (33) which has its other end connected to the first input (3') of the second pair of inputs, characterized in that the second output (23) of the fourth pair of outputs is connected to the second input (3) of the second pair of inputs.



signals in the known interpolation circuit of Figure 8 are indicated in Figure 10. From this it is evident that only one pair of complementary signals is derived by interpolation from the two pairs of input signals V_1 , V_{1c} and V_3 , V_{3c} . The intersections P_1 , P_2 and P_3 in Figure 10 can be determined by means of three sample latches (not shown) connected to the three pairs of outputs.

Figure 9 shows the circuit in accordance with the invention, which can replace the known interpolation circuit of Figure 8. The output 61 is now connected to the input 2 and the output 61' is connected to the input 3'. The sample latch (not shown) connected to the pair of outputs 61, 61' thus detects the intersection P_2' between the signals V_1 and V_{3c} . The circuit of Figure 9 with the following sample latches thus enables the intersections P_1 , P_2' and P_3 to be determined.

So far only circuits comprising an odd number of output pairs have been described. However, the invention can also be applied to circuits having an even number of output pairs. Figures 11 and 12 show examples of such circuits.

Figure 11 shows a known interpolation circuit having four pairs of outputs 20, 20'; 71, 71'; 72, 72'; 24, 24'. The known circuit which comprises two strings of three series connected impedance elements each (resistors having equal resistance values R) supplies two pairs of output signals V_2 , V_{2c} and V_3 , V_{3c} , which are derived from the two pairs of input signals V_1 , V_{1c} and V_4 , V_{4c} by interpolation. Figure 13 shows the four pairs of signals appearing in the known circuit. Sample latches (not shown) connected to the pairs of outputs 20, 20'; 71, 71'; 72, 72' and 24, 24' detect the intersections P_1 to P_4 between the respective pairs of output signals V_1 , V_{1c} ; V_2 , V_{2c} ; V_3 , V_{3c} and V_4 , V_{4c} .

Figure 12 shows the circuit 70' in accordance with the invention which can replace the circuit 70. The circuit 70' again comprises two strings of impedance elements. Both strings 73 and 74 each comprise a series arrangement of two impedance elements R , $2R$. The impedance value ($2R$) of one impedance element 75, 76 in each string 73 or 74 is equal to twice the impedance value (R) of the other element 77 or 78 in the respective string 73 or 74. The two impedance elements 75 and 76 may obviously comprise a series arrangement of two impedance elements of the value R . Such a construction is preferred if the circuit 70' is integrated. Sample latches (not shown) connected to the pairs of outputs of the circuit 70' now detect the intersections P_1 , P_2' , P_3 and P_4 . This circuit 70' has the advantage that although its overall impedance value is equal to that of the circuit 70 in Figure 11 the number of tapplings on the impedance string can be reduced.

If desired, other intersections in Figures 4, 7, 10 and 13 can be determined than the intersections detected by means of the embodiments described.

5 Claims

1. An electric circuit (Fig 9; Figs 2, 3, 12) for use in an A/D converter, having a first and a second pair of inputs (2,2'; 3',3) and at least three pairs of outputs (20,20'; 24',24; 61',61), each pair of inputs serving to receive two input signals (V_1 , V_{1c} ; V_{3c} , V_3) which are substantially complementary to one another, each of at least two pairs of outputs (20,20'; 24',24) serving to supply two output signals which are substantially complementary to one another, the first pair of outputs (20,20') being connected to the first pair of inputs (2,2') and the second pair of outputs (24',24) being connected to the second pair of inputs (3',3), and a first output (61') of the third pair of outputs (61',61) being connected to a node in the circuit which is not one of the inputs of the first pair of inputs, characterized in that the second output (61) of the third pair of outputs is connected to a first input (2) of the first pair of inputs.
2. An electric circuit (Fig 9; 60') as claimed in Claim 1, characterized in that the first output (61') of the third pair of outputs is connected to a first (3') input of the second pair of inputs.
3. An electric circuit (Fig 12; 70') as claimed in Claim 1, comprising at least four pairs of outputs (20,20'; ... 24',24), a string of at least two series-connected impedance elements (75,77) being arranged between the second input (2') of the first pair of inputs and a first input (3') of the second pair of inputs, characterized in that the first output (71') of the third pair of outputs (71',71) is connected to one end of the impedance element (75) which has its other end connected to the second input (2') of the first pair of inputs.
4. An electric circuit (Fig 3; 31') as claimed in Claim 3, comprising at least five pairs of outputs (20,20'; ... 24',24), a first output (23') of the fourth pair of outputs (23', 23) being connected to one end of the impedance element (33) which has its other end connected to the first input (3') of the second pair of inputs, characterized in that the second output (23) of the fourth pair of outputs is connected to the second input (3) of the second pair of inputs.



5. An electric circuit (Fig 3; 31') as claimed in Claim 4, comprising five pairs of outputs, characterized in that the string of impedance elements arranged between the second input (2') of the first pair of inputs and the first input (3') of the second pair of inputs comprises two impedance elements (32,33).

6. An electric circuit (Fig 3; 31') as claimed in Claim 4 or 5, characterized in that the first output (22) of the fifth pair of outputs (22,22') is connected to a first input (2) of the first pair of inputs and the second output (22') of the fifth pair of outputs is connected to the first input (3') of the second pair of inputs.

7. An electric circuit as claimed in Claim 4 or 5, characterized in that a first output of the fifth pair of outputs is connected to the second input of the first pair of inputs and the second output of the fifth pair of outputs is connected to the second input of the second pair of inputs.

8. An electric circuit (Fig 2; 31) as claimed in Claim 3, a first string (32,33) of two series connected impedance elements being arranged between the second input (2') of the first pair of inputs and the first input (3') of the second pair of inputs and a second string (34,36) of two series connected impedance elements being arranged between the first input (2) of the first pair of inputs and the second input (3) of the second pair of inputs, characterized in that the circuit comprises five pairs of outputs, in that a first output (23') of the fourth pair of outputs (23',23) is connected to one of the two inputs (3) of the second pair of inputs, the second output (23) of the fourth pair of outputs is connected to one end of the impedance element (36) which has its other end connected to the other input (3) than the said one input (3') of the second pair of inputs.

9. An electric circuit (Fig 2; 31) as claimed in Claim 8, characterized in that the nodes between the two impedance elements in the two strings constitute the fifth pair of outputs (22,22').

10. An electric circuit (Figs 2, 3, 12) as claimed in any one of the Claims 3 to 9, characterized in that all the impedance elements have the same impedance value.

11. An electric circuit (Figs 2,3) as claimed in any one of the preceding Claims, characterized in that it comprises a first (4) and a second (5)

signal source, each having a first (6,7') and a second (6',7) output for supplying a pair of complementary signals (V_1, V_{1c} ; V_{5c}, V_5) and in that the first and the second output of the first and second signal source are connected to the first (2,3') and second (2',3) input of the first (2,2') and the second (3',3) pair of inputs respectively.

12. An electric circuit (Figs 2,3) as claimed in Claim 11, characterized in that the signal sources (4,5) are folding amplifiers.

13. An electric circuit (Fig 12; 70') as claimed in Claim 3, comprising four pairs of outputs (20,20'; 24',24), characterized in that a first string (75,77) of two impedance elements is arranged between the second input (2') of the first pair of inputs (2,2') and the first input (3') of the second pair (3',3) of inputs and a second string (76,78) of two impedance elements is arranged between the first input (2) of the first pair of inputs and the second input (3) of the second pair of inputs, in that the nodes between the two impedance elements in the two strings constitute the fourth pair of outputs (72',72), and in that the impedance elements (75,76) arranged between the first pair of inputs (2,2') and the fourth pair of outputs (72',72) have an impedance value ($2R$) which is twice the impedance value (R) of the impedance elements (77,78) arranged between the second pair of inputs (3',3) and the fourth pair of outputs.

Patentansprüche

1. Elektrische Schaltung (Fig. 9; Fig. 2, 3, 12) zur Verwendung in einem Analog/Digital-Wandler mit einem ersten und einem zweiten Eingängepaar (2,2'; 3',3) und wenigstens drei Ausgängepaaren (20,20'; 24',24; 61',61), wobei jedes Eingängepaar zum Empfangen von zwei Eingangssignalen (V_1, V_{1c} ; V_{3c}, V_3) dient, die im wesentlichen einander komplementär sind, jedes Paar von wenigstens zwei Ausgängepaaren (20,20'; 24',24) zum Liefern von zwei Ausgangssignalen dient, die im wesentlichen einander komplementär sind, das erste Ausgängepaar (20,20') mit dem ersten Eingängepaar (2,2') und das zweite Ausgängepaar (24',24) mit dem zweiten Eingängepaar (3',3) verbunden sind, und ein erster Ausgang (61') des dritten Ausgängepaars (61',61) mit einem Knotenpunkt in der Schaltung verbunden ist, der nicht einer der Eingänge des ersten Eingängepaars ist, dadurch gekennzeichnet, daß der zweite Ausgang (61) des dritten Ausgänge-



paars mit einem ersten Eingang (2) des ersten Eingängepaars verbunden ist.

Elektrische Schaltung (Fig. 9; 60') nach Anspruch 1, dadurch gekennzeichnet, daß der erste Ausgang (61') des dritten Ausgängepaars mit einem ersten Eingang (3') des zweiten Eingängepaars verbunden ist.

3. Elektrische Schaltung (Fig. 12; 70') nach Anspruch 1, mit wenigstens vier Ausgängepaaren (20,20'; ... 24',24'), wobei eine Reihe von wenigstens zwei reihengeschalteten Impedanzelementen (75,77) zwischen dem zweiten Eingang (2') des ersten Eingängepaars und einem ersten Eingang (3') des zweiten Eingängepaars angeordnet ist, dadurch gekennzeichnet, daß der erste Ausgang (71') des dritten Ausgängepaars (71',71) mit einem Ende des Impedanzelements (75) verbunden ist, das mit seinem anderen Ende mit dem zweiten Eingang (2') des ersten Eingängepaars verbunden ist.

4. Elektrische Schaltung (Fig. 3; 31') nach Anspruch 3, mit wenigstens fünf Ausgängepaaren (20,20'; ... 24',24'), wobei ein erster Ausgang (23') des vierten Ausgängepaars (23',23) mit einem Ende des Impedanzelements (33) verbunden ist, das mit seinem anderen Ende an den ersten Eingang (3') des zweiten Eingängepaars angeschlossen ist, dadurch gekennzeichnet, daß der zweite Ausgang (23) des vierten Ausgängepaars mit dem zweiten Eingang (3) des zweiten Eingängepaars verbunden ist.

5. Elektrische Schaltung (Fig. 3; 31') nach Anspruch 4, mit fünf Ausgängepaaren, dadurch gekennzeichnet, daß die zwischen dem zweiten Eingang (2') des ersten Eingängepaars und dem ersten Eingang (3') des zweiten Eingängepaars angeordnete Kette von Impedanzelementen zwei Impedanzelemente (32,33) enthält.

6. Elektrische Schaltung (Fig. 3; 31') nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß der erste Ausgang (22) des fünften Ausgängepaars (22,22') mit einem ersten Eingang (2) des ersten Eingängepaars und der zweite Ausgang (22') des fünften Ausgängepaars mit dem ersten Eingang (3') des zweiten Eingängepaars verbunden sind.

7. Elektrische Schaltung nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß ein erster Ausgang des fünften Ausgängepaars mit dem zweiten Eingang des ersten Eingängepaars verbunden ist und daß der Zweite Ausgang

des fünften Ausgängepaars mit dem zweiten Eingang des zweiten Eingängepaars verbunden ist.

8. Elektrische Schaltung (Fig. 2; 31) nach Anspruch 3, wobei eine erste Kette (32,33) von zwei reihengeschalteten Impedanzelementen zwischen dem zweiten Eingang (2') des ersten Eingängepaars und dem ersten Eingang (3') des Zweiten Eingängepaars angeordnet ist, und eine zweite Kette (34,36) von zwei reihengeschalteten Impedanzelementen zwischen dem ersten Eingang (2) des ersten Eingängepaars und dem zweiten Eingang (3) des zweiten Eingängepaars angeordnet ist, dadurch gekennzeichnet, daß die Schaltung fünf Ausgängepaare enthält, daß ein erster Ausgang (23') des vierten Ausgängepaars (23',23) mit einem der zwei Eingänge (3) des zweiten Eingängepaars verbunden ist, der zweite Ausgang (23) des vierten Ausgängepaars mit einem Ende des Impedanzelements (36) verbunden ist, das mit seinem anderen Ende an den anderen Eingang (3) als der genannte eine Eingang (3') des zweiten Eingängepaars angeschlossen ist.

9. Elektrische Schaltung (Fig. 2; 31) nach Anspruch 8, dadurch gekennzeichnet, daß die Knotenpunkte zwischen den zwei Impedanzelementen in den zwei Ketten das fünfte Ausgängepaar (22,22') bilden.

10. Elektrische Schaltung (Fig. 2, 3, 12) nach einem der Ansprüche 3 bis 9, dadurch gekennzeichnet, daß alle Impedanzelemente den gleichen Impedanzwert besitzen.

11. Elektrische Schaltung (Fig. 2, 3) nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß sie eine erste (4) und eine zweite (5) Signalquelle enthält, die je einen ersten (6,7') und einen zweiten (6',7) Ausgang zum Ausgeben eines komplementären Signalaars (V_1 , V_{1C} ; V_{5C} , V_5) besitzt, und daß der erste und der zweite Ausgang der ersten und zweiten Signalquelle mit dem ersten (2,3') und dem zweiten (2',3) Eingang des ersten (2,2') und des zweiten (3',3) Eingängepaars verbunden sind.

12. Elektrische Schaltung (Fig. 2, 3) nach Anspruch 11, dadurch gekennzeichnet, daß die Signalquellen (4,5) Faltungsverstärker sind.

13. Elektrische Schaltung (Fig. 12; 70') nach Anspruch 3, mit vier Ausgängepaaren (20,20'; ... 24',24'), dadurch gekennzeichnet, daß eine er-



ste Kette (75,77) von zwei Impedanzelementen zwischen dem zweiten Eingang (2') des ersten Eingängepaars (2,2') und dem ersten Eingang (3') des zweiten Eingängepaars (3',3) und eine Zweite Kette (76,78) von zwei Impedanzelementen zwischen dem ersten Eingang (2) des ersten Eingängepaars und dem zweiten Eingang (3) des zweiten Eingängepaars angeordnet sind, daß die Knotenpunkte zwischen den zwei Impedanzelementen in den zwei Ketten das vierte Ausgänpaar (72',72) bilden, und daß die Impedanzelemente (75,76) zwischen dem ersten Eingängepaar (2,2') und dem vierten Ausgänpaar (72',72) einen Impedanzwert (2R) besitzen, der das Doppelte des Impedanzwerts (R) der Impedanzelemente (77,78) zwischen dem zweiten Eingängepaar (3',3) und dem vierten Ausgänpaar ist.

Revendications

1. Circuit électrique (Fig. 9; Fig. 2, 3, 12) à utiliser dans un convertisseur A/N, comportant une première et une seconde paires d'entrées (2,2'; 3', 3) et au moins trois paires de sorties (20, 20'; 24', 24; 61', 61), chaque paire d'entrées servant à recevoir deux signaux d'entrée (V_1 , V_{1c} ; V_{3c} , V_3), qui sont en substance complémentaires l'un de l'autre, chacune d'au moins deux paires de sorties (20,20'; 24', 24) servant à fournir deux signaux de sortie qui sont en substance mutuellement complémentaires, la première paire de sorties (20, 20') étant connectée à la première paire d'entrées (2, 2') et la seconde paire de sorties (24', 24), à la seconde paire d'entrées (3', 3), et une première sortie (61') de la troisième paire de sorties (61', 61) étant connectée à un noeud dans le circuit qui n'est pas une des entrées de la première paire d'entrées, caractérisé en ce que la seconde sortie (61) de la troisième paire de sorties est connectée à une première entrée (2) de la première paire d'entrées.

2. Circuit électrique (Fig. 9; 60') suivant la revendication 1, caractérisé en ce que la première sortie (61') de la troisième paire de sorties est connectée à une première entrée (3') de la seconde paire d'entrées.

3. Circuit électrique (Fig. 12; 70') suivant la revendication 1, comprenant au moins quatre paires de sorties (20, 20'; ... ; 24', 24), une chaîne d'au moins deux éléments d'impédance connectés en série (75, 77) étant disposée entre la seconde entrée (2') de la première paire d'entrées et une première entrée (3') de la seconde paire d'entrées, caractérisé en ce

que la première sortie (71') de la troisième paire de sorties (71', 71) est connectée à une extrémité de l'élément d'impédance (75), dont l'autre extrémité est connectée à la seconde entrée (2') de la première paire d'entrées.

4. Circuit électrique (Fig. 3; 31') suivant la revendication 3, comprenant au moins cinq paires de sorties (20,20'; ...; 24', 24), une première sortie (23') de la quatrième paire de sorties (23', 23) étant connectée à une extrémité de l'élément d'impédance (33), dont l'autre extrémité est connectée à la première entrée (3') de la seconde paire d'entrées, caractérisé en ce que la seconde sortie (23) de la quatrième paire de sorties est connectée à la seconde entrée (3) de la seconde paire d'entrées.

5. Circuit électrique (Fig. 3; 31') suivant la revendication 4, comprenant cinq paires de sorties, caractérisé en ce que la chaîne d'éléments d'impédance disposée entre la seconde entrée (2') de la première paire d'entrées et la première entrée (3') de la seconde paire d'entrées comprend deux éléments d'impédance (32,33).

6. Circuit électrique (Fig. 3; 31') suivant la revendication 4 ou 5, caractérisé en ce que la première sortie (22) de la cinquième paire de sorties (22,22') est connectée à une première entrée (2) de la première paire d'entrées et la seconde sortie (22') de la cinquième paire de sorties est connectée à la première entrée (3') de la seconde paire d'entrées.

7. Circuit électrique suivant la revendication 4 ou 5, caractérisé en ce qu'une première sortie de la cinquième paire de sorties est connectée à la seconde entrée de la première paire d'entrées et la seconde sortie de la cinquième paire de sorties est connectée à la seconde entrée de la seconde paire d'entrées.

8. Circuit électrique (Fig. 2; 31) suivant la revendication 3, dans lequel une première chaîne (32,33) de deux éléments d'impédance connectés en série est disposée entre la seconde entrée (2') de la première paire d'entrées et la première entrée (3') de la seconde paire d'entrées et une seconde chaîne (34,36) de deux éléments d'impédance connectés en série est disposée entre la première entrée (2) de la première paire d'entrées et la seconde entrée (3) de la seconde paire d'entrées, caractérisé en ce que le circuit comprend cinq paires de sorties, qu'une première sortie (23') de la quatrième paire de sorties (23', 23) est connectée à une des deux entrées (3) de la



seconde paire d'entrées, la seconde sortie (23) de la quatrième paire de sorties est connectée à une extrémité de l'élément d'impédance (36), dont l'autre extrémité est connectée à l'autre entrée (3) que ladite première entrée (3') de la seconde paire d'entrées.

trées (3', 3) et la quatrième paire de sorties.

9. Circuit électrique (Fig. 2; 31) suivant la revendication 8, caractérisé en ce que les noeuds entre les deux éléments d'impédance dans les deux chaînes constituent la cinquième paire de sorties (22,22'). 10
10. Circuit électrique (Fig. 2, 3, 12) suivant l'une quelconque des revendications 3 à 9, caractérisé en ce que tous les éléments d'impédance ont la même valeur d'impédance. 15
11. Circuit électrique (Fig. 2,31) suivant l'une quelconque des revendications précédentes, caractérisé en ce qu'il comprend une première (4) et une seconde (5) source de signaux comportant chacune une première (6,7') et une seconde (6', 7) sortie pour fournir une paire de signaux complémentaires (V_1 , V_{1c} ; V_{5c} , V_5) et que la première et la seconde sortie de la première et de la seconde source de signaux sont connectées respectivement à la première (2, 3') et à la seconde (2', 3) entrée de la première (2, 2') et de la seconde (3', 3) paire d'entrées. 20 25 30
12. Circuit électrique (Fig. 2, 3) suivant la revendication 11, caractérisé en ce que les sources de signaux (4, 5) sont des amplificateurs à repliement. 35
13. Circuit électrique (Fig. 12; 70') suivant la revendication 3, comprenant quatre paires de sorties (20, 20'; ...; 24', 24), caractérisé en ce qu'une première chaîne (75, 77) de deux éléments d'impédance est disposée entre la seconde entrée (2') de la première paire d'entrées (2, 2') et la première entrée (3') de la seconde paire d'entrées (3', 3) et une seconde chaîne (76, 78) de deux éléments d'impédance est disposée entre la première entrée (2) de la première paire d'entrées et la seconde entrée (3) de la seconde paire d'entrées, que les noeuds entre les deux éléments d'impédance dans les deux chaînes constituent la quatrième paire de sorties (72', 72) et que les éléments d'impédance (75, 76) disposés entre la première paire d'entrées (2, 2') et la quatrième paire de sorties (72', 72) ont une valeur d'impédance (2R) qui vaut le double de la valeur d'impédance (R) des éléments d'impédance (77, 78) disposés entre la seconde paire d'en- 40 45 50 55