CLAIMS

1. A method for fabricating a FET on a silicon-on-insulator substrate, including:
   (a) forming an isolated silicon island;
   (b) forming a gate structure overlying the isolated silicon island to define a central conduction channel having a center length L and a threshold voltage Vt_C, the gate structure having central and edge regions each with an associated work function Φ_{MF}, wherein at least one edge transistor is defined by a corresponding edge region of the gate structure overlying the isolated silicon island, each edge transistor having a threshold voltage Vt_E determined in part by the work function Φ_{MF} of the corresponding edge region of the gate structure;
   (c) forming source and drain regions within the isolated silicon island and defined by the gate structure; and
   (d) increasing the work function Φ_{MF} of at least one corresponding edge region of the gate structure sufficiently to increase the Vt_E of such corresponding edge transistor to be approximately equal to or greater than Vt_C.

2. The method of claim 1, wherein the FET is an NMOSFET.

3. The method of claim 2, wherein increasing the work function Φ_{MF} of the corresponding edge regions of the gate structure includes implanting a P dopant within a P implant region within such edge regions.

4. The method of claim 3, wherein the P implant region has a length L_P less than or equal to length L.

5. The method of claim 3, wherein the P implant region within such edge regions is triangular shaped.

6. The method of claim 1, wherein the gate structure includes an N+ polysilicon layer and increasing the work function Φ_{MF} of the corresponding edge regions of the gate structure includes implanting a P dopant within the N+ polysilicon layer of such edge regions.

7. The method of claim 1, further including flaring at least one edge region of the gate structure to a length L^+ greater than length L to increase the Vt_E of the corresponding edge transistor compared to Vt_C.

8. The method of claim 1, wherein the increase in the work function Φ_{MF} and Vt_E is at least about 0.3 V.

9. The method of claim 1, further including forming a body tie to one of the source region, the gate structure, or an external node.

10. The method of claim 1, wherein increasing the work function Φ_{MF} of the corresponding edge regions of the gate structure includes forming a metal or metal-like region within the edge regions of the gate structure such that the work function Φ_{MF} differs between the central and edge regions of the gate structure.

11. The method of claim 1, wherein increasing the work function Φ_{MF} of the corresponding edge portions of the gate structure includes forming the central region of the gate structure with a first metal or metal-like material, and forming the edge regions of the gate structure with a second metal or metal-like material, such that the work function Φ_{MF} differs between the central and edge regions of the gate structure.

12. The method of claim 1, wherein the gate structure is formed of polysilicon, and increasing the work function Φ_{MF} of the corresponding edge portions of the gate structure includes doping the edge regions of the gate structure to form degeneratively-doped polysilicon, such that the work function Φ_{MF} differs between the central and edge regions of the gate structure.

13. The method of claim 1, wherein increasing the work function Φ_{MF} of the corresponding edge portions of the gate structure includes doping an insulator beneath the gate structure, such that the work function Φ_{MF} differs between the central and edge regions of the gate structure.

14. The method of claim 1, wherein increasing the work function Φ_{MF} of the corresponding edge portions of the gate structure includes forming the central region of the gate structure

from a material having a first dopant, and modifying the edge regions of the gate structure with a second dopant, such that the work function Φ_{MF} differs between the central and edge regions of the gate structure.