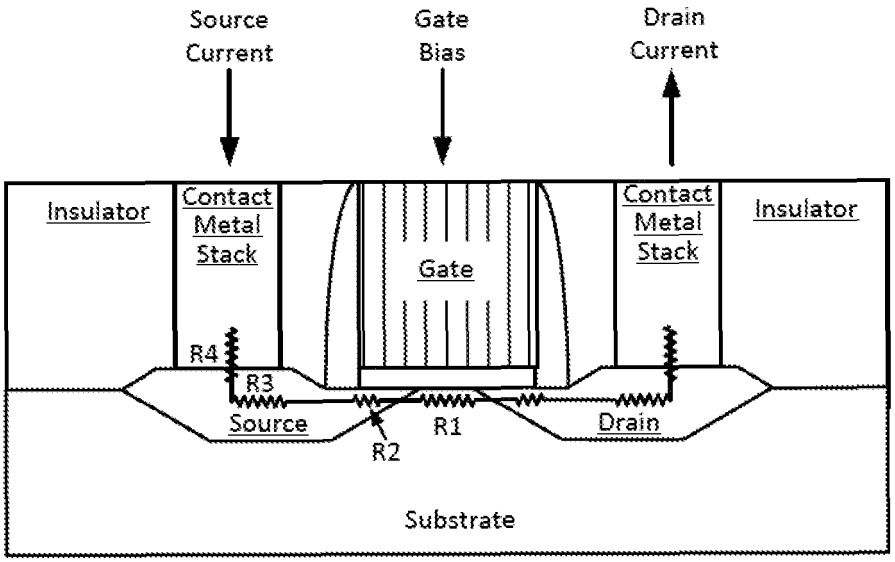

Source Current
Gate Bias
Drain Current
Insulator
Contact Metal Stack
Gate
Contact Metal Stack
Insulator
R4
R3
Source
R2
R1
Drain
Substrate

FIG. 1

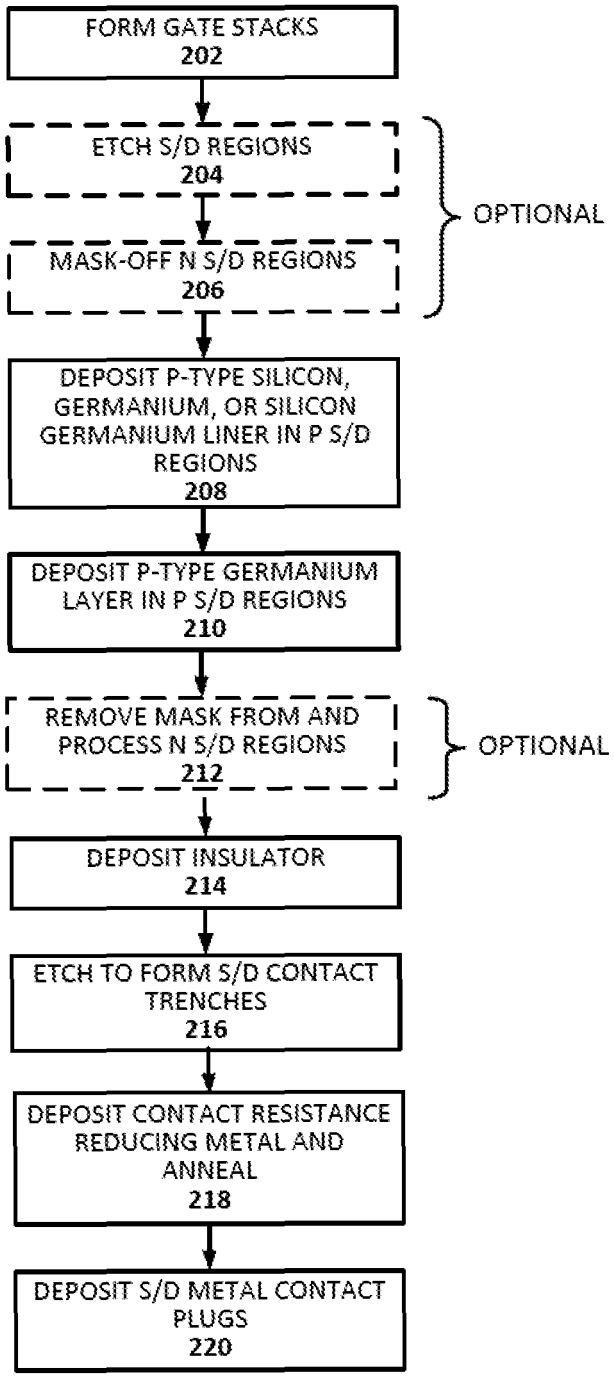

FORM GATE STACKS
202
ETCH S/D REGIONS
204
MASK-OFF N S/D REGIONS
206
OPTIONAL
DEPOSIT P-TYPE SILICON, GERMANIUM, OR SILICON GERMANIUM LINER IN P S/D REGIONS
208
DEPOSIT P-TYPE GERMANIUM LAYER IN P S/D REGIONS
210
REMOVE MASK FROM AND PROCESS N S/D REGIONS
212
OPTIONAL
DEPOSIT INSULATOR
214
ETCH TO FORM S/D CONTACT TRENCHES
216
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
218
DEPOSIT S/D METAL CONTACT PLUGS
220

FIG. 2

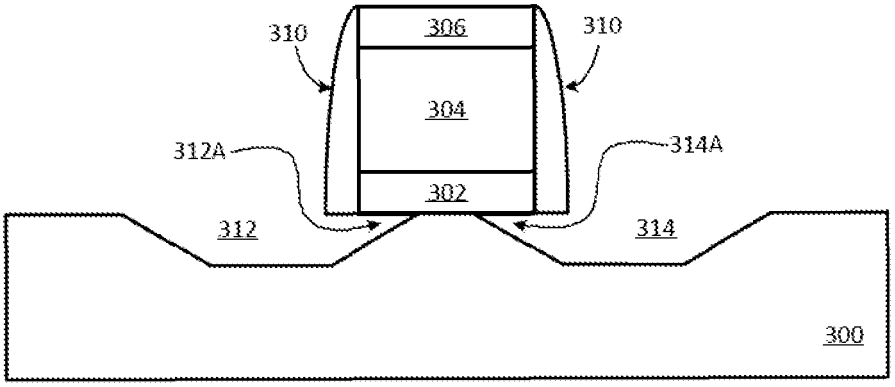


FIG. 3A

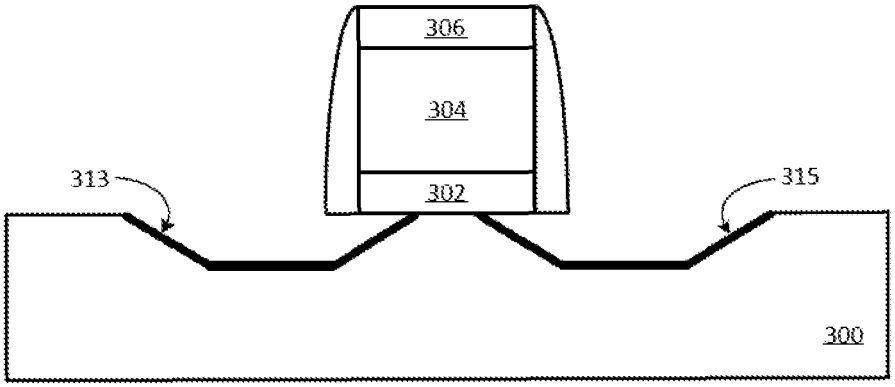


FIG. 3B

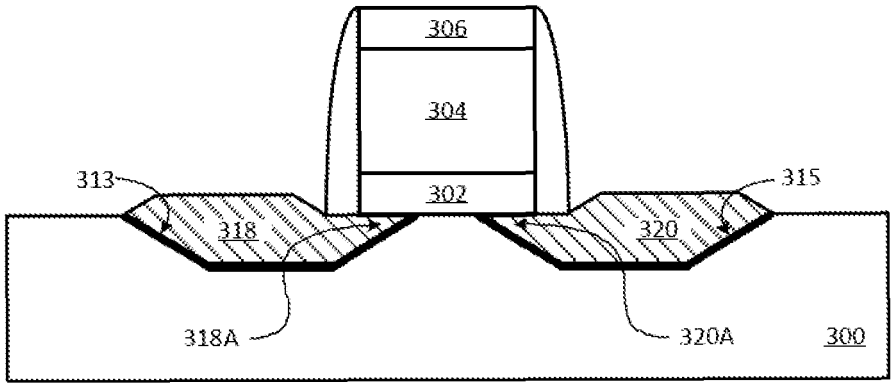


FIG. 3C

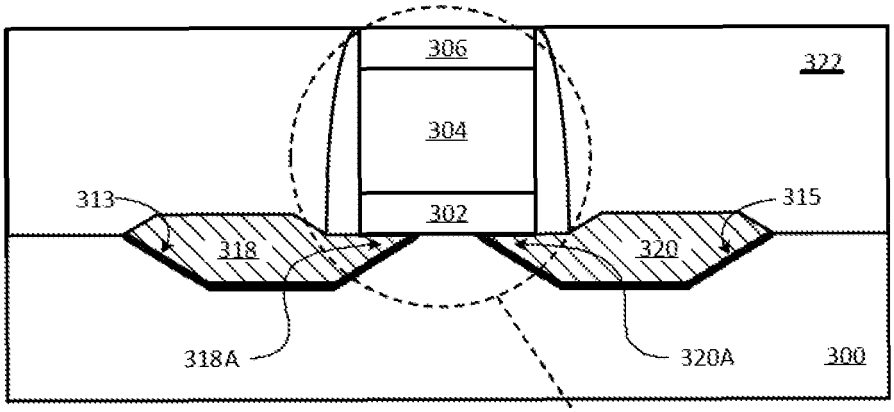


FIG. 3D

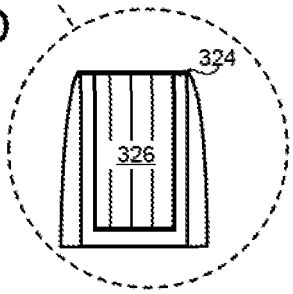


FIG. 3D'

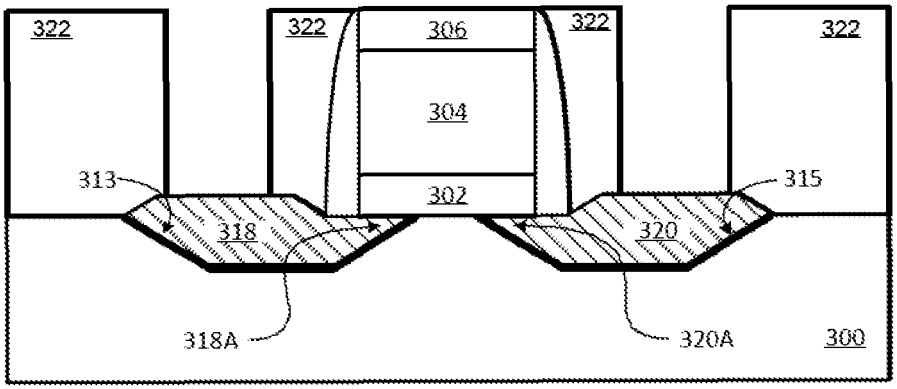


FIG. 3E

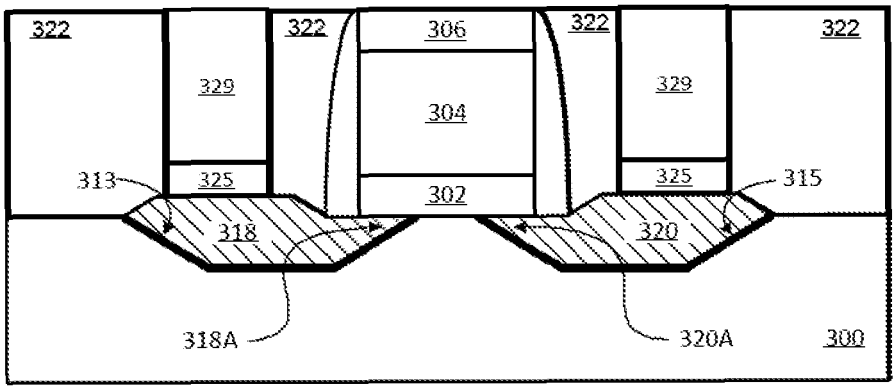


FIG. 3F

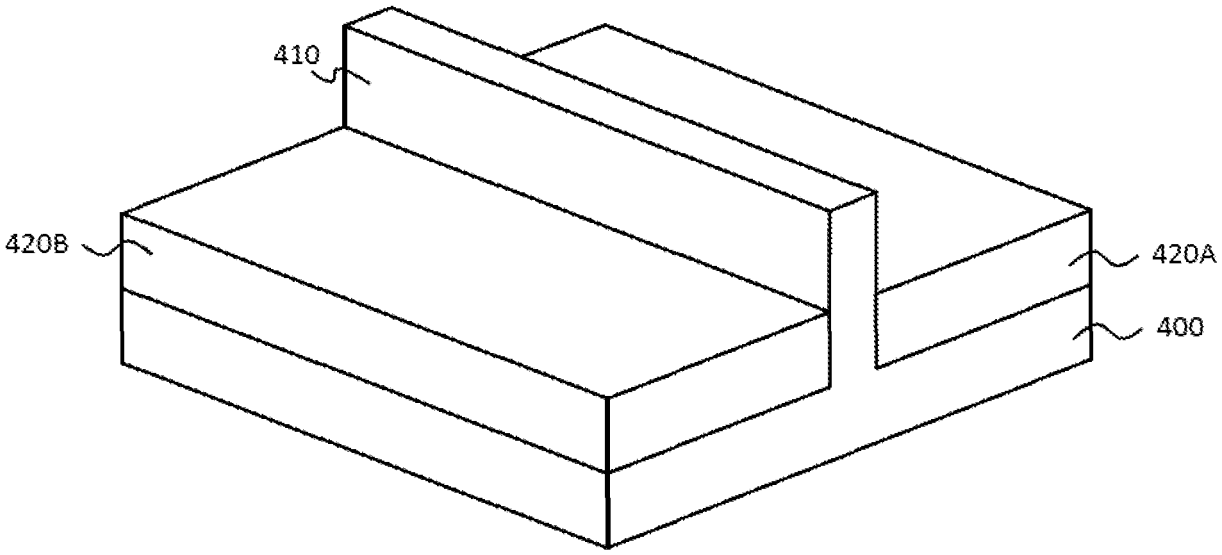


FIG. 4A

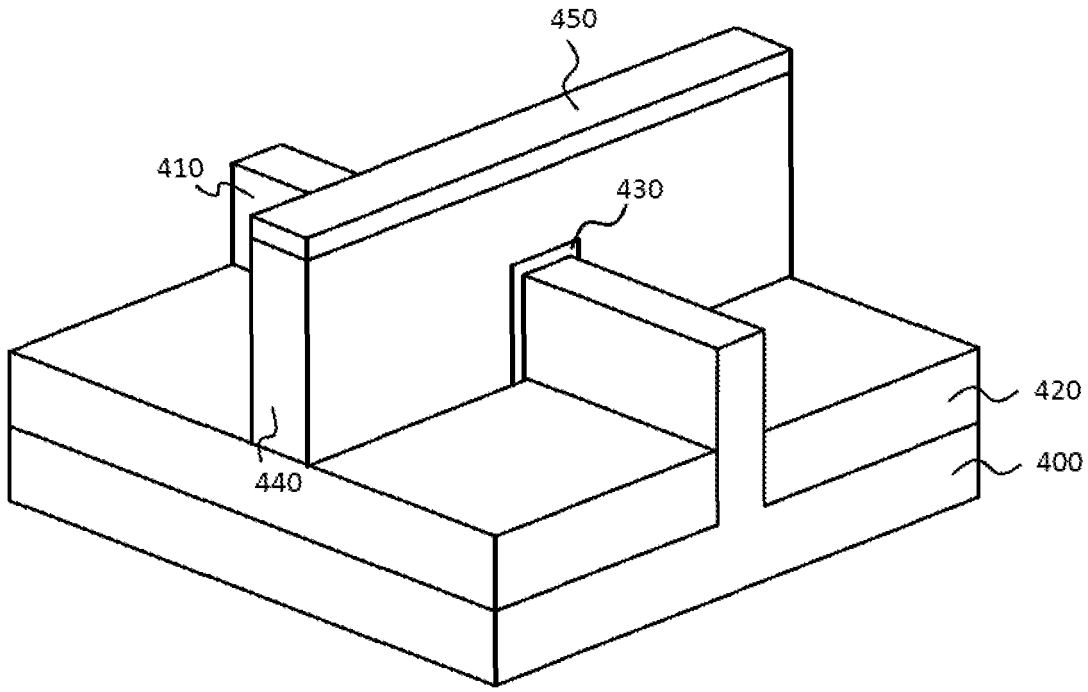


FIG. 4B

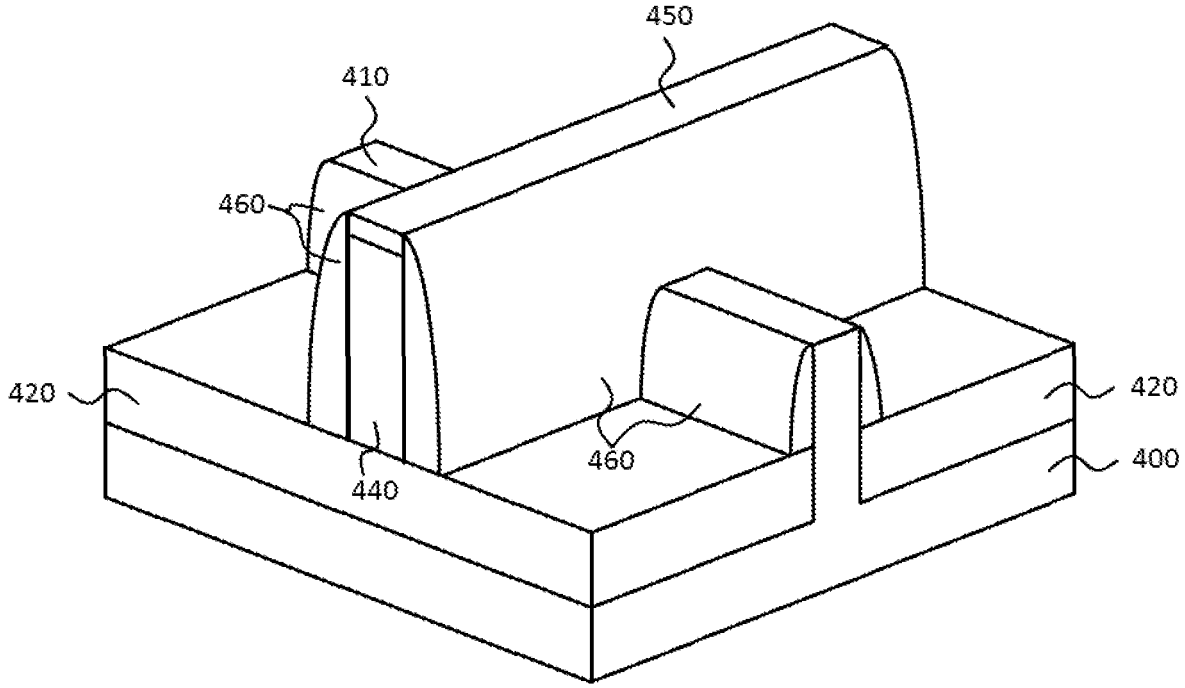


FIG. 4C

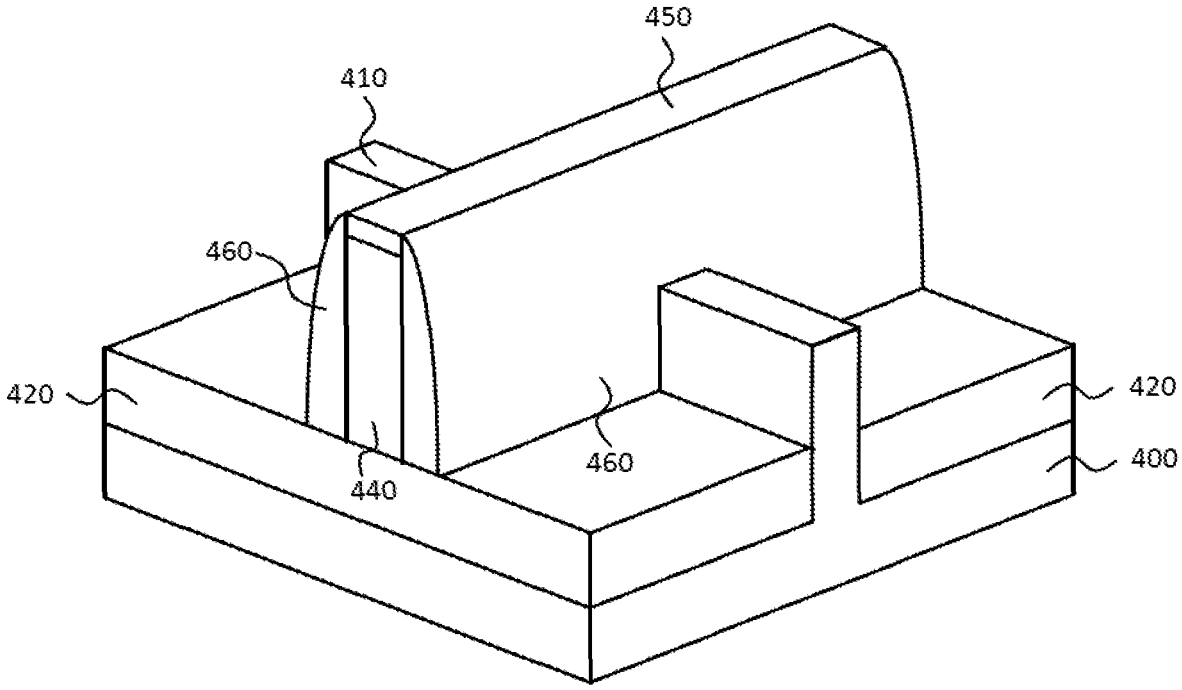


FIG. 4D

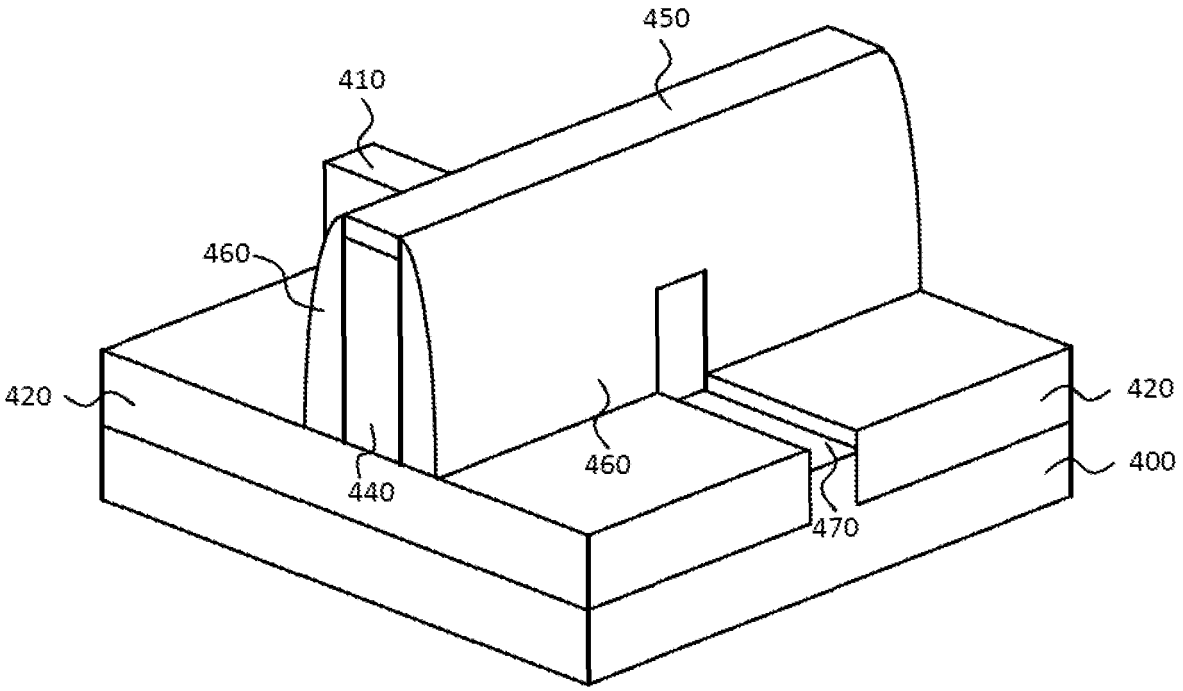

450
410
460
420
460
420
400
440
470

FIG. 4E

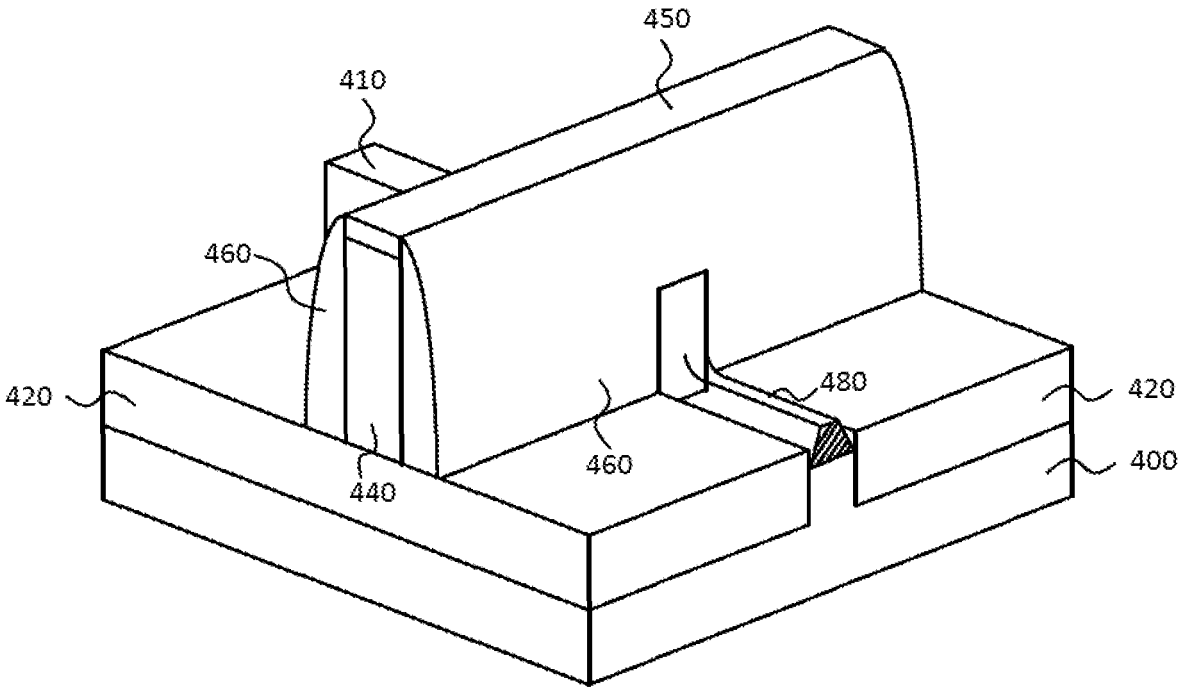

450
410
460
420
480
420
400
460
440

FIG. 4F

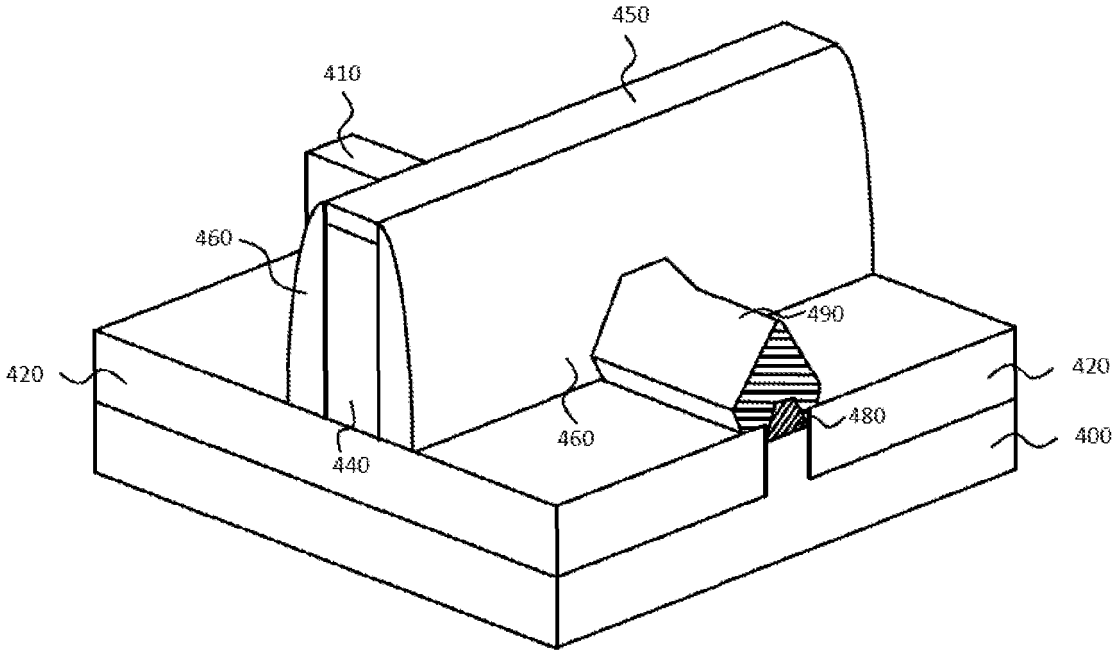


FIG. 4G

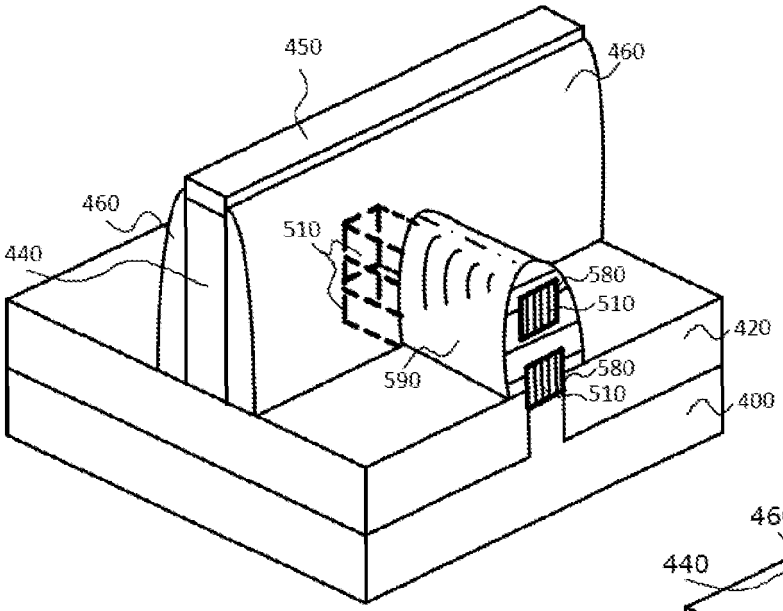
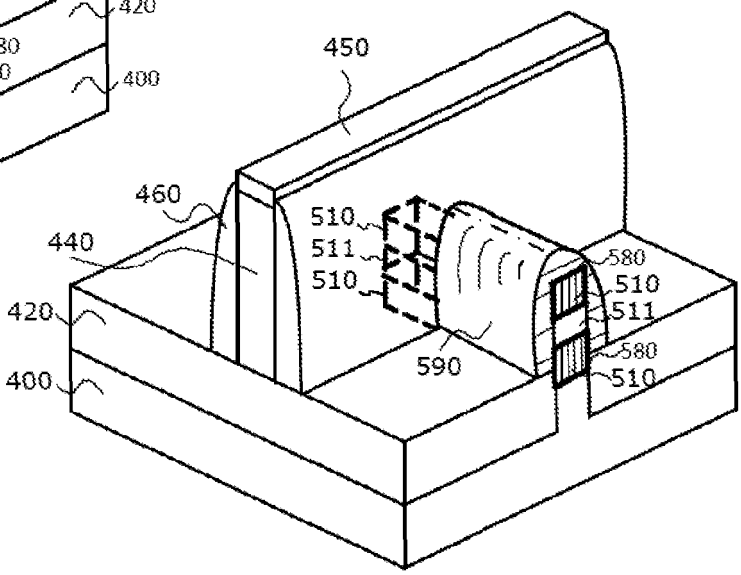


FIG. 5A

FIG. 5B



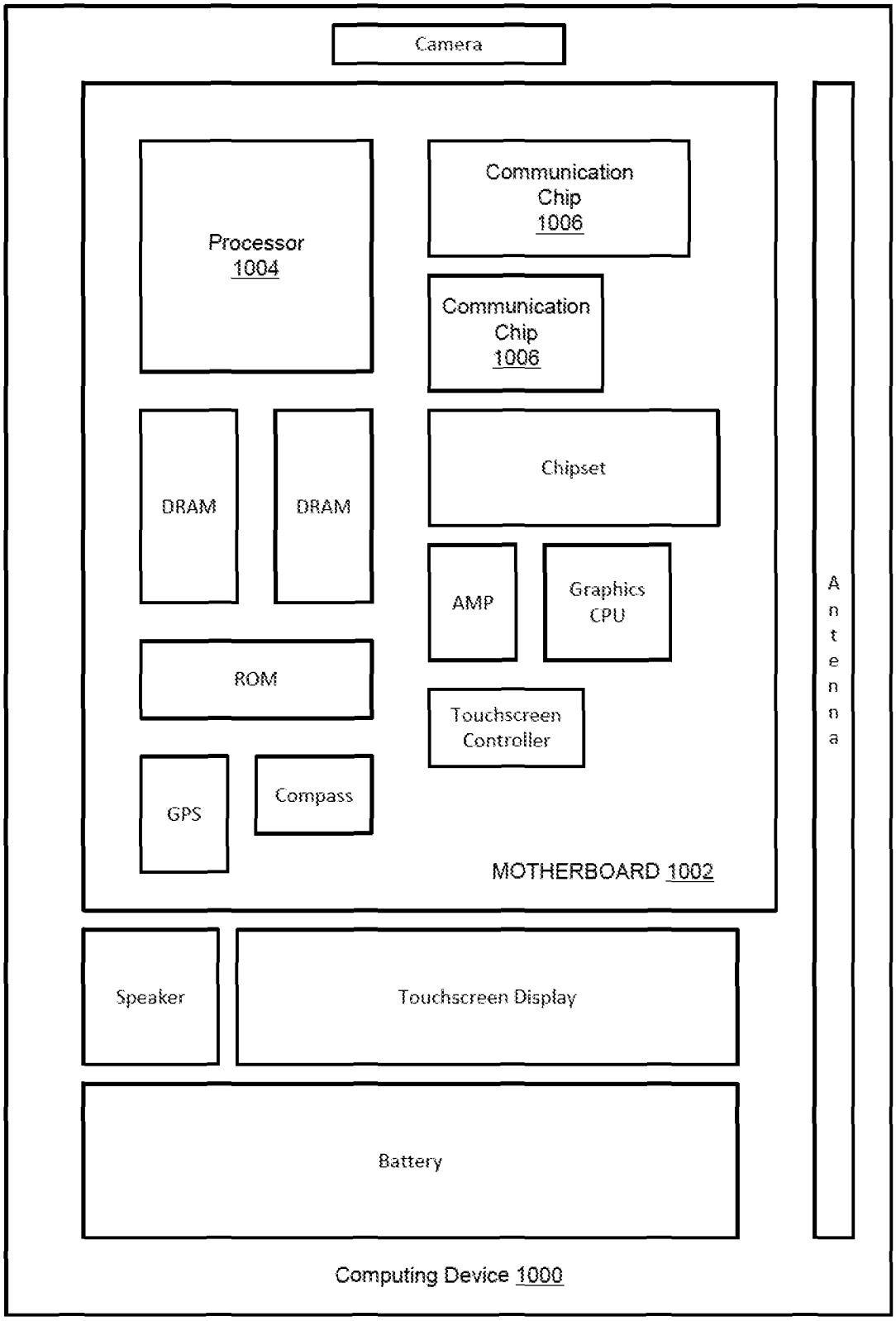

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 6