

## Description

### Background of the Invention

The present invention relates to an electrical resistor and an electron device employing it, and more particularly to techniques which are effective when applied to a thin-film resistor and a high-precision digital-to-analog (D/A) converter or analog-to-digital (A/D) converter employing it.

When it is intended to form a large number of resistors having a desired resistance value within a limited space as in a semiconductor wafer, the resistors are inevitably put into a curved shape on account of a limited layout space.

The inventors' study has revealed that the curved parts of the resistors form, for example, a cause for lowering the relative precision of the resistance values of the individual resistors.

The present invention has been made in quest of providing, in an electron device such as semiconductor device, a large number of resistors which are especially characterized by a high relative precision of resistance values.

### Summary of the Invention

Typical aspects of performance of the present invention will be summarized below.

#### Features of Single Resistor

A single resistor is as shown in Fig. 2(a).

(1) The flexional angle of the rectilinear sections or turn parts ( $a_1 - a_8$ ) of the resistor is set at an obtuse angle, for example,  $135^\circ$ .

(2) More preferably, the resistor is so shaped as to bend alternately bilaterally with respect to a phantom center line. That is, the resistor is so shaped as to have a first bent portion X (hatched in Fig. 2(a)) which lies on the right side of a plane bisected with the center line as a boundary and a second bent portion Y which lies on the left side.

(3) More preferably, the number, flexional angle and shape of the turn parts ( $a_3, a_4, a_7, a_8$ ) in the first bent portion X are made the same as those of the turn parts ( $a_1, a_2, a_5, a_6$ ) in the second bent portion Y.

(4) More preferably, the shape of a polygon enclosed with the outer edge of the first bent portion X and the phantom center line is made congruent or similar to the shape of a polygon enclosed with the outer edge of the second bent portion Y and the phantom center line.

These produce effects as follows.

Owing to (1), the deviation of a resistance value attributed to the processing error of the resistor can

be reduced. The reason is that the precision of etching processing is higher than in a case where the flexional angle is a right angle or an acute angle.

Owing to (2), deviations within a semiconductor wafer, for example, a deviation ascribable to evaporation in the case of forming thin-film resistors can be reduced. More specifically, in depositing aluminum or the like on the wafer by the use of vacuum evaporation, there might arise a tendency in which an evaporated thickness increases from the left toward the right of the wafer by way of example. Even in such a case, the changes of resistance values due to the deviation of the evaporated thickness are cancelled by the right and left bent portions which are alternately bent bilaterally with respect to the phantom center line.

Owing to (3) and (4), the deviation between the right and left portions with the phantom center line as the boundary is more effectively cancelled, and the deviation of the resistance value of the resistor can be minimized.

#### Features of Series Resistor (Ladder Resistor) with the Above Resistors connected in series

This series resistor has a folded-back portion and a non-folded-back portion.

In the non-folded-back portion, the resistors as described in (1) - (4) are connected in series and used, whereby the relative precision of the resistance values of the individual resistors is sharply enhanced as compared with that in a prior art.

In the folded-back portion, a resistor is used whose turn parts have the same shape as that of the turn parts of the resistor described in (1) - (4), thereby to prevent the disorder of the relative precision in this folded-back portion.

Another example of the folded-back portion has an arrangement in which rectilinear resistors are connected in parallel. In this case, the absolute deviation of a resistance value is diminished in correspondence with the parallel connection, with the result that the disorder of the relative precision in the folded-back portion can be prevented.

When an electron device such as A/D converter or D/A converter is constructed by the use of the above series resistor, the conversion precision thereof can be enhanced to achieve an enhanced performance.

#### Brief Description of the Drawings

Fig. 1(a) shows the plane shape of a thin-film resistor which was studied before the present invention by the inventors;

Fig. 1(b) is a plan view showing the corners of the resistor in Fig. 1(a) on enlarged scale;

Fig. 2(a) shows the plane shape of a thin-film resistor according to the present invention;

Fig. 2(b) is a plan view showing the corners of the resistor in Fig. 2(a) on enlarged scale;

Fig. 3 is a circuit diagram showing the circuit arrangement of an A/D converter;

Fig. 4 is a plan view for explaining the state of plane layout in a semiconductor integrated circuit in which the A/D converter shown in Fig. 3 is implemented;

Fig. 5 is a plan view showing the shape of a thin-film resistor portion indicated at A in Fig. 4;

Fig. 6 is a plan view showing an example of the shape of a thin-film resistor portion indicated at B in Fig. 4;

Fig. 7 is a plan view showing another example of the shape of the thin-film resistor portion indicated at B in Fig. 4; and

Fig. 8 is a circuit diagram showing the circuit arrangement of a D/A converter.

### Description of the Preferred Embodiments

#### Matters studied before the present invention by the inventors

As compared with a diffused layer resistor etc., a thin-film resistor made of a metallic resistor of aluminum or the like has the advantage that a resistance value of high precision can be attained reproducibly. Accordingly, it is used especially in a place requiring a high precision in a semiconductor integrated circuit device.

In, for example, a parallel type A/D converter, a common analog input voltage is applied to one input of each of a large number of voltage comparators, while reference voltages differing stepwise are respectively applied to the other inputs of the large number of voltage comparators, and a digital output corresponding to the input voltage is derived from the comparison output sides of the respective voltage comparators. To this end, a ladder resistor in which a large number of resistors of high relative precision are connected is necessitated. This ladder resistor is formed by connecting the aforementioned thin-film resistors in large numbers.

Here, let's consider the plane pattern shape of a thin-film resistor as shown in Figs. 1(a) and 1(b).

As illustrated in the figures, the thin-film resistor R1 is formed in such a way that the thin-film layer of a metallic resistor 1 of aluminum or the like is etched into a zigzagged plane pattern shape. The thin-film resistors R1 thus formed are connected in large numbers, whereby a resistor ladder for use in, e. g., an A/D converter is constructed. In this case, the plane pattern shape of the thin-film resistor is put into the bent shape for the purpose

of securing a large resistance value in a limited space.

The inventors have revealed, however, the problem that the thin-film resistor inevitably involves corners 1A and 1B of sharp angle (approximately 90 degrees) on account of the bending formation and that the corners 1A and 1B degrade the precision of the resistor R1.

Concretely, the inventors have revealed that as partly enlarged and shown in Fig. 1(b), the reproducibility of the shape of the corners 1A and 1B of the resistor 1 is limited by the precision of etching with photolithography, etc. so the effective resistor width W between the corners 1A and 1B changes irregularly, causing a discrepancy in the resistance value of the resistor R1. In Fig. 1(b),  $\Delta WA$  and  $\Delta WB$  indicate the deviations of dimensions at the corners 1A and 1B. In particular, the inner corner 1A tends to undergo more concentration of current than the outer corner 1B. Therefore, the dimensional deviation  $\Delta WA$  at the inner corner 1A forms a major cause for changing the resistance value of the resistor R1.

Accordingly, even when the ladder resistor is formed by the prior-art thin-film resistors R1 stated above, it has been very difficult to raise the relative precision among the individual resistors R1. For this reason, it has been difficult to attain a high resolution precision in a circuit whose precision depends upon the relative precision of a ladder resistor, for example, the parallel type A/D converter.

#### Embodiments

Now, typical embodiments of this invention will be described with reference to the drawings.

In the drawings, the same symbols indicate identical or corresponding portions.

Figs. 2(a) and 2(b) show an embodiment of a thin-film resistor according to this invention.

The thin-film resistor R1 shown in the figures is formed in such a way that a conductor layer of aluminum or the like is evaporated on the principal surface of an insulator film such as oxide film ( $\text{SiO}_2$  film) which is provided on a semiconductor wafer in a semiconductor integrated circuit device (IC), and that it is thereafter etched by the use of the photoetching process. The plane pattern shape of the thin-film resistor is bent zigzag in order to attain a large resistance value. Also, the corners 1A and 1B of the pattern are respectively formed at an obtuse angle (approximately 135 degrees).

Since the corners 1A and 1B are respectively formed at the obtuse angle in this manner, deformation ascribable to the etching becomes difficult to appear in the widthwise direction and dimensional deviations in the widthwise direction,

$\Delta W_A$  and  $\Delta W_B$  at the inner corner 1A and the outer corner 1B can be respectively suppressed small, as partially enlarged and illustrated in Fig. 2-(b). As a result, the deviation of a resistance value decreases, and especially in case of connecting a large number of such resistors into the ladder type, a high relative precision can be attained.

Fig. 3 shows an embodiment of a parallel type A/D converter to which this invention is applied.

As shown in the figure, the parallel type A/D converter is such that a common analog input voltage  $V_{in}$  15 applied to one input (+) of each of a large number of voltage comparators  $CP_1 - CP_n$ , while reference voltages  $V_{s1} - V_{sn}$  differing stepwise are respectively applied to the other inputs (-) of the large number of voltage comparators  $CP_1 - CP_n$ , and that a digital output  $D_{out}$  corresponding to the input voltage  $V_{in}$  is derived from the comparison output sides of the voltage comparators  $CP_1 - CP_n$ . In this case, the comparison outputs of the comparators  $CP_1 - CP_n$  are respectively provided in terms of the logic levels "1" and "0", and they are converted into alternative selection signals  $X_1 - X_n$  by logical product gates  $G_1 - G_n$  which are disposed in correspondence with the respective comparators  $CP_1 - CP_n$ . The selection signals  $X_1 - X_n$  are assembled into a binary code train of a predetermined number of digits by an encoder 3. The assembled code train becomes the digital output  $D_{out}$ .

Here, the respective reference voltages  $V_{s1} - V_{sn}$  are obtained in such a way that the voltage of a reference voltage source  $V_s$  is divided at equal intervals by a ladder resistor 10. The ladder resistor 10 is constructed in such a way that a large number of resistors  $R_1 - R_n$  having equal values to one another are connected in series.

The voltage comparators  $CP_1 - CP_n$  compare the respective reference voltages  $V_{s1} - V_{sn}$  divided by the ladder resistor 10 and the analog input voltage  $V_{in}$  applied in common.

Assuming now that the input voltage  $V_{in}$  be in a relationship of  $V_{sn-2} < V_{in} < V_{sn-1}$ , the output of the logical product (AND) gate  $G_{n-2}$  becomes the "H" level, and all the outputs of the other AND gates ( $G_1 - G_{n-3}$ ,  $G_{n-1}$  and  $G_n$ ) become the "L" level. Owing to the "H" level of the output of the AND gate  $G_{n-2}$ , it is decided that the input voltage is in the aforementioned relationship. The encoder 3 converts the decided result into the digital signal ( $D_{out}$ ) of desired bits. Then, an A/D conversion operation is completed.

The parallel type A/D converter of this sort can attain a very high conversion speed as compared with a follow-up type A/D converter. It is therefore suited to digitise high-speed analog signals, for example, video signals. This parallel type A/D converter, however, requires the ladder resistor 10 of

high relative precision in order to produce the reference voltages  $V_{s1} - V_{sn}$ . When the relative precision of the ladder resistor 10 is low, the resolution and linearity of a conversion characteristic are spoilt, and the so-called conversion error comes to arise. In an A/D converter to be described below, therefore, the ladder resistor 10 is constructed in such a way that thin-film resistors  $R_1 - R_n$  each having a plane pattern shape including a plurality of turn parts are connected in large numbers, and the relative precision among the individual resistors  $R_1 - R_n$  is raised in such a way that the corners of the pattern in the thin-film resistors  $R_1 - R_n$  are formed at an obtuse angle, whereby A/D conversion of high speed and high precision is permitted.

First, Fig. 4 shows the circuit of the A/D converter shown in Fig. 3, considering also a plane arrangement state in a silicon chip 100 in the IC implementation thereof. The A/D converter shown in the figure is similar circuit-wise to that shown in Fig. 3, and it is formed with a ladder resistor 10 as well as comparator circuit columns 2 which are divided and formed in a plurality of blocks. In each comparator circuit column 2, the large number of pairs of voltage comparators and logic gates shown in Fig. 3 are arrayed. The ladder resistor 10 is formed while being folded back between and around the comparator circuit blocks 2, 2' and 2". One end of the ladder resistor 10 is connected to the reference voltage source  $V_s$ , while the other end thereof is connected to the ground potential. The input voltage  $V_{in}$  is applied through an input pad 110. Logic outputs from the respective comparator circuit blocks are subjected to preliminary encoding based on wired logic, and are thereafter input to the encoder 3. The digital output  $D_{out}$  of the binary code train is delivered from the encoder 3 through an output pad 120.

Here, the ladder resistor 10 has a non-folded-back portion (rectilinear portion) which extends along the side part of the comparator circuit block 2 (2', 2''), a small round portion (a portion A enclosed with a dotted line in Fig. 4) which is folded back to back, and a large round portion (a portion B enclosed with a dotted line in Fig. 4) which strides over the end part of the comparator circuit block 2 (2', 2''). In the non-folded-back portion, the thin-film resistors  $R_1 - R_n$  shown in Fig. 2(a) are connected in series in large numbers. Besides, in the small round portion, a thin-film resistor  $R_{33}$  of a plane pattern shape indicated with hatching in Fig. 5 is arranged. Further, in the large round portion, a thin-film resistor  $R_{25}$  of a plane pattern shape as shown in Fig. 6 is arranged.

Likewise to the thin-film resistor  $R_{34}$  or  $R_{32}$  in the rectilinear portion, the thin-film resistor  $R_{33}$  shown in Fig. 5 has the plane pattern shape includ-

ing a plurality of turn parts and has the corners of the pattern formed at an obtuse angle. The thin-film resistor  $R_{33}$  in the small round portion is a resistor which connects the thin-film resistors  $R_{34}$  and  $R_{32}$  of the two rectilinear portions to each other, and the disorder of the relative precision of the ladder resistor is prone to occur here. However, the widths and lengths of the resistors are equalized, so that the resistors have resistance values equal to one another. Further, although the thin-film resistor  $R_{34}$  or  $R_{32}$  of the non-folded-back portion and the thin-film resistor  $R_{33}$  of the small round portion differ in the bending direction partly, the numbers and flexional angles of the turn parts  $a_1 - a_8$  of both the resistors are equalized to each other. Thus, even when some errors have developed in the precision of photoetching, for example, the positioning of a mask or the etching of the turn parts, the fluctuations of the resistance values attributed to the errors appear similarly in the thin-film resistor  $R_{32}$  or  $R_{34}$  of the non-folded-back portion and the thin-film resistor  $R_{33}$  of the small round portion. Accordingly, the thin-film resistor  $R_{33}$  of the small round portion has its absolute error suppressed small and can also have a very high relative precision to the thin-film resistor  $R_{32}$  or  $R_{34}$  of the non-folded-back portion.

Fig. 6 shows the plane pattern shape of the thin-film resistor  $R_{25}$  which is formed in the portion B enclosed with the dotted line in Fig. 4, namely, the large round folded-back portion.

As illustrated in Fig. 6, the thin-film resistor  $R_{25}$  formed in the large round folded-back portion has turn parts  $a_1' - a_8'$  which are identical in shape to the turn parts  $a_1 - a_8$  in the thin-film resistor  $R_{24}$  or  $R_{26}$  in the non-folded-back portion. In addition, the size of the plane shape is adjusted so that the resistance value of the resistor  $R_{25}$  may equalize to the resistance value of the resistor  $R_{24}$  or  $R_{26}$ .

In this case, the thin-film resistor  $R_{25}$  of the folded-back portion is formed by resistor portions  $R_C$  and  $R_D$  which have the turn parts identical in shape to those of the thin-film resistor  $R_{24}$  or  $R_{26}$  of the non-folded-back portion, and a broad oblong resistor  $R_E$  which is formed for interconnecting the resistor portions  $R_C$  and  $R_D$ .

The portions  $R_C$  and  $R_D$  are formed with the plurality of turn parts likewise to the thin-film resistor  $R_{24}$  or  $R_{26}$  in the non-folded-back portion, and the plane shape of the turn parts  $a_1' - a_8'$  is identical to that of the turn parts  $a_1 - a_8$  of the resistor  $R_{24}$  or  $R_{26}$ . On the other hand, the portion  $R_E$  has its length  $L_3$  determined to a magnitude necessary for striding over the end part of the comparator circuit (Fig. 4). Also, it has its width  $W_3$  held great so that its resistance value  $\Delta r$  may become sufficiently small.

Although the resistor  $R_{24}$  or  $R_{26}$  and the resis-

tor  $R_{25}$  differ in the plane shape and dimensions partly, they are identical in the shape of the turn parts ( $a_1 - a_8$ ,  $a_1' - a_8'$ ) to each other. Therefore, even when some errors have developed in the process of photoetching, for example, the positioning of a mask, the changes of the resistance values attributed to the errors appear similarly in both the thin-film resistor  $R_{24}$  or  $R_{26}$  of the non-folded-back portion and the resistor  $R_{25}$  of the large round folded-back portion. Accordingly, the thin-film resistor  $R_{25}$  of the large round folded-back portion can have a very high relative precision to the thin-film resistor  $R_{24}$  or  $R_{26}$  of the non-folded-back portion even when a trimming correction is not made.

Fig. 7 shows another example of the large round portion. This thin-film resistor  $R_{25}'$  is composed of a large number of rectilinear thin-film resistor pattern portions  $r_1 - r_k$ . The respective thin-film resistor pattern portions  $r_1 - r_k$  are connected in parallel to one another, and they are formed so that the combined parallel resistance thereof may equalize to the resistance value of the thin-film resistor  $R_{24}$  or  $R_{26}$ . In addition, the width  $W$  of each of the parallel resistors is equalized to the width  $W$  of the resistor in the rectilinear portion. When the large number of thin-film resistor pattern portions  $r_1 - r_k$  are connected in parallel in this manner, the extent of the deviations of resistance values to occur in the parallel resistors  $r_1 - r_k$  becomes equal to the extent of the deviations to occur in the resistors  $R_{24}$  and  $R_{26}$  in the rectilinear portions, and further, a resistance error to develop in each of the resistor pattern portions  $r_1 - r_k$  is diminished in accordance with the number of the pattern portions connected in parallel. Accordingly, the precision of this thin-film resistor  $R_{25}'$  of the large round portion can also be rendered high.

Fig. 8 shows an embodiment of a D/A converter to which this invention is applied.

The D/A converter shown in the figure has a decoder 4 which converts a digital input  $D_{in}$  into an alternative selection signal  $X_1 - X_n$ , analog switches  $S_1 - S_n$  which are individually controlled 'on' and 'off' by the selection signals  $X_1 - X_n$ , and a resistor ladder 10 which equally divides the voltage of a reference voltage source  $V_s$  so as to apply the divided voltage to one end of each of the analog switches  $S_1 - S_n$ . The other ends of the respective analog switches  $S_1 - S_n$  are connected in common, and an analog voltage  $V_{out}$  corresponding to the digital input  $D_{in}$  is output from the common connection point. Here, the ladder resistor 10 is constructed by the use of the thin-film resistors described before. Thus, the D/A converter whose conversion characteristic has a very high linearity precision can be provided.

The effects of the present invention thus far described are summed up below.

(1) The corners of a thin-film resistor in a plane pattern shape having a plurality of turn parts are formed at an obtuse angle. This produces the effect that the precision of the resistor can be raised.

(2) The thin-film resistor is bent alternately bilaterally with respect to a phantom center line, whereby the deviation of a resistance value can be cancelled in the right and left parts of the resistor.

(3) In a ladder resistor in which the thin-film resistors are connected in large numbers, the corners of a pattern in each thin-film resistor is formed at the obtuse angle, and the numbers and flexional angles of the turn parts of the patterns in the respective thin-film resistors are equalized to one another, whereby even when some errors have developed in the precision of etching, for example, the positioning of a mask, the fluctuations of resistance values ascribable to the errors arise similarly. This produces the effect that the relative precision among the resistors can be held high.

(4) In a ladder resistor which is folded back and formed, a thin-film resistor in a folded-back portion and a thin-film resistor in a non-folded-back portion are so formed that the plane shapes of turn parts in the respective portions are identical to each other. This produces the effect that, with the simple construction of merely altering the pattern shapes of the thin-film resistors, the relative precision between the thin-film resistor in the folded-back portion of the ladder resistor folded back and formed and the thin-film resistor in the non-folded-back portion can be raised reproducibly.

(5) Accordingly, the use of the ladder resistor can bring forth the effect that a parallel type A/D converter or D/A converter excellent in resolution and linearity can be provided.

The present invention can be variously modified. For example, the resistance values of the respective thin-film resistors  $R_1$ ,  $R_2$ , ... constituting the ladder resistor 10 may well be weighted. While, in the above, the invention made by the inventors has been chiefly described as to the application to the parallel type A/D conversion technology which is the background field of utilization, the invention is not restricted thereto but is also applicable to, for example, attenuator or regulated current circuit technology. The invention is applicable to devices which have at least the condition that resistors of high relative precision are required.

## Claims

1. A thin-film resistor made of a conductive layer formed on an insulating film on a semiconduc-

tor substrate,

characterised in that the conductive layer comprises a plurality of rectilinear sections (a1...a8) adjoining ones of which form an obtuse angle.

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2. The resistor of claim 1 wherein said conductive layer is formed by the use of a photolithographic process.

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3. The resistor of claim 1 or 2, comprising a first bent portion (X), and a second bent portion (Y), which joins to a terminal end of said first bent portion (X), wherein

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said first bent portion (X) is so shaped as to have a plurality of rectilinear sections (a3, a4, a7, a8) which extend at obtuse angles on one side of a plane bisected with a phantom center line as a boundary, said first bent portion extending from the phantom center line back to this phantom center line,

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said second bent portion (Y) is so shaped as to have a plurality of rectilinear sections (a1, a2, a5, a6) which extend at obtuse angles on the other side of the plane bisected with the phantom center line as the boundary, said second bent portion extending from the phantom center line back to this phantom center line, and

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the number and the obtuse angle of said rectilinear sections (a3, a4, a7, a8) in said first bent portion (X) being equal to those (a1, a2, a5, a6) in said second bent portion (Y).

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4. The resistor according to claim 3, wherein a polygon defined by said first bent portion (X) and the phantom center line is congruent or similar to a polygon defined by said second bent portion (Y) and the phantom center line.

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5. A ladder resistor comprising a plurality of resistors according to claim 3 or 4 connected in series.

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6. The ladder resistor of claim 5, comprising a non-folded-back portion (R32, R34; R24, R26) which extends in a predetermined direction, and

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a folded-back portion (R25; R33) which joins to a terminal of said non-folded-back portion and which is folded back at a predetermined angle to the predetermined direction,

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wherein said non-folded-back portion (R32; R34; R24, R26) is constructed by connecting the plurality of resistors according to claim 3 or 4 in series, and the resistor constituting said folded-back portion (R25; R33) is equal in the

(1) The corners of a thin-film resistor in a plane pattern shape having a plurality of turn parts are formed at an obtuse angle. This produces the effect that the precision of the resistor can be raised.

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(3) In a ladder resistor in which the thin-film resistors are connected in large numbers, the corners of a pattern in each thin-film resistor is formed at the obtuse angle, and the numbers and flexional angles of the turn parts of the patterns in the respective thin-film resistors are equalized to one another, whereby even when some errors have developed in the precision of etching, for example, the positioning of a mask, the fluctuations of resistance values ascribable to the errors arise similarly. This produces the effect that the relative precision among the resistors can be held high.

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(5) Accordingly, the use of the ladder resistor can bring forth the effect that a parallel type A/D converter or D/A converter excellent in resolution and linearity can be provided.

The present invention can be variously modified. For example, the resistance values of the respective thin-film resistors  $R_1$ ,  $R_2$ , ... constituting the ladder resistor 10 may well be weighted. While, in the above, the invention made by the inventors has been chiefly described as to the application to the parallel type A/D conversion technology which is the background field of utilization, the invention is not restricted thereto but is also applicable to, for example, attenuator or regulated current circuit technology. The invention is applicable to devices which have at least the condition that resistors of high relative precision are required.

#### Claims

1. A thin-film resistor made of a conductive layer formed on an insulating film on a semiconduc-

tor substrate,

characterised in that the conductive layer comprises a plurality of rectilinear sections (a1...a8) adjoining ones of which form an obtuse angle.

2. The resistor of claim 1 wherein said conductive layer is formed by the use of a photolithographic process.
3. The resistor of claim 1 or 2, comprising a first bent portion (X), and a second bent portion (Y), which joins to a terminal end of said first bent portion (X), wherein said first bent portion (X) is so shaped as to have a plurality of rectilinear sections (a3, a4, a7, a8) which extend at obtuse angles on one side of a plane bisected with a phantom center line as a boundary, said first bent portion extending from the phantom center line back to this phantom center line, said second bent portion (Y) is so shaped as to have a plurality of rectilinear sections (a1, a2, a5, a6) which extend at obtuse angles on the other side of the plane bisected with the phantom center line as the boundary, said second bent portion extending from the phantom center line back to this phantom center line, and the number and the obtuse angle of said rectilinear sections (a3, a4, a7, a8) in said first bent portion (X) being equal to those (a1, a2, a5, a6) in said second bent portion (Y).
4. The resistor according to claim 3, wherein a polygon defined by said first bent portion (X) and the phantom center line is congruent or similar to a polygon defined by said second bent portion (Y) and the phantom center line.
5. A ladder resistor comprising a plurality of resistors according to claim 3 or 4 connected in series.
6. The ladder resistor of claim 5, comprising a non-folded-back portion (R32, R34; R24, R26) which extends in a predetermined direction, and a folded-back portion (R25; R33) which joins to a terminal of said non-folded-back portion and which is folded back at a predetermined angle to the predetermined direction, wherein said non-folded-back portion (R32; R34; R24, R26) is constructed by connecting the plurality of resistors according to claim 3 or 4 in series, and the resistor constituting said folded-back portion (R25; R33) is equal in the



number of said rectilinear sections and the obtuse angle thereof to the resistor constituting said non-folded-back portion.

7. The ladder resistor of claim 6, wherein said folded-back portion (R25) is constructed of a plurality of rectilinear conductor films (r1...rk) which are connected in parallel, and the combined resistance value of which is approximate to the resistance value of the single resistor constituting said non-folded-back portion (R24, R26).

8. An electron device which employs a ladder resistor according to any of claims 5 to 7.

9. The electron device of claim 8, having an analog-to-digital converter which comprises a large number of voltage comparators (2) each of which has two input terminals, and a ladder resistor (10) according to any of claims 5 to 7,

wherein a fixed voltage is applied across both ends of said ladder resistor (10) thereby to generate a plurality of reference voltages which are successively different stepwise by voltage drops across the respective resistors (R1...R48) constituting said ladder resistor (10), the corresponding one of the reference voltages is applied to one input terminal of said each voltage comparator (2), an analog input voltage is applied to the other input terminals of said respective voltage comparators (2) in common, and a digital output corresponding to the input voltage is derived as an output of said each voltage comparator (2).

10. The electron device of claim 8, having a digital-to-analog converter, which comprises a decoder circuit (4) which delivers a set of digital signals corresponding to an input digital signal, and

switch means (S1...Sn) controlled by the outputs of said decoder circuit (4) to selectively supply an output terminal with a plurality of voltages of different values derived from said ladder resistor (10).

#### Revendications

1. Résistance à pellicule mince constituée par une couche conductrice formée sur une pellicule isolante sur un substrat semiconducteur, caractérisée en ce que la couche conductrice comprend une pluralité de sections rectilignes (a1...a8), des sections adjacentes faisant entre elles un angle obtus.

2. Résistance selon la revendication 1, dans laquelle ladite couche conductrice est formée moyennant l'utilisation d'un procédé photolithographique.

3. Résistance selon la revendication 1 ou 2, comprenant

une première partie coudée (X), et

une seconde partie coudée (Y), qui est réunie à une extrémité de ladite première partie coudée (X),

et dans laquelle

ladite première partie coudée (X) est conformée de manière à posséder une pluralité de sections rectilignes (a3,a4,a7,a8) qui s'étendent, en formant des angles obtus, d'un côté d'un plan subdivisé en deux par une ligne centrale imaginaire en tant que limite, ladite première partie coudée s'étendant à partir de la ligne centrale imaginaire pour revenir à cette ligne centrale imaginaire,

ladite seconde partie coudée (Y) est conformée de manière à posséder une pluralité de sections rectilignes (a1,a2,a5,a6) qui s'étendent, en formant des angles obtus, de l'autre côté du plan subdivisé en deux par la ligne centrale imaginaire en tant que limite, ladite seconde partie coudée s'étendant à partir de la ligne centrale imaginaire pour revenir à cette ligne centrale imaginaire, et

le nombre et l'angle obtus desdites sections rectilignes (a3,a4,a7,a8) de ladite première partie coudée (X) étant les mêmes que pour les sections (a1,a2,a5,a6) de ladite seconde partie coudée (Y).

4. Résistance selon la revendication 3, dans laquelle un polygone défini par ladite première partie coudée (X) et la ligne centrale imaginaire est congruent ou semblable à un polygone défini par ladite seconde partie coudée (Y) et la ligne centrale imaginaire.

5. Résistance en échelle comprenant une pluralité de résistances selon la revendication 3 ou 4 branchées en série.

6. Résistance en échelle selon la revendication 5, comprenant

une partie non repliée (R32,R34; R24, R26), qui s'étend dans une direction prédéterminée, et

une partie repliée (R25;R33), qui est raccordée à une borne de ladite partie non repliée et est repliée suivant un angle prédéterminé par rapport à la direction prédéterminée, et

dans laquelle ladite partie non repliée (R32,R34; R24,R26) est formée au moyen du



branchement en série de la pluralité de résistances selon la revendication 3 ou 4, et le nombre desdites sections rectilignes et l'angle obtus de ces sections de la résistance constituant ladite partie repliée (R25; R33) sont les mêmes que pour la résistance constituant ladite partie non repliée.

7. Résistance en échelle selon la revendication 6, dans laquelle ladite partie repliée (R25) est formée par une pluralité de pellicules conductrices rectilignes (r1...rk), qui sont branchées en parallèle et dont la valeur résistive combinée est égale approximativement à la valeur résistive de la résistance unique constituant ladite partie non repliée (R24, R26).
8. Dispositif électronique utilisant une résistance en échelle selon l'une quelconque des revendications 5 à 7.
9. Dispositif électronique selon la revendication 8, possédant un convertisseur analogique/numérique qui comprend
  - un nombre élevé de comparateurs de tension (2) dont chacun possède deux bornes d'entrée, et
  - une résistance en échelle (10) selon l'une quelconque des revendications 5 à 7, et
  - dans lequel une tension fixe est appliquée aux deux extrémités de ladite résistance en échelle (10) de manière à produire une pluralité de tensions de référence, qui diffèrent successivement pas-à-pas, de chutes de tension aux bornes des résistances respectives (R1...R48) constituant ladite résistance en échelle (10), l'une correspondante des tensions de référence est appliquée à une borne d'entrée de chacun desdits comparateurs de tension (2), une tension d'entrée analogique est appliquée en commun aux autres bornes d'entrée desdits comparateurs de tension respectifs (2), et un signal de sortie numérique correspondant à la tension d'entrée est obtenu en tant que signal de sortie de chacun desdits comparateurs de tension (2).
10. Dispositif électronique selon la revendication 8, comportant un convertisseur numérique/analogique, qui comprend
  - un circuit décodeur (4) qui délivre un ensemble de signaux numériques correspondant à un signal numérique d'entrée, et
  - des moyens de commutation (S1...Sn) commandés par les sorties dudit circuit décodeur (4) pour envoyer de façon sélective à une borne de sortie une pluralité de tensions ayant des valeurs différentes et tirées de ladite résis-

tance en échelle (10).

#### Patentansprüche

1. Dünnschicht-Widerstand, der aus einer auf einer Isolierschicht auf einem Halbleitersubstrat angeordneten leitfähigen Schicht besteht, dadurch gekennzeichnet, daß die leitfähige Schicht mehrere geradlinige Abschnitte (a1...a8) umfaßt, wobei benachbarte Abschnitte einen stumpfen Winkel miteinander bilden.
2. Widerstand nach Anspruch 1, wobei die leitfähige Schicht unter Anwendung eines photolithographischen Verfahrens hergestellt ist.
3. Widerstand nach Anspruch 1 oder 2, mit einem ersten geknickten Abschnitt (X) und einem zweiten geknickten Abschnitt (Y), der an ein Anschlußende des ersten geknickten Abschnitts (X) anschließt, wobei der erste geknickte Abschnitt (X) aus mehreren geradlinigen Abschnitten (a3, a4, a7, a8) geformt ist, die unter stumpfen Winkeln auf einer Seite einer mit einer gedachten Linie als Grenze unterteilten Ebene verlaufen, wobei der erste geknickte Abschnitt von der gedachten Mittellinie ausgeht und zu dieser zurück verläuft, wobei der zweite geknickte Abschnitt (Y) aus mehreren geradlinigen Abschnitten (a1, a2, a5, a6) geformt ist, die unter stumpfen Winkeln auf der anderen Seite der mit der gedachten Mittellinie als Grenze unterteilten Ebene verlaufen, wobei der zweite geknickte Abschnitt von der gedachten Mittellinie ausgeht und zu dieser zurück verläuft, und wobei die Anzahl und der stumpfe Winkel der geradlinigen Abschnitte (a3, a4, a7, a8) in dem ersten geknickten Abschnitt (X) gleich ist wie bei denen (a1, a2, a5, a6) in dem zweiten geknickten Abschnitt (Y).
4. Widerstand nach Anspruch 3, wobei ein von dem ersten geknickten Abschnitt (X) und der gedachten Mittellinie gebildetes Vieleck zu einem von dem zweiten geknickten Abschnitt (Y) und der gedachten Mittellinie gebildeten Vieleck kongruent oder ähnlich ist.
5. Leiterwiderstand, bestehend aus mehreren in Serie geschalteten Widerständen nach Anspruch 3 oder 4.
6. Leiterwiderstand nach Anspruch 5, mit einem in einer vorgegebenen Richtung verlaufenden nichtgefalteten Abschnitt (R32, R34; R24, R26) und



einem gefalteten Abschnitt (R25; R33), der an einen Anschluß des nicht-gefalteten Abschnitts anschließt und unter einem vorgegebenen Winkel zu der vorgegebenen Richtung gefaltet ist,

wobei der nicht-gefaltete Abschnitt (R32, R34; R24, R26) aus einer Serienschaltung mehrerer Widerstände nach Anspruch 3 oder 4 aufgebaut ist und der den gefalteten Abschnitt (R25; R33) bildende Widerstand hinsichtlich der Anzahl von geradlinigen Abschnitten und des stumpfen Winkels gleich ist mit dem den nicht-gefalteten Abschnitt bildenden Widerstand.

7. Leiterwiderstand nach Anspruch 6, wobei der gefaltete Abschnitt (R25) aus mehreren parallel geschalteten geradlinigen Leiterschichten ( $r_1 \dots r_k$ ) aufgebaut ist und sein kombinierter Widerstandswert etwa gleich ist dem Widerstandswert des den nicht-gefalteten Abschnitt (R24, R26) bildenden Einzelwiderstands.

8. Elektronisches Gerät mit einem Leiterwiderstand nach einem der Ansprüche 5 bis 7.

9. Elektronisches Gerät nach Anspruch 8, enthaltend einen Analog/Digital-Umsetzer mit einer großen Anzahl von Spannungskomparatoren (2), deren jeder zwei Eingangsklemmen aufweist, und

einem Leiterwiderstand (10) nach einem der Ansprüche 5 bis 7,

wobei zwischen beiden Enden des Leiterwiderstands (10) eine feste Spannung liegt, um mehrere Bezugsspannungen zu erzeugen, die sich durch Spannungsabfälle an den jeweiligen, den Leiterwiderstand (10) bildenden Widerständen ( $R_1 \dots R_{48}$ ) nacheinander schrittweise unterscheiden, wobei an einer Eingangsklemme jedes Spannungskomparators (2) die entsprechende Bezugsspannung und an der anderen Eingangsklemme der Spannungskomparatoren (2) gemeinsam eine analoge Eingangsspannung liegt, und wobei am Ausgang jedes Spannungskomparators (2) ein der Eingangsspannung entsprechendes digitales Ausgangssignal auftritt.

10. Elektronisches Gerät nach Anspruch 8, umfassend einen Digital/Analog-Umsetzer mit einer Decoderstufe (4), die einen einem digitalen Eingangssignal entsprechenden Satz von Digitalsignalen abgibt, und

eine von den Ausgangssignalen der Decoderstufe (4) gesteuerte Schalteinrichtung ( $S_1 \dots S_n$ ), die eine Ausgangsklemme selektiv mit mehreren von dem Leiterwiderstand (10)

abgeleiteten Spannungen unterschiedlicher Größe versorgt.

