

Description

This invention relates to a video display system having automatic adjustment of the peak beam current and more particularly to a control circuit for automatically adjusting the peak beam cathode current in a television receiver or a similar apparatus of the type having a display tube to which a video signal is supplied.

Excessive beam currents can cause the cathode ray tube (CRT) of a television receiver to produce a degraded image. For example, in a conventional system for driving the picture tube, a voltage amplifier drives the cathode of the picture tube directly. During the picture display periods of the television signal the instantaneous amplitude of the beam current may rise beyond the level at which it remains in reasonable focus because of limitations in the performance of the electron gun assembly. Displayed captions, for example, can become illegible as a result of this poor focusing.

Many circuits for automatically controlling the beam current have been suggested in the prior art for example in US Patent No. 4,017,681. Quite a few of these prior art systems control excessive beam current by responding to the average beam current. In this type of system the full dynamic range of the television tube cannot be used since the average value of the beam current must be set where the peak beam current does not affect the focus of the tube.

Another problem with some prior art beam leveler circuits such as that disclosed in US Patent No. 3,855,614 is that detection of the cathode current occurs during the horizontal retrace intervals wherein the video signal corresponds to the black level. This results in a disadvantage because the detected level of the cathode current is defined relative to the actual black level of the video signal. Moreover, it is not unusual to have detection during the horizontal retrace interval manifest itself as a light track on the screen and thus disturb the picture, at least in dark surroundings. Moreover, since detection of the beam current occurs during the previous retrace interval, instantaneous and automatic adjustment of the cathode current is not provided by these systems but rather is delayed to the next trace and retrace interval.

Summary of the Invention

Accordingly, the present invention provides a video display system including a cathode ray tube having at least one cathode, video processing circuitry responsive to an applied video signal to produce cathode beam current flow in the cathode and a cathode beam current limiting circuit, wherein the cathode beam current limiting circuit comprises:

a first transistor the emitter-collector path of which is connected in series with the cathode so that the instantaneous cathode beam current flows through the transistor; a first resistor connected to said collector of said first transistor, a voltage being developed across the resistor, the magnitude of which is related to said instantane-

ous cathode beam current; a video amplifier coupled between the video processing circuit and the base of said first transistor for controlling the conduction thereof; a reference potential circuit which provides an adjustable voltage potential at a first circuit node; a second transistor having an emitter coupled to said collector of said first transistor, a base connected to said first circuit node and a collector coupled to a control terminal of said video amplifier, said second transistor being rendered conductive to conduct excess instantaneous cathode peak beam current as the voltage developed across said resistor exceeds said adjustable voltage potential; and integrating circuitry responsive to said second transistor being rendered conductive to provide a gain control signal at said control terminal of said video amplifier to thereby adjust the gain thereof to limit the instantaneous cathode beam current to a predetermined value. Thus, the present invention automatically adjusts the instantaneous level of the peak beam current to maintain good focus in the video display system.

Brief Description of the Drawings

FIG. 1 is a block diagram of a color television receiver including a peak beam leveler circuit of the embodiment of the invention;

FIG. 2 is a schematic diagram illustrating the peak beam leveler circuit of the present invention.

Detailed Description of the Preferred Embodiment

FIG. 1 illustrates in block diagram form a general arrangement of color television receiver 10 employing the circuit of the preferred embodiment of the present invention. As shown, a radio frequency composite television signal is received at antenna 12 and is supplied to video processing circuit 14. As is understood, video processing circuit 14 generates a plurality of output signals which are utilized to provide an audio output from sound system 16, synchronizing components to sweep signal system 18, and a composite video signal containing chrominance and luminance components which are applied to the chrominance and luminance processing channels of the television, respectively. Thus, an output of video processing circuit 14 is provided to chrominance channel 20 and to luminance channel 22 as is known to those familiar to the art.

Chrominance channel 20 includes a frequency selection unit 24 for selectively coupling the chrominance component to chrominance processing unit 26 for deriving the R-Y, B-Y and G-Y color difference signals as is known. These color difference signals are then combined in video matrix circuit 28 with a luminance signal Y supplied from luminance channel 22 to produce the red, blue and green color signals in the television receiver.

A luminance processing circuit 30 of luminance channel 22 serves to amplify and otherwise process the luminance component of the composite video signal to supply the luminance signal Y to video matrix 28.

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The individual red, blue and green color signals derived at respective outputs of video matrix 28 may be supplied over respective conductors 32, 34 and 36 to individual video amplifiers 38, 40, and 42. The amplified color signals are coupled from the outputs of video amplifiers 38, 40, and 42 to respective cathodes of cathode ray tube 44 to generate the color television signals.

In the preferred embodiment of the present invention, the instantaneous peak beam current associated with each cathode 46, 48 and 50 is detected by peak beam leveler circuit 52 to derive an output control signal to adjust the gain of gain controlled video amplifiers 38, 40 and 42 as will be hereinafter explained in greater detail.

Turning to FIG. 2 there is shown peak beam leveler circuit 52 of the present invention. It is to be understood that peak beam current leveler circuit 52 may be utilized in both monochrome and color television receivers in the preferred embodiment. Therefore, although the following description for the operation of peak beam leveler circuit 52 is in conjunction with the color television receiver 10 shown in FIG. 1 it is to be realized that in a monochrome television receiver system a single gain control video amplifier could be controlled to adjust the peak beam current passing through to the cathode of the cathode ray tube supplied in such a television receiver as is shown in FIG. 2. As illustrated in FIG. 2, peak beam current leveler circuit 52 is shown coupled to only one cathode of the cathode ray tube 44. It is to be understood that components in FIG. 2 corresponding to those in FIG. 1 are referenced by the same reference numerals.

For illustration purposes peak beam current leveler circuit 52 is shown coupled with one of the video amplifiers which may for instance be video amplifier 38 of FIG. 1. In this example then the cathode of cathode ray tube 44 would correspond to cathode 46 of FIG. 1. Hence the video input to amplifier 38 at terminal 54 would correspond to the red color signal. The amplified video signal from gain controlled video amplifier 38 is applied to the base of high voltage PNP transistor 56 which in the preferred embodiment would be an external transistor: peak beam current leveler circuit 52 being shown in dashed outline form to suggest that it is suitable for manufacture in integrated circuit form. The cathode 46 is driven by the emitter follower action of transistor 56 which implies that the emitter of this transistor passes all of the cathode beam current provided by video gain controlled amplifier 38. It is also assumed that the collector current of transistor 56 is substantially equal to the emitter current such that the total beam cathode current is produced at the output of the collector of transistor 56. The collector of transistor 56 is shown as being connected to an external resistor 58 which is returned to ground reference terminal 60 and also to terminal 62 of beam current leveler circuit 52. Terminal 62 is connected at node 64 to an internal resistor 66 which is returned to ground reference terminal 60 at terminal 68. The emitter electrode

of internal PNP transistor 70 is connected to terminal 64. The base of transistor 70 is connected at terminal 72 to a voltage reference potential with the collector thereof being connected to the base of NPN transistor 74. If peak beam current leveler circuit 52 is to be incorporated into the color television receiver 10 two additional transistors having their base and collector electrodes coupled in parallel with the base and collector electrodes of transistor 70 would be provided with their respective emitter electrodes being coupled to respective external PNP transistors in the same manner as shown for transistor 70 and transistor 56. One such additional transistor 75 is shown in phantom form. As an example, the emitter of transistor 75 would be connected to the collector of an external PNP transistor in the same manner shown for transistor 70. In this configuration, peak beam current leveler circuit 52 would be continuously sampling the instantaneous peak beam cathode currents in all three cathodes of the color television receiver.

The aforementioned voltage reference potential supplied at terminal 72 is established across resistor 76 which is connected between terminal 72 and terminal 78 at which is supplied ground reference potential 60. The magnitude of the voltage reference potential supplied at terminal 72 is set by the collector current of multiple collector PNP transistor 80 which has the emitter thereof connected at terminal 82 to a source of operating potential V and one collector connected to terminal 72. The other collector of transistor 80 is coupled with its base to terminal 84. An external bias resistor 86 is connected between ground reference 60 and terminal 84. In the system, the magnitude of the voltage reference potential appearing at terminal 72 can be adjusted by changing the value of external bias resistor 86.

The base electrode of transistor 74 is connected in series with the collector of transistor 70. The emitter electrode of this transistor is connected to terminal 88 to ground reference 60. The collector of transistor 74 is coupled to output terminal 90 of peak beam current leveler circuit 52. An external integrating circuit comprising capacitor 92 and resistor 94 coupled in series with each other with the common junction therebetween being connected to terminal 90. A bias potential, V bias, is supplied at terminal 96 to resistor 94. Terminal 90 is shown as being connected to the gain control terminal of video amplifier 38 such that any control signals generated at terminal 90 will adjust the gain of the video signal appearing at the output of video amplifier 38 accordingly.

In operation, the beam current in each cathode of cathode ray tube 44 is monitored by a respective transistor 56. The peak beam cathode current appearing as the collector current of transistor 56 produces a voltage across resistor 66 which appears at terminal 64 and is applied to the emitter of transistor 70. If the magnitude of the voltage at terminal 64 becomes greater than the magnitude of the voltage reference appearing at terminal 72 plus the base-to-emitter voltage of

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transistor 70, the excess peak beam current will be passed through the emitter of transistor 70 to render transistor 74 conductive. Thus, the excess peak beam current produces collector current in transistor 74 which is integrated by the resistance-capacitor network. This signal then appears as an output control signal from peak beam current leveler circuit 52 to control the gain of gain controlled video amplifier 38 such that the higher the peak beam current the more gain reduction occurs through video amplifier 38.

Additionally, it is to be recognized that peak beam leveler circuit 52 may be utilized to control the average beam current by integrating the collector current of transistor 56 in addition to integrating the collector current of transistor 74. Hence, the voltage appearing at the collector of transistor 74 could then control automatically the brightness of the displayed picture appearing on cathode ray tube 44.

What has been described above then is a novel peak beam current leveler circuit suitable for use in a television receiver for sampling the instantaneous peak beam cathode current in the cathode ray tube of the television receiver. The sampled peak beam current is utilized to produce a voltage which is compared with a reference voltage to produce a control voltage for automatically adjusting the level of the peak beam current if its magnitude should be in excess of a predetermined level.

Claims

1. A video display system (10) including a cathode ray tube (44) having at least one cathode (46), video processing circuitry (24, 20, 22, 23) responsive to an applied video signal to produce cathode beam current flow in the cathode and a cathode beam current limiting circuit (38, 52, 56, 58), characterized in that the cathode beam current limiting circuit comprises:

a first transistor (56) the emitter-collector path of which is connected in series with the cathode (46) so that the instantaneous cathode beam current flows through the transistor (56); a first resistor (58) connected to said collector of said first transistor, a voltage being developed across the resistor (58), the magnitude of which is related to said instantaneous cathode beam current; a video amplifier (38) coupled between the video processing circuit (24, 20, 22, 28) and the base of said first transistor (56) for controlling the conduction thereof; a reference potential circuit (76, 80, 86) which provides an adjustable voltage potential at a first circuit node (72); a second transistor (70) having an emitter coupled to said collector of said first transistor (56), a base connected to said first circuit node (72) and a collector coupled to a control terminal of said video amplifier (38), said second transistor (70) being rendered conductive to conduct excess instantaneous cathode peak beam current as the voltage developed across said resistor (58) exceeds said adjustable voltage potential; and integrating circuitry (92, 94) re-

sponsive to said second transistor being rendered conductive to provide a gain control signal at said control terminal of said video amplifier (38) to thereby adjust the gain thereof to limit the instantaneous cathode beam current to a predetermined value.

2. The video system of claim 1 characterised in that said reference potential circuit (76, 80, 86) includes a third transistor having an emitter coupled to a first power supply conductor (82) to which is supplied a dc operating potential (V), a collector coupled to said first circuit node (72) and a base; a second resistor (86) coupled between said base of said third transistor (80) and a second power supply conductor (60); and a third resistor (76) connected between said first circuit node (72) and said second power supply conductor (60).

3. The video display system of claim 2 characterised in that a fourth transistor (74) is included having a base coupled to said collector of said second transistor (70) an emitter coupled to said second power supply conductor and a collector coupled to said control terminal of said video amplifier (38).

4. A television receiver incorporating a video display system (10) and cathode beam current limiting circuit (52, 56) according to any preceding claim.

Patentansprüche

1. Videoanzeigesystem (10) mit einer Kathodenstrahlröhre (44), die wenigstens eine Kathode (46) aufweist, einer Videoverarbeitungsschaltung (24, 20, 22, 23), die auf ein zugeführtes Videosignal anspricht, um einen Kathodenstrahlstromfluß in der Kathode hervorzurufen, und einer Kathodenstrahlstrombegrenzungsschaltung (38, 52, 56, 58), dadurch gekennzeichnet, daß die Kathodenstrahlstrombegrenzungsschaltung enthält:

einen ersten Transistor, dessen Emittor/Kollektor-Strecke in Serie mit der Kathode (46) geschaltet ist, so daß der augenblickliche Kathodenstrahlstrom durch den Transistor (56) fließt; einen ersten Widerstand (58), der mit dem Kollektor des ersten Transistors verbunden ist, wobei eine Spannung über dem Widerstand (58) entwickelt wird, deren Größe auf den augenblicklichen Kathodenstrahlstrom bezogen ist; einen Videoverstärker (38), der zwischen die Videoverarbeitungsschaltung (24, 20, 22, 28) und die Basis des ersten Transistors (56) geschaltet ist, um dessen Leitfähigkeit zu steuern; eine Bezugspotentialschaltung (76, 80, 86), die ein einstellbares Spannungspotential an einem ersten Schaltungsknoten (72) zur Verfügung stellt; einen zweiten Transistor (70), dessen Emittor mit dem Kollektor des ersten Transistors (56) verbunden ist, wobei dessen Basis mit dem ersten Schaltungsknoten (72) verbunden ist und der Kollektor mit einem Steueranschluß des Videoverstärkers (38) verbunden ist, wobei der zweite Transistor (70) leitfähig gemacht wird, um einen übermäßigen augenblicklichen Kathodenspitzenstrahlstrom zu leiten, wenn die Spannung, die sich über dem

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transistor 70, the excess peak beam current will be passed through the emitter of transistor 70 to render transistor 74 conductive. Thus, the excess peak beam current produces collector current in transistor 74 which is integrated by the resistance-capacitor network. This signal then appears as an output control signal from peak beam current leveler circuit 52 to control the gain of gain controlled video amplifier 38 such that the higher the peak beam current the more gain reduction occurs through video amplifier 38.

Additionally, it is to be recognized that peak beam leveler circuit 52 may be utilized to control the average beam current by integrating the collector current of transistor 56 in addition to integrating the collector current of transistor 74. Hence, the voltage appearing at the collector of transistor 74 could then control automatically the brightness of the displayed picture appearing on cathode ray tube 44.

What has been described above then is a novel peak beam current leveler circuit suitable for use in a television receiver for sampling the instantaneous peak beam cathode current in the cathode ray tube of the television receiver. The sampled peak beam current is utilized to produce a voltage which is compared with a reference voltage to produce a control voltage for automatically adjusting the level of the peak beam current if its magnitude should be in excess of a predetermined level.

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sponsive to said second transistor being rendered conductive to provide a gain control signal at said control terminal of said video amplifier (38) to thereby adjust the gain thereof to limit the instantaneous cathode beam current to a predetermined value.

2. The video system of claim 1 characterised in that said reference potential circuit (76, 80, 86) includes a third transistor having an emitter coupled to a first power supply conductor (82) to which is supplied a dc operating potential (V), a collector coupled to said first circuit node (72) and a base; a second resistor (86) coupled between said base of said third transistor (80) and a second power supply conductor (60); and a third resistor (76) connected between said first circuit node (72) and said second power supply conductor (60).

3. The video display system of claim 2 characterised in that a fourth transistor (74) is included having a base coupled to said collector of said second transistor (70) an emitter coupled to said second power supply conductor and a collector coupled to said control terminal of said video amplifier (38).

4. A television receiver incorporating a video display system (10) and cathode beam current limiting circuit (52, 56) according to any preceding claim.

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1. Videoanzeigesystem (10) mit einer Kathodenstrahlröhre (44), die wenigstens eine Kathode (46) aufweist, einer Videoverarbeitungsschaltung (24, 20, 22, 23), die auf ein zugeführtes Videosignal anspricht, um einen Kathodenstrahlstromfluß in der Kathode hervorzurufen, und einer Kathodenstrahlstrombegrenzungsschaltung (38, 52, 56, 58), dadurch gekennzeichnet, daß die Kathodenstrahlstrombegrenzungsschaltung enthält:

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Widerstand (58) entwickelt, das einstellbare Spannungspotential übersteigt; und eine Integrierschaltung (92, 94), die darauf anspricht, daß der zweite Transistor leitfähig gemacht ist, um ein Verstärkungssteuersignal an dem Steueranschluß des Videoverstärkers (38) bereitzustellen, um dadurch dessen Verstärkung einzustellen, um den augenblicklichen Kathodenstrahlstrom auf einen vorbestimmten Wert zu begrenzen.

2. Videosystem nach Anspruch 1, dadurch gekennzeichnet, daß die Bezugspotentialschaltung (76, 80, 86) enthält: einen dritten Transistor, dessen Emitter mit einem ersten Stromzuführungsleiter (82) verbunden ist, dem ein Gleichspannungs-Betriebspotential (V) zugeführt ist, mit einem Kollektor, der mit dem ersten Schaltungsknoten (72) verbunden ist, und einer Basis; einen zweiten Widerstand (86), der zwischen die Basis des dritten Transistors (80) und einen zweiten Stromversorgungsleiter (60) geschaltet ist; und einen dritten Widerstand (76), der zwischen den ersten Schaltungsknoten (72) und den zweiten Stromversorgungsleiter (60) geschaltet ist.

3. Videoanzeigesystem nach Anspruch 2, dadurch gekennzeichnet, daß ein vierter Transistor (74) enthalten ist, mit einer Basis, die mit dem Kollektor des zweiten Transistors (70) verbunden ist, einem Emitter, der mit dem zweiten Stromzuführungsleiter verbunden ist, und einem Kollektor, der mit dem Steueranschluß des Videoverstärkers (38) verbunden ist.

4. Fernsehempfänger, enthaltend ein Videoanzeigesystem (10) und eine Kathodenstrahlstrombegrenzungsschaltung (52, 56) nach einem der vorhergehenden Ansprüche.

Revendications

1. Système de visualisation (10) incluant un tube à rayons cathodiques (44) comportant au moins une cathode (46), un circuit de traitement de signaux vidéo (24, 20, 22, 23) sensible à un signal vidéo appliqué pour produire un passage de courant de faisceau de cathode dans la cathode et un circuit de limitation de courant de faisceau de cathode (38, 52, 56, 58), caractérisé en ce que le circuit de limitation de courant de faisceau de cathode comprend:

un premier transistor (56) dont le chemin d'émetteur-collecteur esxt connecté en série à la cathode (46) de sorte que le courant de faisceau de cathode instantané passe dans le transistor

(56); une première résistance (58) connectée au collecteur du premier transistor, une tension étant produite dans la résistance (58) dont l'amplitude est fonction du courant de faisceau de cathode instantané; un amplificateur vidéo (38) couplé entre le circuit de traitement de signaux vidéo (24, 20, 22, 28) et la base du premier transistor (56) pour régler sa conduction; un circuit de potentiel de référence (76, 80, 86) qui fournit un potentiel de tension réglage à un premier noeud de circuit (72); un deuxième transistor (70) ayant un émetteur couplé au collecteur du premier transistor (56), une base connectée au premier noeud de circuit (72) et un collecteur couplé à une borne de commande de l'amplificateur vidéo (38), le deuxième transistor (70) étant rendu conducteur pour conduire un courant de faisceau de crête de cathode instantané en excès quand la tension produite dans la résistance (58) dépasse le potentiel de tension de réglage; et un circuit d'intégration (92, 94) sensible au deuxième transistor rendu conducteur pour fournir un signal de réglage de gain à la borne de commande de l'amplificateur vidéo (38) pour régler de la sorte son gain afin de limiter le courant de faisceau de cathode instantané à une valeur prédéterminée.

2. Système de visualisation selon la revendication 1, caractérisé en ce que le circuit à potentiel de référence (76, 80, 86) comprend un troisième transistor ayant un émetteur couplé à un premier conducteur de source d'alimentation (82) auquel est fournie une tension de fonctionnement en courant continu (V), un collecteur couplé au premier noeud de circuit (72) et une base; une deuxième résistance (86) couplée entre la base du troisième transistor (80) et un second conducteur de source d'alimentation (60); et une troisième résistance (76) connectée entre le premier noeud de circuit (72) et le second conducteur de source d'alimentation (60).

3. Système de visualisation selon la revendication 2, caractérisé en ce qu'un quatrième transistor (74) est inclus qui comporte une base couplée au collecteur du deuxième transistor (70), un émetteur couplé au second conducteur de source d'alimentation et un collecteur couplé à la borne de commande de l'amplificateur vidéo (38).

4. Récepteur de télévision incorporant un système de visualisation (10) et un circuit de limitation de courant de faisceau de cathode (52, 56) selon l'une quelconque des revendications 1 à 3.

