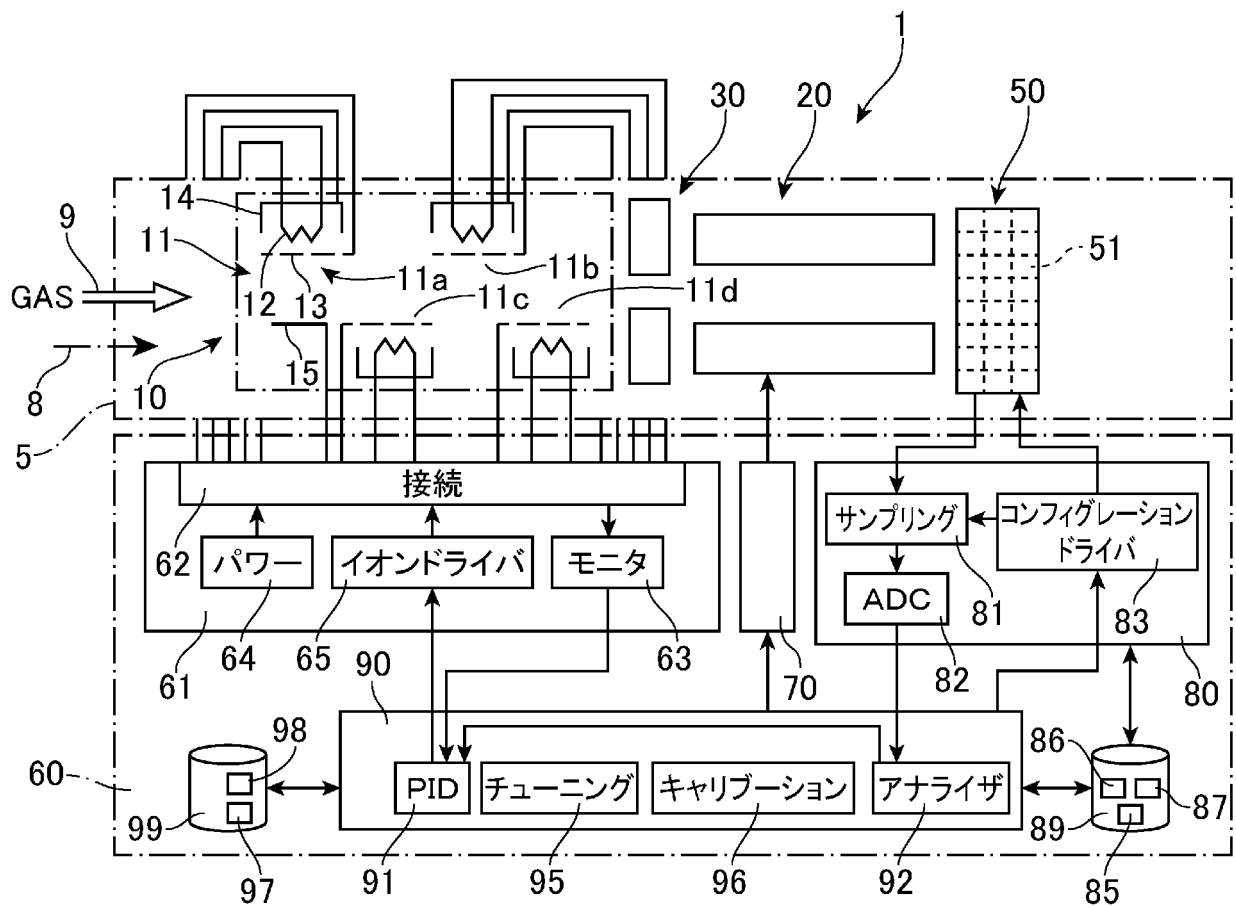
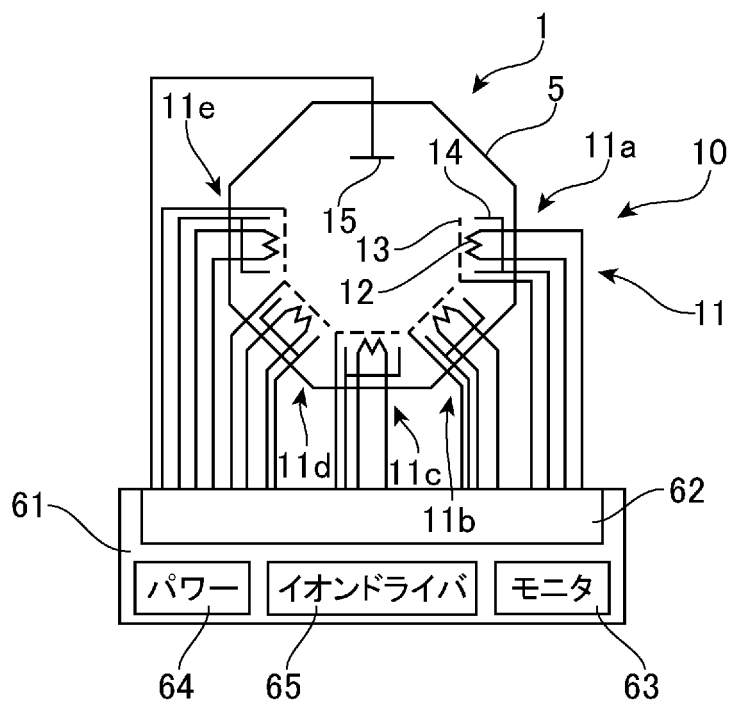


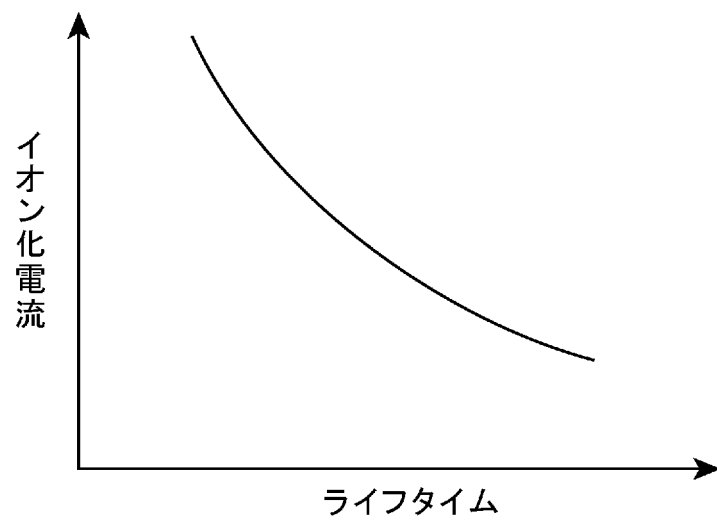
[図1]



[図2]

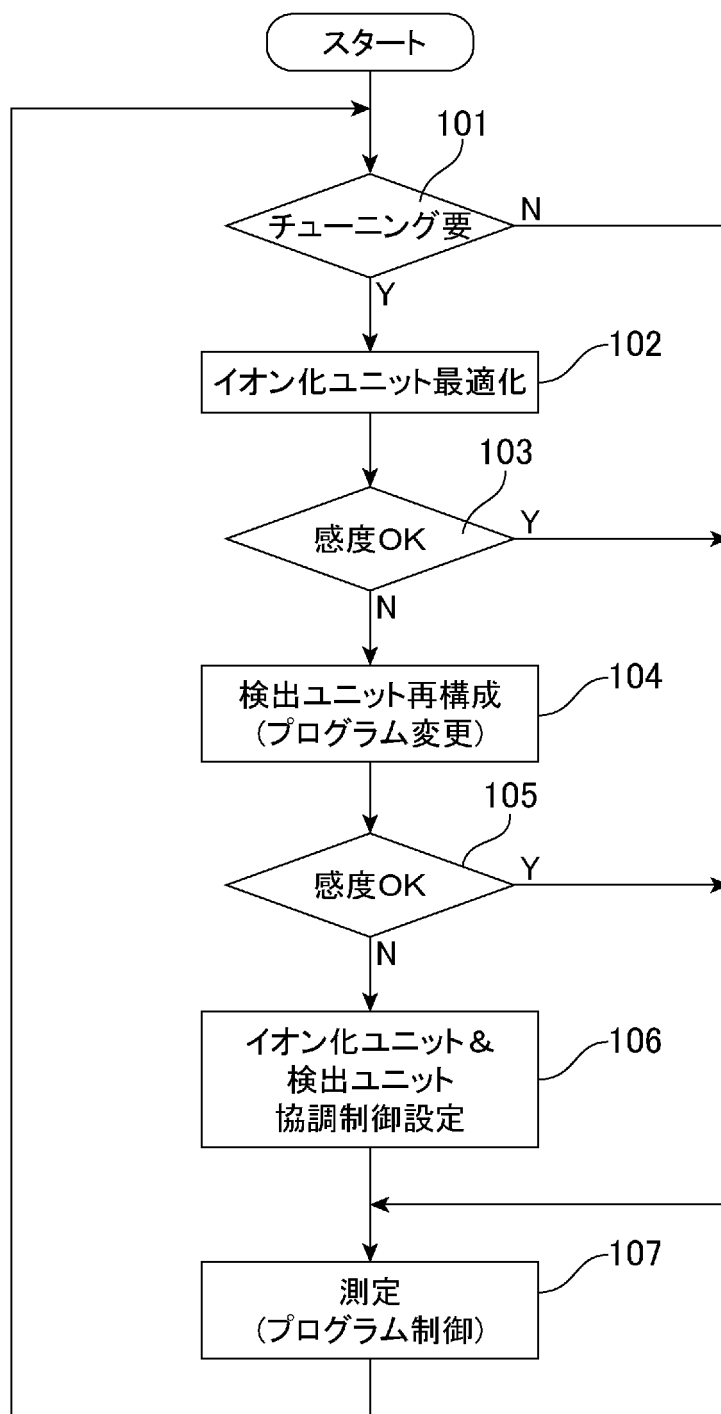


[図3]



The diagram illustrates a system architecture. At the top, a large grid labeled 50 is shown. Below it, a processing unit 80 is depicted, containing three main components: a 'サンプリング' (Sampling) block 81, an 'ADC' (Analog-to-Digital Converter) block 82, and a 'コンフィギュレーションドライバ' (Configuration Driver) block 83. The grid 50 is connected to the sampling block 81. The sampling block 81 is connected to the ADC block 82, which outputs a signal 90. The ADC block 82 is also connected to the configuration driver block 83. The configuration driver block 83 is connected to the grid 50 and also receives input from a signal 89. A data path 87 connects the configuration driver block 83 to a storage unit 88. The storage unit 88 contains three grids: 88A, 88B, and 88C, all of which are labeled with the reference numeral 51. Arrows indicate the flow of data and control signals between these components.

[図5]



[図6]

