



## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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| (51) International Patent Classification <sup>6</sup> :<br><b>G06F 9/46, 13/24</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | <b>A1</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | (11) International Publication Number: <b>WO 99/32971</b><br>(43) International Publication Date: <b>1 July 1999 (01.07.99)</b> |
| <p>(21) International Application Number: <b>PCT/US98/26500</b></p> <p>(22) International Filing Date: <b>11 December 1998 (11.12.98)</b></p> <p>(30) Priority Data:<br/><b>08/997,103</b>      <b>23 December 1997 (23.12.97)</b>      <b>US</b></p> <p>(71) Applicant (for all designated States except US): <b>INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).</b></p> <p>(72) Inventor; and<br/>(75) Inventor/Applicant (for US only): <b>PAWLOWSKI, Stephen, S. [US/US]; 6624 S.W. 158th Avenue, Beaverton, OR 97007 (US).</b></p> <p>(74) Agents: <b>TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor &amp; Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).</b></p> | <p>(81) Designated States: <b>AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</b></p> <p><b>Published</b><br/><i>With international search report.</i><br/><i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p> |                                                                                                                                 |

(54) Title: **MECHANISMS FOR CONVERTING INTERRUPT REQUEST SIGNALS ON ADDRESS AND DATA LINES TO INTERRUPT MESSAGE SIGNALS**

## (57) Abstract

In one embodiment of the invention, an apparatus (10) includes address and data ports (104, 106) to receive an interrupt request signal in the form of address signals and data signals (44). The apparatus (10) also includes decode logic (122) to receive at least some of the address signals and data signals (44) and provide a decoded signal at one of several decode output lines (124) of the decode logic (122). A redirection table (128) includes a send pending bit that is set responsive to the decode signal. In another embodiment, an apparatus (10) includes dedicated interrupt ports (38) to receive an interrupt request signal. The apparatus (10) also includes address and data ports (104, 106) capable of receiving an interrupt request signal in the form of address signals and data signals (114, 116), and decode logic (122) to provide a decode signal at one of several decode output lines (124) in response to reception of the interrupt request signal in the form of address signals and data signals (114, 116).

