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(71) Applicant: MOTOROLA, INC., A CORPORATION OF THE STATE OF DELAWARE [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventor: MOYER, William, C.; 1005 Pier Branch Road, Dripping Springs, TX 78620 (US).

(74) Agents: KOCH, William, E., et al.; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

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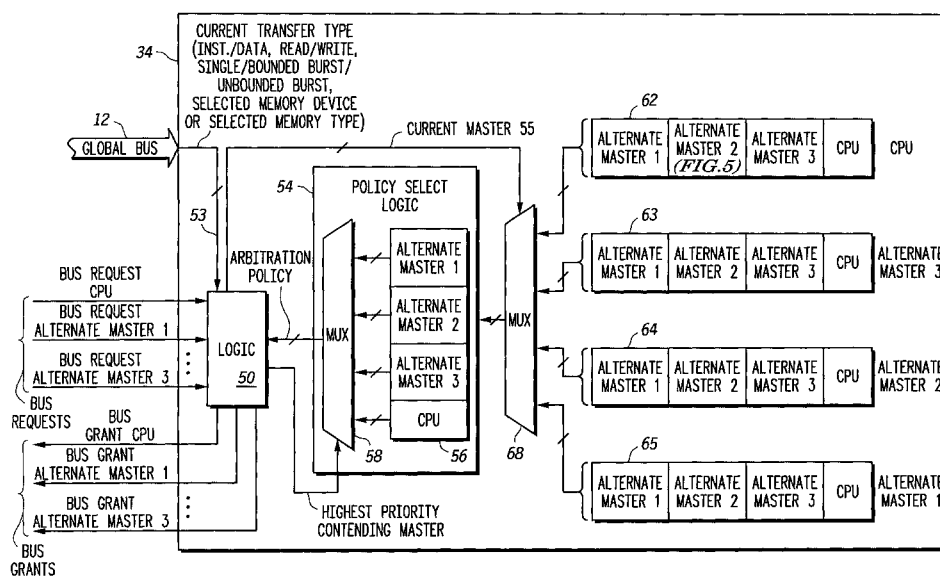
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(54) Title: SYSTEM AND METHOD FOR CONTROLLING BUS ARBITRATION DURING CACHE MEMORY BURST CYCLES



(57) Abstract: A bus arbiter (34) monitors characteristics associated with the type of information that is transferred via a global data bus (12) during burst transactions of information. A user-controlled arbitration policy register (56) may be programmed with values that are decoded to control whether interruption by a requesting bus master are permitted. Various factors can be used to determine interrupt permissions. Examples of such factors include the type of requesting device, whether a burst transaction is bounded or unbounded, whether a transaction is a read or a write of a system memory and the identity of the particular device requesting bus mastership.



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